TM 11-5895-479-35

TECHNICAL MANUAL

Direct Support, General Support, Depot

Maintenance Manual

Interrogator

Set

AN/TPX-41

This copy is a reprint which includes current pages from Changes 1 and 2.

HEADQUARTERS DEPARTMENT OF THE ARMY

November 1971

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on the 117-volt ac circuits and the 300-volt dc circuit.

DON'T TAKE CHANCES

EXTREMELY DANGEROUS VOLTAGES
EXIST IN RECEIVER - TRANSMITTER
RADIO RT-264D/UPX-6

Voltage as high as 3500 volts dc are present in this unit

TOXIC FUMES RESULT FROM
BURNED SELENIUM RECTIFIERS

Failed of selenium rectifiers in KY-97C/TPX and RT-264D/UPX-6 can result in liberation of poisonous fumes and deposit of poisonous selenium compounds. If a rectifier burns out or arcs over, the odor is strong. Provide adequate ventilation immediately. Avoid inhaling fumes and do not handle damaged rectifier until it has cooled.

TECHNICAL MANUAL
No. 11-5895-479-35

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D. C., 4 November 1971

Direct Support, General Support, DS, GS, and Depot Maintenance Manual Interrogator Set AN/TPX-41

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CHAPTER 1
INTRODUCTION

1-1. Scope

a. General. This manual contains direct support, general support, and depot level maintenance instructions for Interrogator Set AN/TPX-41. Coverage includes equipment theory of operation, and essential troubleshooting, testing, and maintenance instructions for each specific level of maintenance.

b. Complete Manual. The complete manual for the AN/TPX-41 includes TM 11-5895-479-12 and TM 11-5895-479-34P, TM 11-5895-201-35, TM 11-5895-201-24P, TM 11-5895-245-35, TM 11-5840-309-35, TM 11-5840-309-35P, TM 11-5840-326-35, and TM 11-5840-326-35P.

NOTE

Applicable forms and records are covered in TM 11-5895-479-12.

1-2. Indexes of Publications

Refer to the latest issues of DA Pam 310-4 and DA Pam 310-7 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-3. Reporting of Errors

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forwarded direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

1-3. Reporting Equipment Improvement Recommendations (EIR)

EIR's will be prepared using Standard Form 368, Quality Deficiency Report. Instructions for preparing EIR's are provided in TM 38-750, The Army Maintenance Management System. EIR's should be hailed direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703. A reply will be furnished direct to you.

1-4. Internal Equipment Differences

a In some Modulator, Pulse MD-638/TPX-41 units, 47k resistors (type RC42GF473J) are used in place of 27k resistors for R1336, and R1361, and 0.01-uf capacitors (type C009-AIKF103K3) are used in place of 0.015-uf capacitors for C1310 and C1318 shown in figure FO-12 because the manufacturer of associated silicon controlled rectifiers CR1314, CR1316, CR1326 and CR1328 (type G390045S1) (fig. FO-12) no longer supplies these rectifiers to existing (10 ma) holding current specifications.

NOTE

When CR1314 and CR1316 in the MD-638/TPX-41 units that do not reflect this change are replaced, R1336 and C1310 should also be replaced with the aforementioned 47k resistor and a 0.01-uf capacitor. In like manner, when CR1326 and CR1328 are replaced, R1361 and C1361 and C1318 should also be replaced with the aforementioned 47k resistor and 0.0001-uf capacitor. The end item performance standard will be met when these changes are made.

b. In some MD-638/TPX-41 units, CP WIDTH ADJ control R1363, a 2500-ohm variable resistor (type RV6SLAYSL252A), is inserted between R1347 and the junction of CR1323 and C1314 shown in figure FO-12; and the value of R1347 is changed from 4700 ohms to 3300 ohms. In these equipments, adjustment of the width of the control pulse signal is therefore provided, but the control pulse duration performance standard (1.2 to 0.2 usec) remains the same.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. SYSTEM ANALYSIS

2-1. Interrogator Set AN/TPX-41 System Analysis

a. When provided with the proper input power, Interrogator Set AN / TPX-41 operates as a complete aircraft identification system, capable of interrogating aircraft, analyzing their replies, and producing identification video for display on the indicator of an associated radar set. System operation of the AN / TPX-41 is described in a through *l* below. A block diagram of the system and the basic subsystems which comprise the AN / TPX-41 is shown in figure 2-1.

b. Application and distribution of system power is controlled through the power distribution system. This system is comprised of interconnecting and switching circuitry for application of ac system power and antenna drive voltage. Most subsystems of the AN / TPX-41 contain individual power supplies which convert ac system power to controlled voltages that can be used within the individual subsystems. Antenna drive voltage is applied to an ac drive motor which rotates the IFF antenna at a constant speed. As the antenna rotates, a synchro transmitter located in the antenna system produces antenna position synchro data. This synchro data is routed from the antenna system to the indicator of the associated radar to synchronize the IFF sweep with antenna rotation.

c. An aircraft interrogation cycle is initiated by an IFF pretrigger which is generated in the timing system. The timing system also produces a display trigger and a 1500-Hz radar synchronizing signal. The display trigger is applied to the indicator of the associated radar set to establish the IFF sweep start time. The 1500-Hz radar synchronizing signal is applied to a synchronizer circuit in the associated radar set. This synchronizer circuit produces radar transmitter triggers in direct synchronization with the applied 1500-Hz synchronizing signal. A delay multivibrator circuit within the IFF timing system is used to synchronize the 1500-Hz synchronizing signal to establish the correct time relationship between radar echoes and IFF replies.

d. The IFF pretrigger produced in the timing system is applied to the coding system to initiate interrogation coding. This code is comprised of two pulses whose interpulse spacing is determined by the selected mode of interrogation. Mode selection may be accomplished through direct switching in the coding system but is usually made at a remote switching location convenient to the radar operator.

e. The coded pulse pairs from the coding system are applied to the interrogation side-lobe suppression (isls) system where a third pulse (P2) is developed for isls operation. The isls system also produces bias voltage and a control pulse which is applied to the antenna system during transmission of the isls pulse (P2).

f. The coded pulse pair and the P2 pulse are routed from the isls system and applied to a modulator in the transmitting system. The resultant output of the transmitting system consists of three high-power, RF pulses which maintain the same spacing characteristics as the input pulses.

g. The RF output pulses from the transmitting system are rerouted back to the isls system where they are diplexed with dc bias voltage and the control pulse described in *e* above. The combined de bias, control pulse, and RF transmitter pulses are then coupled from the isls system to the antenna system.

h. The antenna system accepts the signals from the isls system and provides directional beam transmission of the coded RF pulses and the P2

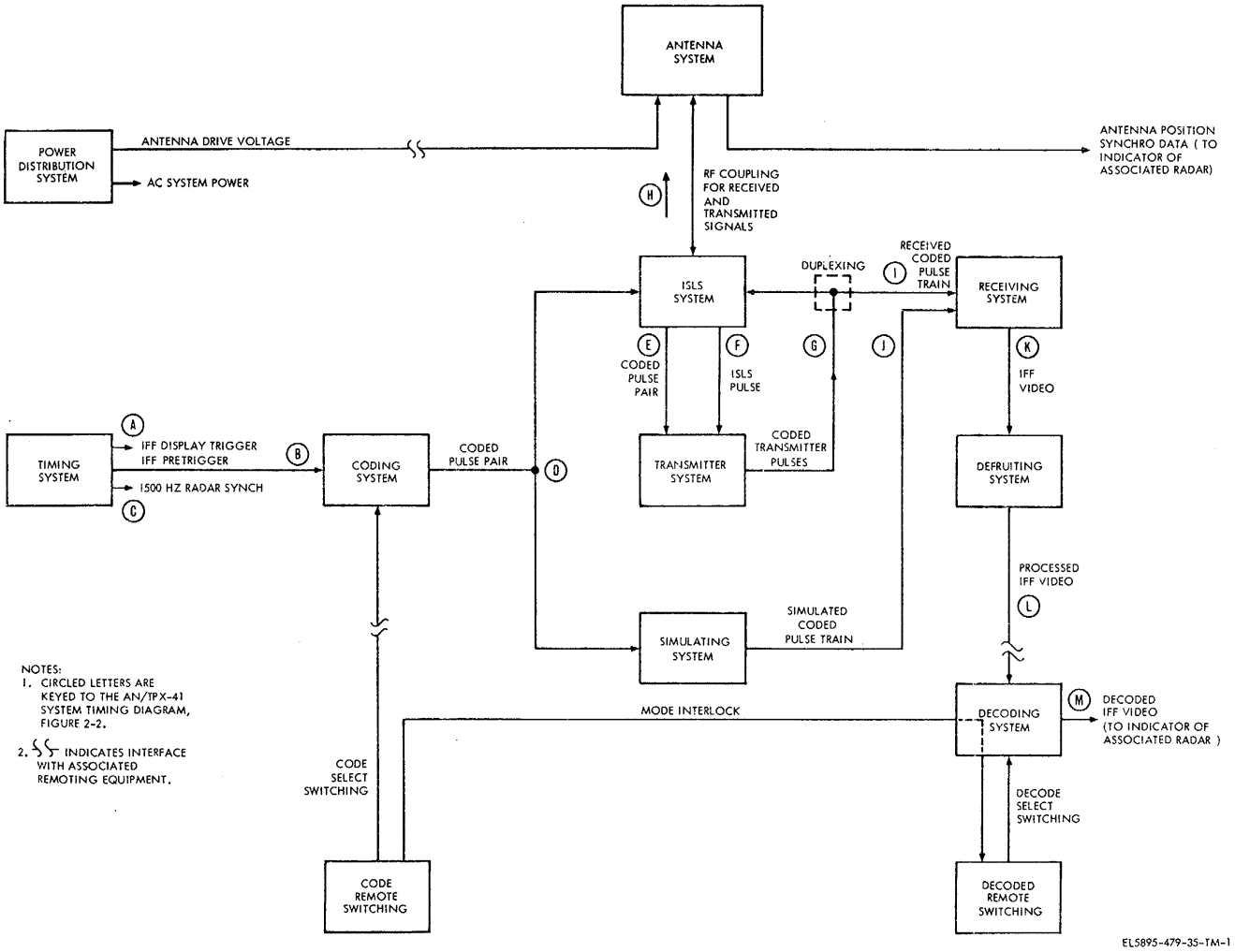


Figure 2-1. Interrogator Set AN/TPX-41, system block diagram.

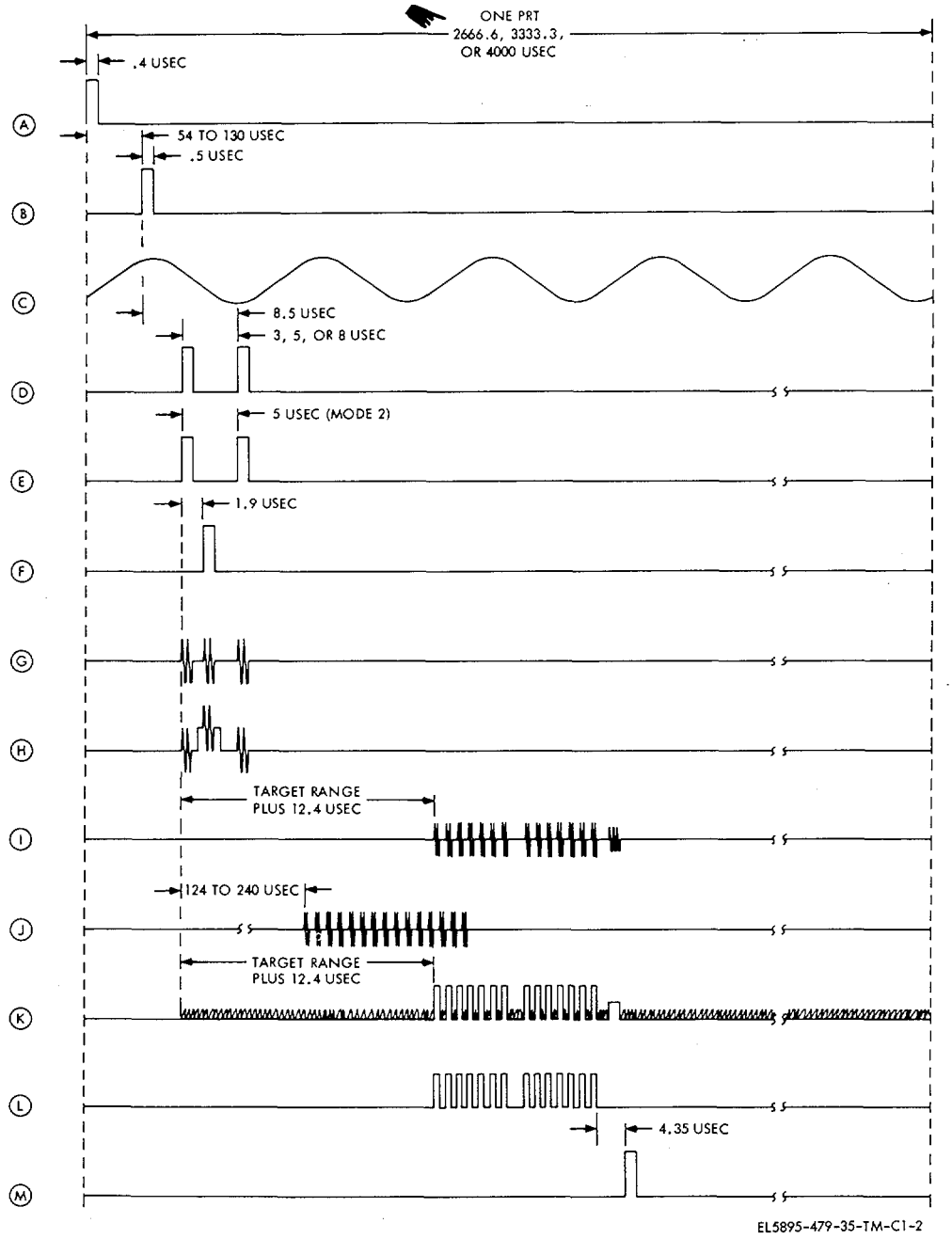


Figure 2-2. Interrogator Set AN/TPX-41, system timing diagram.

pulse. The dc bias voltage and control pulse produced in the isls system, activates elements of the antenna to provide separate beam transmission of the coded pulse pair and the P2 pulse. During transmission of the coded pulse pair, dc bias activates antenna elements to produce a normal sum pattern radiation beam. When the P2 pulse is present, the control pulse activates antenna elements to cause radiation of a difference pattern beam. The difference pattern is a broad beam of RF energy with a deep narrow null in the center which straddles the sum pattern beam. Comparison circuitry in the airborne transponder permits an IFF reply to be transmitted only when the difference pattern pulse is approximately 9 db down from the sum pattern pulses. Thus, an aircraft will reply only when it is close to the center of the sum pattern beam (a narrow sector when the difference pattern is at a null). To eliminate false interrogation of nearby aircraft caused by antenna side- and back-lobe energy, a small amount of difference pattern energy is

transmitted by a backfill dipole antenna mounted on the rear of the main antenna. This acts on the airborne transponder the same way as the main beams and prevents replies from the side and back lobes.

i. Coded replies from airborne transponders are received by the antenna system, coupled through the isls system, and applied to the receiving system through the receiver-transmitter duplexer. This duplexer protects the receiving system from high-power RF energy during transmission time and provides minimum impedance to received signals during reception time. The receiving system detects, amplifies, and shapes the received coded pulse trains to produce low-noise IFF video. The resultant output of the receiving system is a coded video pulse train which maintains all of the code characteristics of the received signal (including nonsynchronous signals).

j. The IFF video output of the receiving system is coupled to the defruiting system where it is processed to eliminate nonsynchronous signals. This processing is accomplished by comparing the received video with the video of a previous pulse train, delayed one pulse period. Coincidence circuitry within the defruiting system produces an output only during coincidence of the two video signals. This results in a video output which contains only those pulses that are synchronous from successive interpulse periods.

k. The final video output of the defruiting system is applied to the decoding system as processed IFF video. The decoding system accepts and analyses the video pulse trains to determine whether the pulse train information corresponds to a preselected decode setting. This decode setting is accomplished at a remote switching unit which is located in a position convenient to the radar operator. The remote switching unit provides decode select switching to set decoding circuits in the decoding system. To accomplish successful interrogation, the decoding system must be set to decode in the mode of interrogation established by the coding system. For this reason, a mode interlock is connected between code and decode switching circuits. The mode interlock ensures that the coding and decoding systems are both set to operate in the same mode of interrogation. When a video pulse-train corresponds to the preselected decode setting in the decoding system, a decoded IFF video output is produced. The decoded IFF video is routed from the decoding system and applied to the indicator of the associated radar set. The resultant display on the indicator crt is an arc or series of arcs that appear adjacent to the aircraft radar echo. This presentation may be interpreted by the radar operator to establish various types of identification. The types and methods of identification which can be accomplished by the AN/TPX-41 are described in the operating instructions contained in TM 11-5895-479-12.

l. In addition to the operating systems described in *b* through h above, the AN/TPX-41 employs a simulating system for testing purposes. The simulating system receives coded pulse pairs from the coding system and produces a simulated IFF pulse train. This pulse train consists of a standard mode 2 test formation which is applied to the receiving system. Application of this test pulse train permits overall analysis of the coding, receiving, and decoding systems without the need for external transponder replies.

2-2. Timing System Functioning

a. General. The timing system provides gating and trigger signals essential for synchronous operation of the AN/TPX-41 and the associated radar set. The system is essentially contained on two plug-in circuit board assemblies in Blanker, Interference MX-8795/TPX-41. Trigger and gate generating circuits are contained on circuit card assembly trigger/gate generator (chassis series 30900). Amplifier and oscillator circuits are contained on circuit card assembly synchronizer multiplier (chassis series 31000). In addition to these circuits, the timing system also uses a recirculating loop in the defruiting system. The defruiting system is also contained in Blanker, Interference MX-8795/TPX-41 and is discussed in paragraph 2-8. System operation of the timing system is described in *b* and c below. A block diagram of the timing system is shown in figure 2-3.

b. Trigger and Gate Generating Circuits. Timing system trigger and gate generating circuits are located on the trigger/gate generator (chassis series 30900). On initial application of timing system power, astable multivibrator Q1 and Q2 attempts to free run at a natural prf of 182.5 pps. A circulated iff pretrigger is applied to the input of the multivibrator to produce a stable pulsed output, This output is differentiated and coupled to trigger shaper Q3. The trigger shaper shapes and amplifies an input pulse to produce a positive output trigger of proper

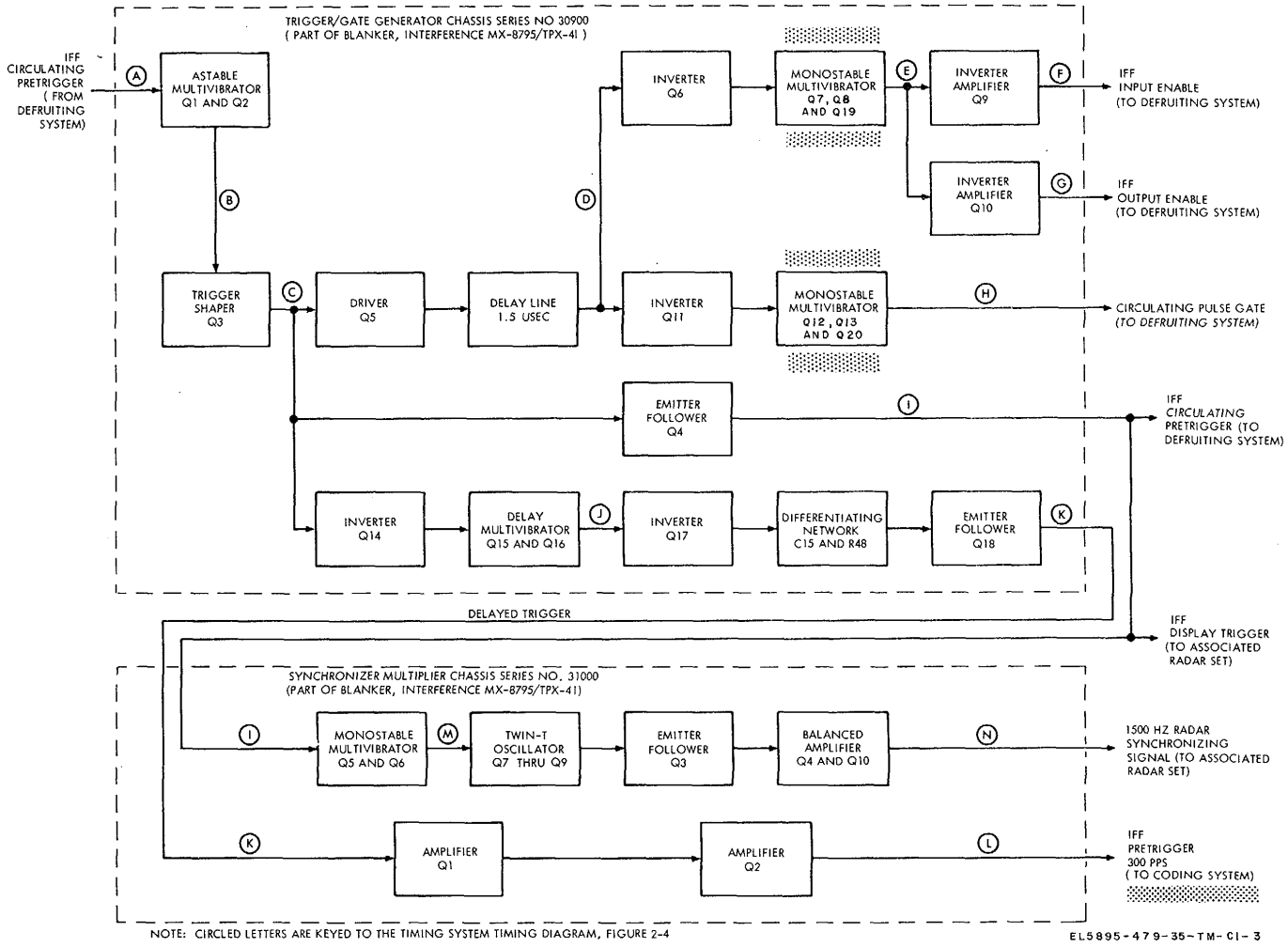


Figure 2-3. Timing system, block diagram.

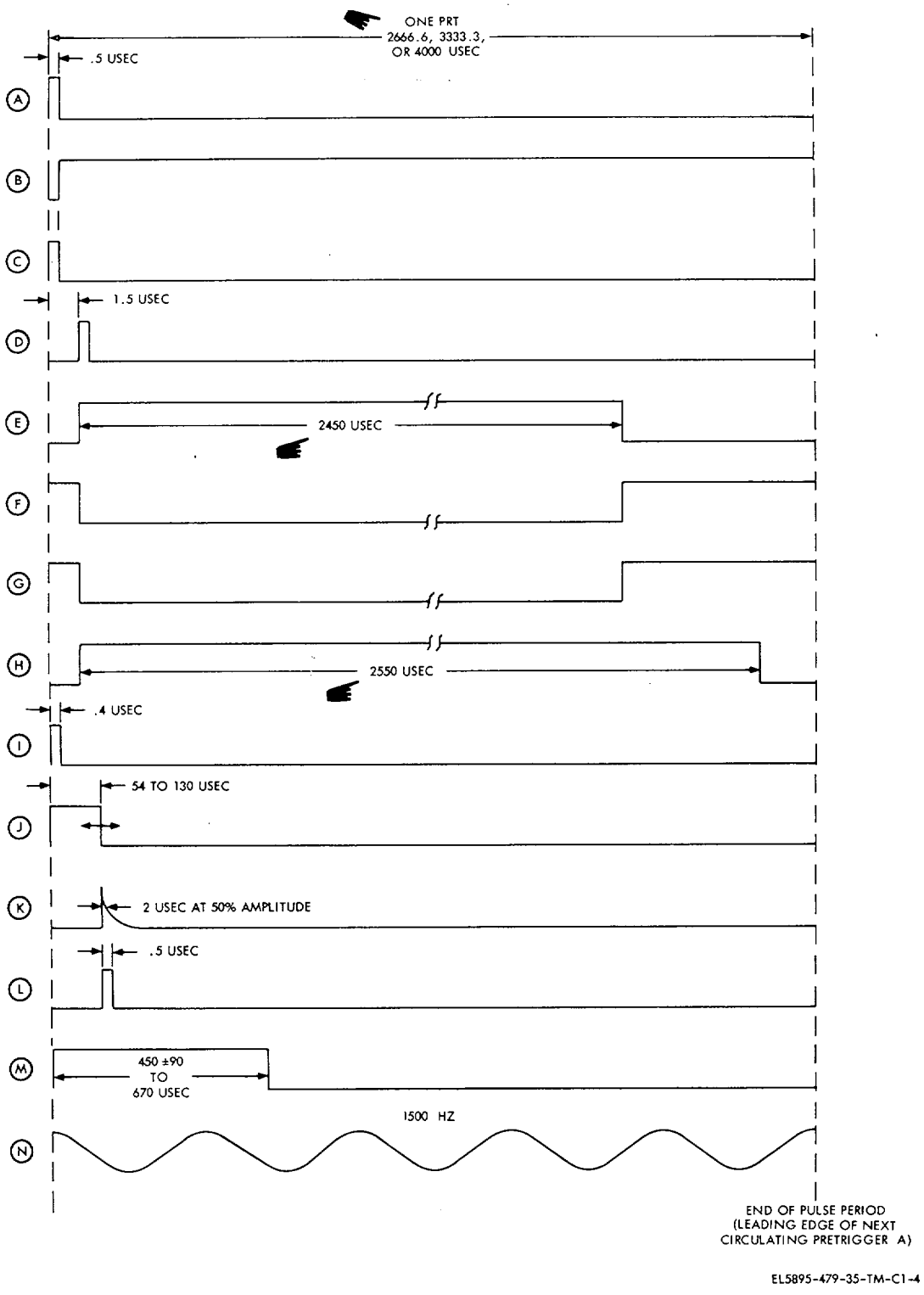


Figure 2-4. Timing system, timing diagram.

amplitude and duration. This trigger is coupled from the output of Q3 to emitter follower Q4, driver Q5, and inverter Q14. The trigger is coupled through driver Q5, delayed 1.5 μsec, and applied to inverters Q6 and Q11 Inverter Q11 produces an inverted trigger output which is applied to monostable multivibrator Q12 and Q13. On receipt of the trigger, the multivibrator produces a

circulating pulse gate that is routed to the defruiting system to determine circulating *protrigger* time coincidence. The inverted trigger at the output of Q6 triggers monostable multivibrator Q7 and Q8 to produce a gating pulse at the output of the multivibrator. The gating pulse is coupled to inverter amplifiers Q9 and Q10, resulting in an inverted amplified gate pulse at the respective outputs of Q9 and Q10. The output of inverter amplifier Q9 is routed to the defruiting system as the IFF input enable gate. The output of QIO is applied to the defruiting system as the IFF output enable gate. The trigger input to emitter follower Q4 is coupled through the emitter follower and applied to the defruiting system as the circulating pretrigger. In the defruiting system, the trigger is delayed for one interpulse period, compared for proper time coincidence, and routed back to the timing system to reset astable multivibrator QI and Q2. This method of triggering the astable multivibrator insures that each pulse period is equal to the delay time of the delay line in the defruiting system. The trigger input to inverter Q14 results in the application of an inverted trigger to delay multivibrator Q 15 and Q16. On receipt of the trigger, the delay multivibrator produces a positive pulse output which is inverted through Q17 and applied to differentiating network C15 and R48 as a negative pulse. The differentiating network develops a negative trigger representing the leading edge of the pulse and a positive trigger representing the trailing edge of the pulse. Only the positive trigger is coupled through emitter follower Q18 to produce a delayed trigger at the output of Q18. The delay of this trigger is equal to the pulse duration time at the output of delay multivibrator Q15 and Q 16. The delayed trigger is routed out of the trigger/gate generator and applied to the synchronizer multiplier (chassis series 31000). The circulating pretrigger at the output of emitter follower Q4 is routed to two locations is addition to the defruiting system. One output is applied to the associated radar set as the IFF display trigger.
Another output is routed out of the trigger/gate generator and applied to the synchronizer multiplier along with the delayed trigger.

c. Synchronizing and Multiplying Circuits. Timing system synchronizing and multiplying circuits are located on the synchronizer multiplier (chassis series 31000). Amplifier QI receives the delayed trigger from emitter follower Q30918 in the trigger/gate generator (chassis series 30900). The delayed trigger is amplified and inverted by QI and ac-coupled to amplifier Q2 Amplifier Q2 provides a second stage of amplification and inversion for the delayed trigger and accomplishes impedance matching to the coaxial line output. The trigger output of amplifier Q2 is routed out of the synchronizer multiplier and applied to the coding system as the IFF pretrigger. Monostable multivibrator Q5 and Q6 receives a circulating pretrigger from the output of emitter follower Q30904 in the trigger / gate generator. On receipt of the circulating pretrigger, monostable multivibrator Q5 and Q6 produces a pulsed output which has an adjustable duration. This output i: differentiated and the negative trigger is rc couple(at a 0-volt reference to the input of a twin-' oscillator consisting of Q7, Q8, and Q9. The twin-T oscillator operates at a free-running frequency o approximately 1500 Hz. The negative trigger at the oscillator input serves as a synchronizing signal by providing phase correction once every pretrigger interpulse period. At this rate, phase correction is accomplished every 4, 5, or 6 cycles of the 1500-H2 oscillator frequency, depending on the selected IFF prf. The 1500-Hz output of the twin-T oscillator i, applied to balance amplifier Q4 and QIO, where ii is amplified, and adjusted for symmetrical balance.

The final output of the balanced amplifier is routed out of the synchronizer multiplier and applied to the synchronizer assembly of the associated radar set as a 1500-Hz radar synchronizing signal.

2-3. Coding System Functioning

a. General. The coding system produces coded pulse pairs to initiate operation of the isls, transmitting, receiving, and simulating systems. The coded pulse pairs are produced in response to IFF pretriggers received from the timing system and are spaced to represent the selected mode of interrogation. Primary control functions of the coding system are of two types: controls which regulate interpulse spacing and select the challenge mode, and controls which regulate performance of the receiving system. Switching circuitry within the coding system permits remote operation of the control functions at a remote control unit. The primary coding circuits and control functions of the coding system are contained in Coder-Control KY97C/TPX. Coding system remote controls are located on Control, Remote Switching C1271A/TPX-22. System operation of the coding system is described in *b* through e below. A block diagram of the coding system is shown in figure 2-5.

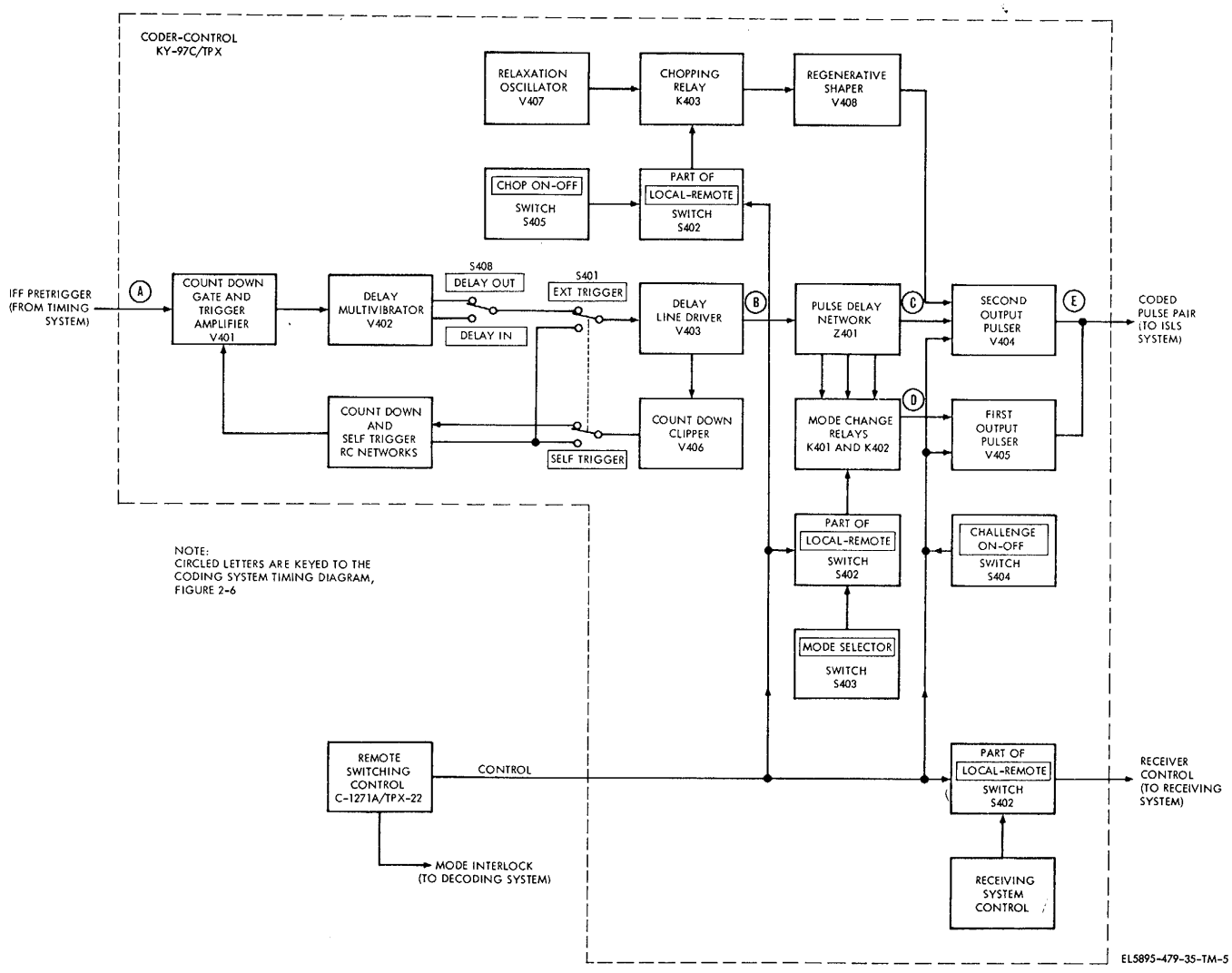


Figure 2-5. Coding system, block diagram.

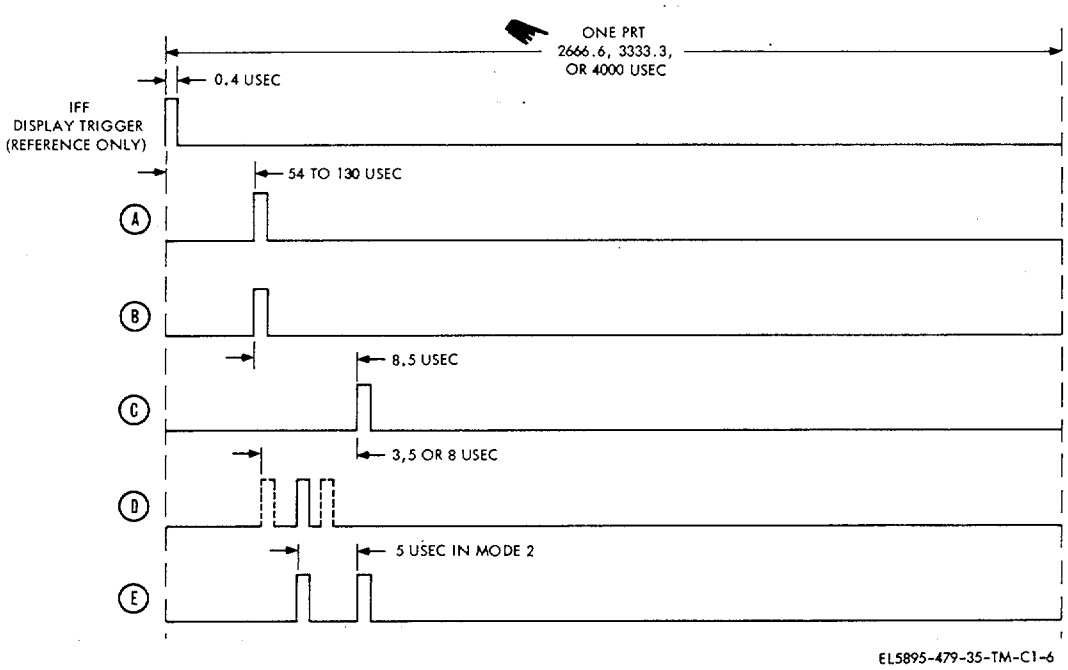


Figure 2-6. Coding system, timing diagram.

b. Trigger Countdown and Delay Circuits. Trigger countdown and delay circuits in the coding system may be used to accomplish two principle functions: produce triggers at a reduced pulse repetition rate from that of the input triggers and delay these triggers to establish the correct time relationship with the associated radar set. These functions are not used in application with the AN/TPX-41 system because the system pulse repetition rate and necessary delay is established in the timing system (para 2-2). The IFF pretrigger from the timing system is applied to countdown gate and trigger amplifier V401 where it is amplified and then coupled to delay multivibrator V402. The delay multivibrator produces a delayed and undelayed output pulse. When used with the AN/TPX-41, the DELAY IN-DELAY OUT switch, S408, is left in the DELAY OUT position and the undelayed output of V402 is coupled through EXT TRIGGER-SELF TRIGGER switch S401 to delay line driver V403. On receipt of the undelayed pulse, the delay line driver produces a positive trigger pulse which is applied to pulse delay network Z401. The delay line driver also produces a negative pulse which forces countdown clipper V406 into conduction. The conduction of V406 initiates development of a negative-going voltage level from the countdown rc network. This voltage is adjusted for a desired exponential rate of change and applied to countd3own gate and trigger amplifier V401 as cutoff bias. The exponential change rate of this bias determines the conduction time of V401, thereby limiting the number of input triggers that are accepted and amplified by the stage. The pulse repetition rate of IFF pretriggers from the timing system is such that this countdown action has no effect and IFF pretriggers are accepted and amplified on a one-for-one basis. When EXT TRIGGE.P-SELF TRIGGER switch S401 is placed to the SELF TRIGGER position, delay line driver V403 functions as a relaxation oscillator with countdown clipper V406 providing feedback to a self-trigger rc network. The rc network provides a fixed time constant which causes the relaxation oscillator to produce pulses, at a pulse repetition rate of 200 pps. This feature permits operation of the coding system for test purposes without the need for an external trigger.

c. Mode Spacing Circuits. The positive trigger pulse at the output of delay line driver V403 is applied to the input of pulse delay network Z401. The pulse delay network provides a total delay of 8.5 usec from input to final output. The positive trigger pulse applied to the input of Z401 is fed through Z401 and applied to second output pulser V404 delayed by 8.5 μsec. In addition to the total of 8.5 μsec, taps connected at points along the pulse delay network provide shorter delays permitting pulse outputs that occur 3, 5, or 8 μsec before the final pulse output. The condition of

mode change relays K401 and K402 determines which of these outputs is applied to first output pulser V405. MODE SELECTOR SWITCH switch S403 controls energization of these relays to provide selection of 3-, 5-, or 8-μsec intervals between pulse inputs to the first and second output pulsers.

d. Output Pulser Circuit. The output pulser circuit is comprised of the first and second output pulsers (V404 and V405, respectively) and CHALLENGE ON-OFF switch S404. The positive pulse input to first input pulser V405 arrives 3, 5 or 8 μsec (determined by the setting of MODE SELECTOR switch S403) before the input to second output pulser V404. When CHALLENGE ON-OFF switch S404 is placed to ON, bias voltage is applied to the output pulser stages causing them to produce positive pulse-outputs in response to their respective inputs. These outputs are combined to form a coded pulse pair with interpulse spacing of 3, 5 or 8 usec, representing challenge modes 1, 2, and 3, respectively. The coded pulse pair is routed out of the coding system and applied to the isls and simulating systems to initiate actual or simulated interrogation.

e. Chop Rate Circuit. The chop rate circuit interrupts operation of the second output pulser stage to reduce the number of pulse pairs applied to the transmitting system. This, in turn, results in fewer replies from aircraft transponders. The final result is an IFF reply which appears as a series of dashes (rather than a solid arc) on the ppi of the associated radar set. Relaxation oscillator V407 operates at an adjustable frequency that permits second output pulser V404 to be disabled up to 60 percent of the time and permitted to fire only 40 percent of the time. When CHOP ON-OFF switch S405 is placed to ON, chopping relay K403 energizes and positive pulses from the output of V407 are fed to regenerative shaper V408. This results in the development of negative squarewave pulses at the output of V408. These negative pulses are coupled to the shield grid of the second output pulser to disable the stage at a rate determined by the frequency of relaxation oscillator V407. When the second output pulser stage is disabled, only the first output pulser produces an output. Since aircraft transponders reply to only pulse pairs, no replies are transmitted during the absence of the second pulse and the chopping effect is achieved.

f. Remote Control Circuits. Under normal operating conditions, the control functions of the coding system are accomplished at Control, Remote Switching C-1271A/TPX-22. This transfer of control is accomplished by placing LOCAL-REMOTE switch S402, on the KY-97C/TPX, to the REMOTE position. When this is done, functions of MODE SELECTOR switch S403, CHOP ON-OFF switch S405, and receiving system controls are transferred to identical controls on the C-1271A/TPX--22. A PUSH TO CHAL switch on the C-1 271A/TPX-22 is not connected through LOCAL-REMOTE switch S402, but is connected directly in parallel with CHALLENGE ON-OFF switch S404. The PUSH TO CHAL switch accomplishes the same electrical function as CHALLENGE ON-OFF switch S404, but operates on a spring-loaded, pushbutton principle. This permits an operator to challenge specific aircraft by momentarily depressing the PUSH TO CHAL switch at the operator's option. Effective use of the PUSH TO CHAL switch requires that CHALLENGE ON--OFF switch S404 be set to OFF so that continuous interrogation does not take place. The MODE SELECTOR switch on the C-1271A/TPX-22 is connected to a mode interlock circuit which is located in the decoding system. This interlock circuit ensures that the decoding system will operate in the mode of interrogation selected by the MODE SELECTOR switch on the C-1271A/TPX-22.

2-4. Isis System Functioning

a. The interrogation-path side lobe suppression (isls) system receives the coded pulse pair from the coding system and produces a third pulse (P2), control pulse, and dc bias for isls operation. The original coded pulse pair and the P2 pulse are applied to the transmitting system which in turn produces a train of three RF pulses for transmission. The three pulses are routed back to the isls system, combined with the control pulse and dc bias, and coupled to the antenna system. The dc bias and control pulse activate antenna elements to provide separate beam patterns for transmission of the coded pulse pair and the P2 pulse. Elements of the antenna system which operate in conjunction with the isls system are described in paragraph 2-6. System operation of the basic isls system, which is contained in Modulator, Pulse MD-638/TPX-41, is described in b through r below. A block diagram of the isls system is shown in figure 2--7.

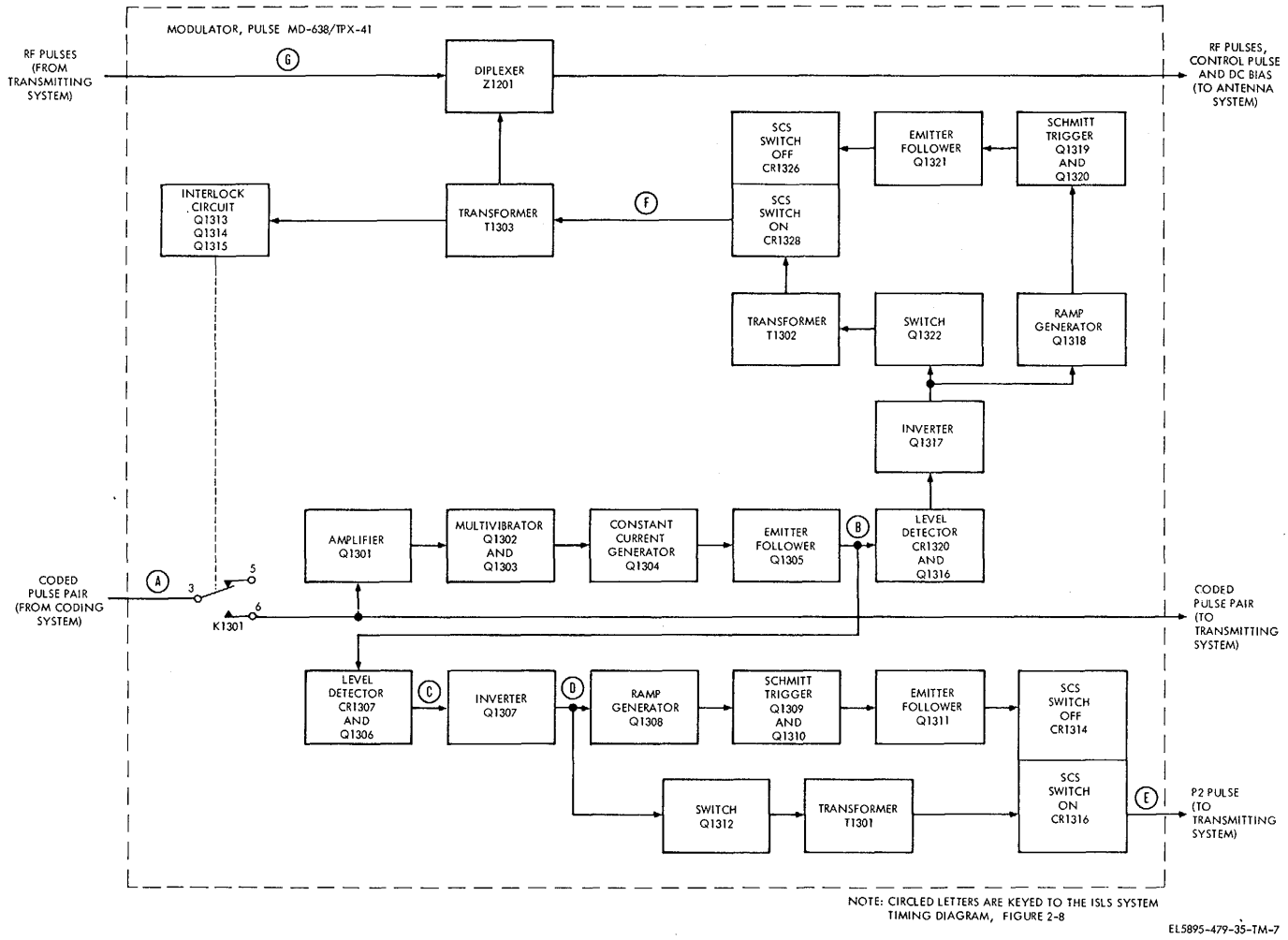


Figure 2-7. Isls system, block diagram.

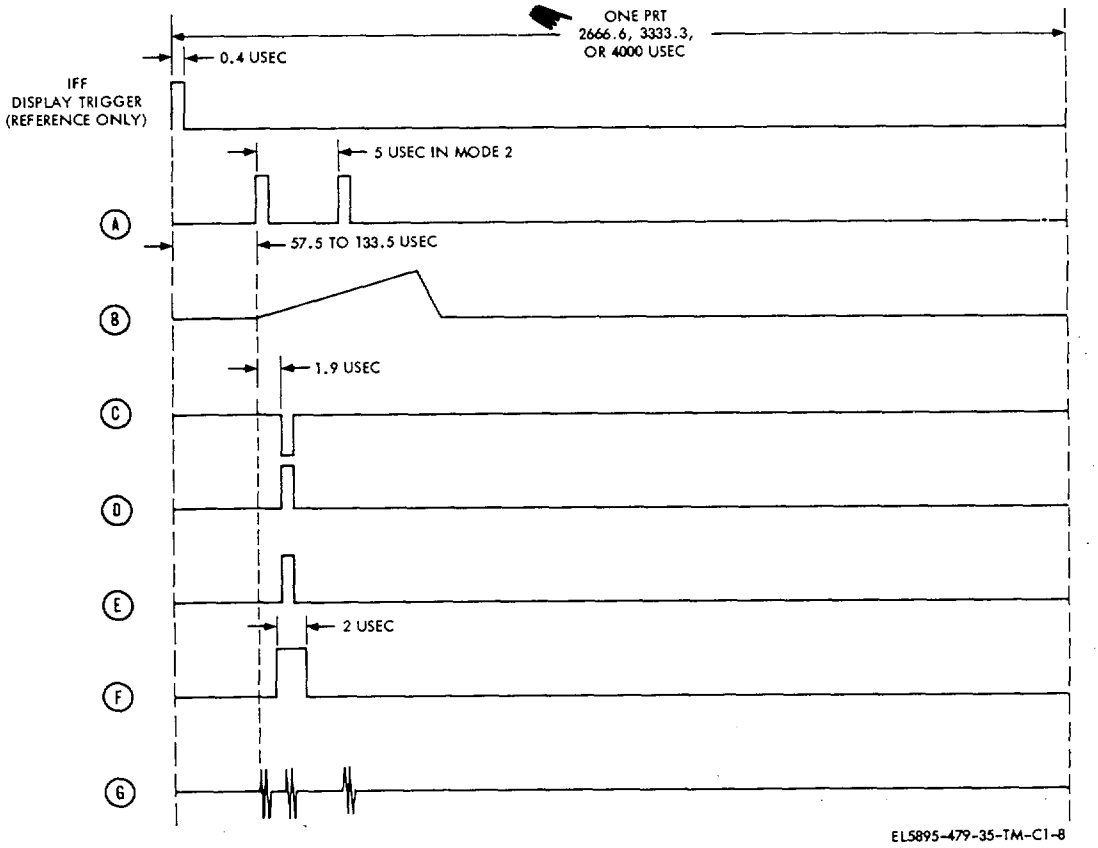


Figure 2-8. Isls system, timing diagram.

b. The delay ramp generator section, consisting of amplifier Q1301, multivibrator Q1302 and Q1303, constant current generator Q1304, and emitter follower Q1305, is contained in the pulse generator processor subassembly located in the MD-638/TPX-41. It is in this section that a linear ramp is produced which generates a delayed pulse for insertion between the coded pulse pair received from the coding system.

c. The coded pulse pair from the coding system is applied to contact 3 of relay K1301. On application of isls system power, relay K1301 energizes and the coded pulse pair is routed out of the MD-638/TPX-41 and applied to the transmitting system. The coded pulse pair is also coupled through K1301 to the base of amplifier Q1301. Amplifier Q1301, which is biased near cutoff, inverts and amplifies the coded pulse pair. The negative output of Q1301 is coupled to multivibrator Q1302 and Q1303 in the delay ramp generator section of the pulse generator processor subassembly.

d. Multivibrator Q1302 and Q1303 is a one-shot multivibrator, in which Q1302 is normally cut off and Q1303 is normally conducting. The negative pulse from Q1301 is coupled to Q1303. Transistor Q1303 is held at cut off by Q1301 for approximately 35 usec. A positive 35-usec gate is developed at the collector of Q1303 which is directly coupled to the constant current generator circuit at coupling diode CR1304.

e. The constant current generator circuit, which consists of coupling diode CR1304, clamp diode CR1305, reference diode CR1306, and constant current generator Q1304, is located within the delay ramp generator section of the MD-638/TPX-41. The positive gate from multivibrator Q1302 and Q1303 back biases CR1304, causing Q1304 to draw current. Zener diode CR1306 keeps voltage at Q1304 constant during the positive gate from multivibrator Q1302 and Q1303 permitting constant current flow. Clamp diode CR1305 provides temperature compensation during the charge cycle. The positive linear ramp from Q1304 is direct-coupled to emitter follower Q1305. Emitter follower Q1305 prevents level detectors Q1306 and Q1316 from impairing the linearity of the positive ramp from Q1304. The positive ramp developed at the emitter

of Q1305 is applied to the P2 pulse generator section and the control pulse generator section of the MD-638/TPX-41.

f. The P2 pulse generator section, consisting of tunnel diode CR1307, level detector Q1306, inverter Q1307, ramp generator Q1308, Schmitt trigger Q1309 and Q1310, emitter follower Q1311, switch Q1312, and silicon controlled switch generator CR1314 and CR1316 is contained in the pulse generator processor subassembly. It is in this section that a third pulse (P2) is generated for transmission of a difference pattern required for isls action.

g. The positive-going ramp from emitter follower Q1305 is applied to the level detector circuit of tunnel diode CR1307 and level detector Q1306. Level detector Q1306 is normally cut off. As the positive ramp increases in amplitude, Q1306 conducts. The point in time along the ramp at which the conduction of Q1306 occurs is determined by P2 DELAY ADJ control R1315 on the pulse generator processor subassembly. The resultant negative signal of Q1306 is coupled to inverter Q1307. The positive signal from Q1307 is applied to ramp generator Q1308 and switch Q1312.

h. Switch Q1312 inverts the positive signal from Q1307. The negative output from Q1312 is inverted through transformer T1301 and applied to the gate of the silicon-controlled switch generator at CR1316 (ON). When CR1316 is gated on by the positive signal from T1301, a sharp rise in voltage occurs, developing the leading edge of the P2 pulse. Silicon-controlled switch CR1316 remains on until silicon-controlled switch CR1314 is gated on.

i. The positive signal from inverter Q1307 is also applied to ramp generator Q1308 through coupling diode CR1312 (g above). P2 PULSE WIDTH ADJ control R1321 located on the pulse generator processor subassembly adjusts the steepness of the ramp voltage applied. The output of Q1308 is a positive linear ramp voltage.

j. Normally at the Schmitt trigger, Q1310 is conducting, while Q1309 is held cut off. The positive linear ramp voltage from Q1308 is applied to Q1309 and overcomes the bias level permitting conduction of Q1309. The negative pulse developed at the collector of Q1309 is coupled to the base of Q1310, cutting Q1310 off. The output of the Schmitt trigger at the collector of Q1310 is a positive pulse which is positioned in time by R1321 (i above). The positive pulse from Q1310 is applied to emitter follower Q1311. The output from Q1311 is a positive pulse applied to the gate of the silicon controlled switch generator at CR1314 (OFF). When CR1314 is gated on, CR1316 is gated off, developing the lagging edge of the P2 pulse. The P2 pulse is routed out of the MD-638/TPX-41 and applied to the transmitting system with the coded pulse pair described in c above.

h. The control pulse generator section, consisting of level detector Q1316, inverter Q1317, ramp generator Q1318, Schmitt trigger generator Q1319 and Q1320, emitter follower Q1321, switch Q1322, and silicon controlled switch generator CR1326 and CR1328, is contained in the pulse generator processor subassembly. Diplexer Z1201 located on the main chassis of the MD-638/TPX-41 also functions as part of the control pulse generator section. The control pulse generated in this section changes the bias in the RF switch in the antenna system, and causes the difference pattern to be transmitted during the time interval of the P2 pulse.

l. Between pulses, a tunnel diode CR1320 shunts most of the current keeping level detector Q1316 cut off. When the positive ramp from emitter follower Q1305 is applied to the control pulse generator section at CR1320 (e above), operation of CR1320 moves into the negative resistance region, current is no longer shunted by CR1320, and Q1316 is turned on. The delay of the negative pulse from Q1316 is adjusted by CP DELAY ADJ control R1343. While the width of the P2 pulse is adjustable (i above), the control pulse generator uses fixed circuit values for the same effect.

m. The negative pulse from Q1316 is coupled to inverter Q1317. The positive pulse from Q1317 is coupled to switch Q1322.

n. Switch Q1322 inverts the positive pulse from Q1317. The negative output from Q1322 is inverted through transformer T1302 and applied to the gate of the silicon-controlled switch generator at CR1328 (ON). When CR1328 is gated on by the positive signal from T1302, a sharp rise in voltage occurs, developing the leading edge of the control pulse. Silicon-controlled switch CR1328 remains

on until silicon-controlled switch CR1326 is gated on.

o. The positive pulse from Q1317 is also coupled to ramp generator Q1318. A positive linear ramp voltage is produced at the emitter of Q1318.

p. Normally, at the Schmitt trigger, Q1320 is conducting, while Q1319 is held cut off. The positive linear ramp voltage from Q1318 is applied to Q1319 and overcomes the bias level, permitting conduction of Q1319. The negative pulse developed at the collector of Q1319 is coupled to the base of Q1320, cutting Q1320 off. The output of the Schmitt trigger at the collector of Q1320 is a positive pulse. The positive pulse from Q1320 is applied to emitter follower Q1321. The output from Q1321 is a positive pulse applied to the gate of the silicon controlled switch generator at CR1326 (OFF). When CR1326 is gated on, CR1328 is gated off, developing the lagging edge of the control pulse. The control pulse is coupled through transformer T1303 to diplexer Z1201 on the main chassis of the MD-638/TPX-41.

q. Diplexer Z1201 receives the train of three RF pulses, consisting of the coded pulse pair and the P2 pulse provided by the transmitting system. The RF bias *(r* below) and control pulse are connected to the low frequency section of diplexer Z1201. The combined output from Z1201 is routed out of the MD-638/TPX-41 and applied to the RF switch in the antenna system. Diplexer Z1201 controls the sum and difference transmission for the isls function required during normal operation of the antenna system.

r. The interlock circuit consists of transistors Q1313 through Q1315, and part of interlock relay K1301. The RF switch used in the antenna system must be in either the sum or difference condition during RF transmission. The control pulse section provides a dc path for bias current to the RF switch in the antenna system (p above). During the time that the control pulse is present, a bias current is available which ensures that Q1314 is turned on. With Q1314 conducting, Q1315 is turned on, allowing Q1313 to conduct. When Q1313 conducts, interlock relay K1301 becomes energized, permitting original signal distribution (c above). If any interruption occurs, the forward bias for Q1313 deenergizes; thus, until the trouble has been removed, all systems will return to a quiescent state.

2-5. Transmitting System Functioning

a. General. The transmitting system is activated by the coded pulse pair and P2 pulse received from the isls system. In response to these input pulses, the transmitting system produces high-power RF pulses which bear the same spacing characteristics as the coded pulse and P2 pulse. The primary components of the transmitting system are contained in Receiver-Transmitter, Radio RT-264D/UPX-6, which also houses the receiving system. The principle circuits of the transmitting system include a modulator group that develops high-voltage pulses, a direct crystal-controlled exciter that generates an RF signal, and a series of cavity units that develop the RF power required for transmission. System operation of the transmitting system is described in *b* through *h* below. A block diagram of the transmitting system is shown in figure 2-9.

b. Modulator Circuits. The modulator circuits consist of trigger input amplifier and blocking oscillator V109, modulator driver V108, and modulator V107. The coded pulse pair from the isls system is transformer-coupled to trigger input amplifier V109B and an auxiliary trigger amplifier in the receiving system. The output of the auxiliary trigger stage is used to activate gtc circuits in the receiving system. The pulses applied to trigger input amplifier V109B are amplified and applied to blocking oscillator V109A which produces 1-,isec pulses at its output. These 1-,sec pulses are applied to modulator driver V108 for further amplification. The amplified output pulses from modulator driver V108 are coupled to the input of modulator V107 where the P2 pulse from the isls system is also supplied. The resultant output of modulator V107 is three high voltage pulses representing the coded pulse pair and the P2 pulse. These pulses are coupled across a tapped transformer output to provide pulse trains of various voltage levels. One winding of the output transformer provides +2100 volta pulses to excite tripler V205 and first amplifier V206. The same winding is tapped for +500-volt pulses which excite tripler V203 and buffer amplifier V204 in the exciter group. Another winding of the transformer provides +3500 volt pulses to excite final amplifier V207. The 500-, 2100-, and 3500-volt pulses occur simultaneously and are 1 usec in duration.

c. Exciter Circuits. The exciter circuits provide RF pulses at a controlled frequency for application

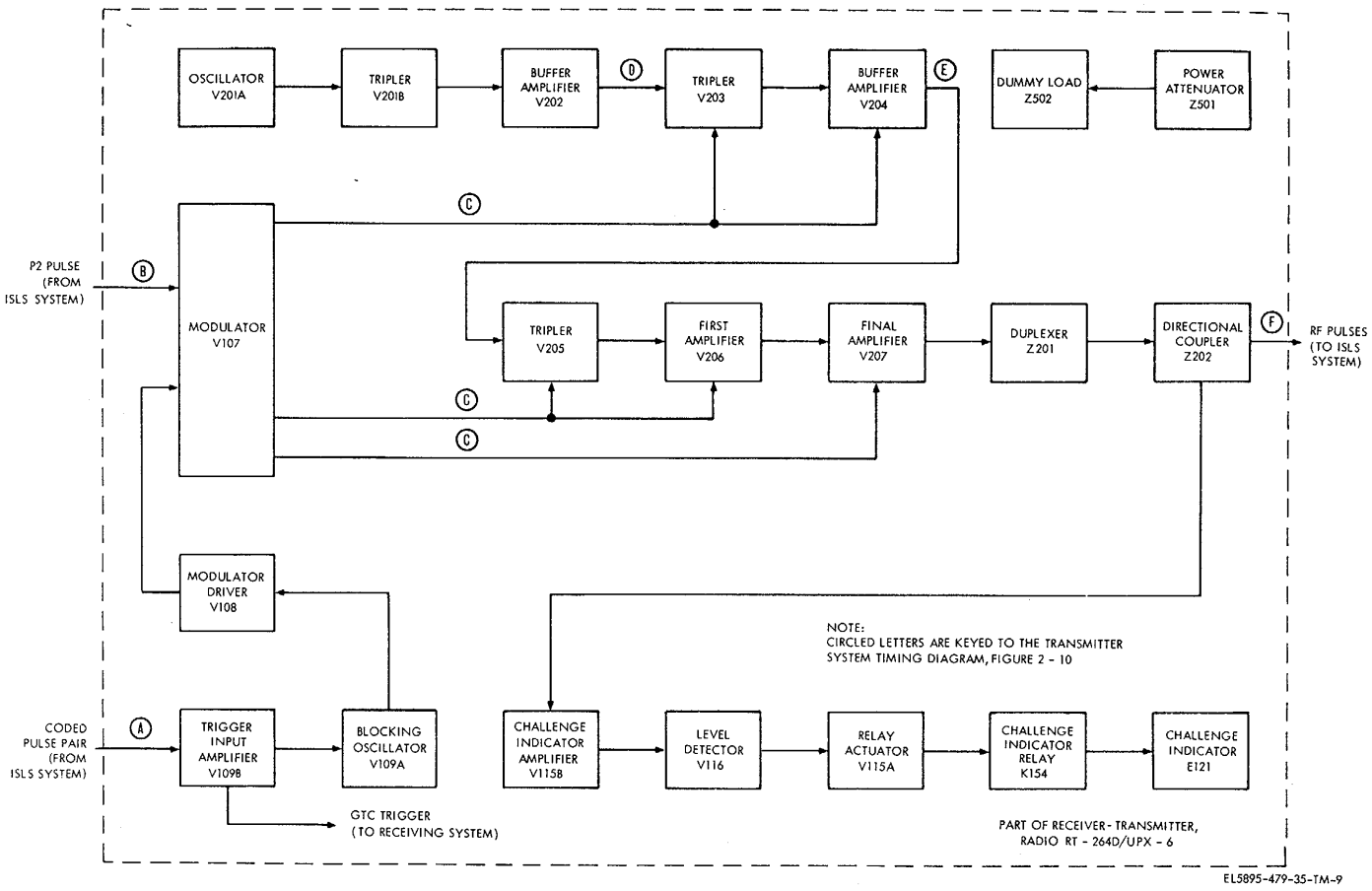


Figure 2-9. Transmitting system, block diagram.

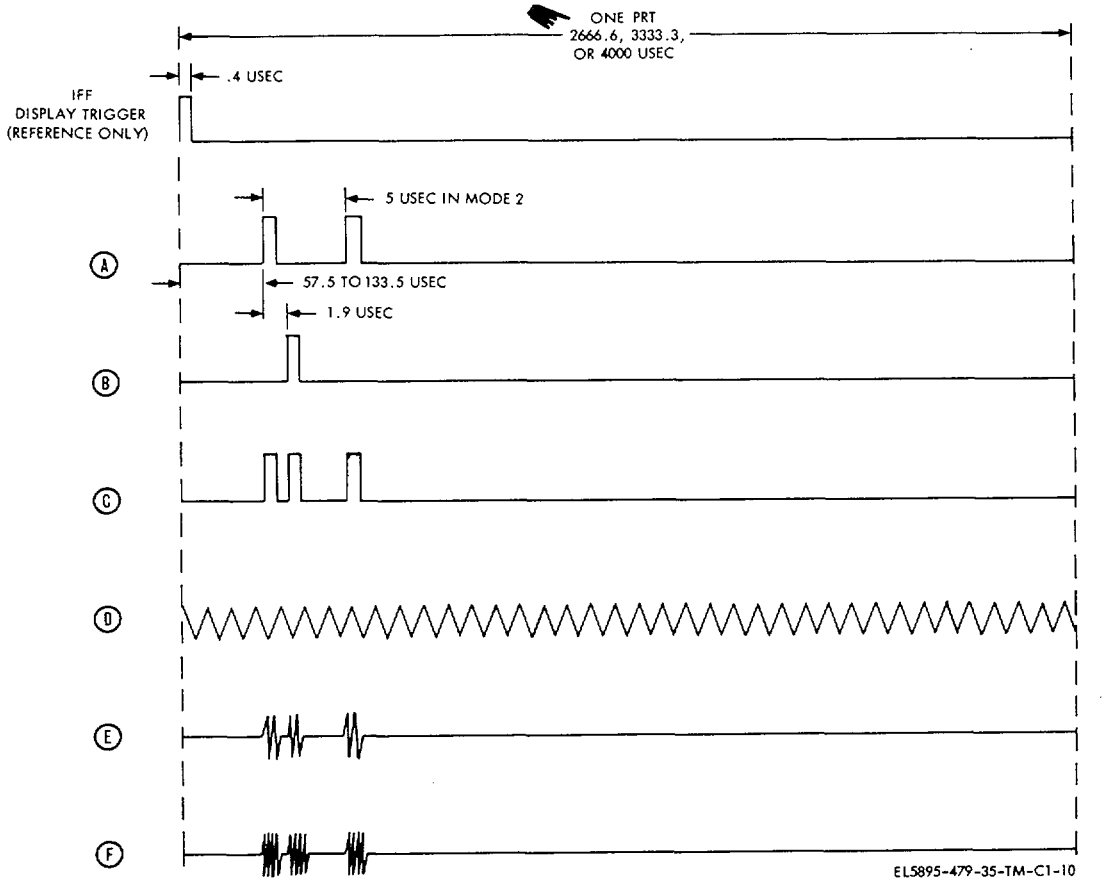


Figure 2-10. Transmitting system, timing diagram.

to the coaxial cavity stages. Crystal-controlled oscillator V201A produces a radio frequency signal, the third harmonic of which is amplified by first tripler V201B. The output of V201B is fed to buffer amplifier V202 for further amplification and application to tripler V203. Tripler V203 amplifies the third harmonic of its input signal providing a frequency nine times that of the original crystal frequency at its output. This output is amplified by buffer amplifier V204 and fed to tripler V205 of the coaxial cavity group.

d. Coaxial Cavity Circuits. The final pulsed output of the transmitting system is developed by three coaxial cavity stages consisting of tripler V205, first amplifier V206, and final amplifier V207. These stages are connected by lengths of coaxial transmission line which are cut to provide tuned coaxial cavities at a specific operating frequency. Tripler V205 receives the RF output of buffer amplifier V204 and amplifies the third harmonic of the signal to provide an RF output with a frequency 27 times that of the original crystal frequency. The output of tripler V205 is coupled to first amplifier V206 where it is amplified and fed to final amplifier V207. Final amplifier V207 produces the final high-power RF output pulses required for transmission. These RF pulses are fed through duplexer Z201, routed out of the RT-264D/UPX-6 and applied to the isls system.

e. Duplexer. Duplexer Z201 provides a means of transmitting and receiving from a common antenna. The duplexer serves as a radio frequency switch which permits transmission of high-power RF signals without damage to the receiving system and reception of low-power received signals without dissipation across the transmitter output stage.

f. Directional Coupler. Directional coupler Z202 provides RF coupling to allow extraction of RF energy for" measuring transmitter power or insertion of RF energy to evaluate receiver system performance. One probe of the directional coupler provides a sample of transmitter output power for application to the challenge indicator circuits.

g. Challenge Indicator Circuits. The challenge indicator circuits monitor the transmitter power output and provide a visual indication if this output is a pulse pair of the proper minimum RF power requirements. Negative pulses, proportional to the transmitter output, are received from the directional coupler in the RF system and are amplified by challenge indicator amplifier V115B. The amplified positive pulses from V115B are then applied to the input network in the grid circuit of level detector V116. If both pulses of the trigger pair are present and of sufficient amplitude, the network will deliver a positive voltage great enough to overcome the bias of the tube, and cause it to fire. The resultant sequence of events will energize the coil of challenge indicator relay K154 in the plate circuit V115A. The relay contacts then will complete the circuit between a 6.3-volt winding on T101 and CHALLENGE indicator lamp E121. When this occurs, the challenge indicator lights, indicating that the transmitter power is of sufficient level.

h. Power Attenuator and Dummy Load. Power attenuator Z501 and dummy load Z502, mounted on the front panel of the RT-264D/UPX-6, permit operation of the equipment while making tests or adjustments without causing interference by radiation of transmitter signals. The dummy load can be connected to the transmitter output, serving as a replacement for the isls and antenna system. The power attenuator may be connected in series with the transmitter output to reduce side lobing effects caused by the antenna in certain installations.

2-6. Antenna System Functioning

a. General. The antenna system provides directional beam propagation of coded RF pulses and reception of IFF replies from airborne transponders. The antenna system is comprised of Pedestal, Antenna AB-1158/GPA-119 and Antenna AS-1796/GPA-119 which together comprise Antenna Group AN/GPA-119. Pedestal, Antenna AB-1158/GPA-119 supports and rotates Antenna AS-1796/GPA-119 while providing rotary coupling to permit transfer of RF energy and control data from the isls system to the rotating antenna. As the antenna is rotated, antenna position synchro data is generated within the AB-1158/GPA-119 and routed to the indicator of the associated radar set. This insures that the IFF sweep on the associated radar indicator is synchronized with IFF antenna rotation. Antenna AS-1796/GPA-119 contains the circuitry and radiating elements necessary for propagation of RF pulses incorporated with the isls feature. System operation of the antenna system is described in *b* and c below. A block diagram of the antenna system is shown in figure 2-11.

b. Pedestal, Antenna AB-1158/GPA119. Antenna drive motor voltage from the power distribution system is applied to antenna drive motor B20002 in the AB-1158/GPA-119. Upon application of the drive voltage, antenna drive motor B20002 rotational drive is coupled through a reduction gear train assembly to turn Antenna AS-1796/GPA-119 at a constant rate of 15 rpm. The input shaft to synchro transmitter B20001 is mechanically coupled to the antenna drive train and rotated synchronously with the antenna; this causes the synchro transmitter to produce an ac error voltage directly proportional to antenna position. The error voltage is routed out of the AB-1158/GPA-119 as antenna position synchro data and applied to the indicator of the associated radar set to establish synchronization between the IFF sweep on the indicator and antenna rotation. Rotary joint E20001 in the AB-1158/GPA-119 couples RF pulses, a control pulse, and dc bias from the isls system to the AS-1796/GPA-119. The rotary joints also transfer received signals from the AS-1796/GPA-119 to a stationary connector on the AB-1158/GPA-119 for application to the isls system.

c. Antenna AS--1796/GPA-119. IFF antenna E1001 is a vertically polarized, longitudinal shunt, slot array. It is constructed from a section of waveguide approximately 10 feet long and divided in the center to form two radiating elements. When the two elements are excited in phase, a radiation pattern equivalent to a normal directional antenna is produced. This pattern is called the sum pattern. When the two elements are excited 180 degrees out-of-phase with respect to each other, an omnidirectional pattern is produced. The omnidirectional (difference) pattern is characterized by a deep null along the centerline of the main lobe of the sum pattern, and the isls pulse (P2) is transmitted on this pattern. RF switch S1001 controls the input ports (sum or difference) of bar hybrid HY1001 into which the RF energy enters. The bias control pulse, generated in the isls system, initiates this action in S1001. The control pulse appears between the coded pulse pair

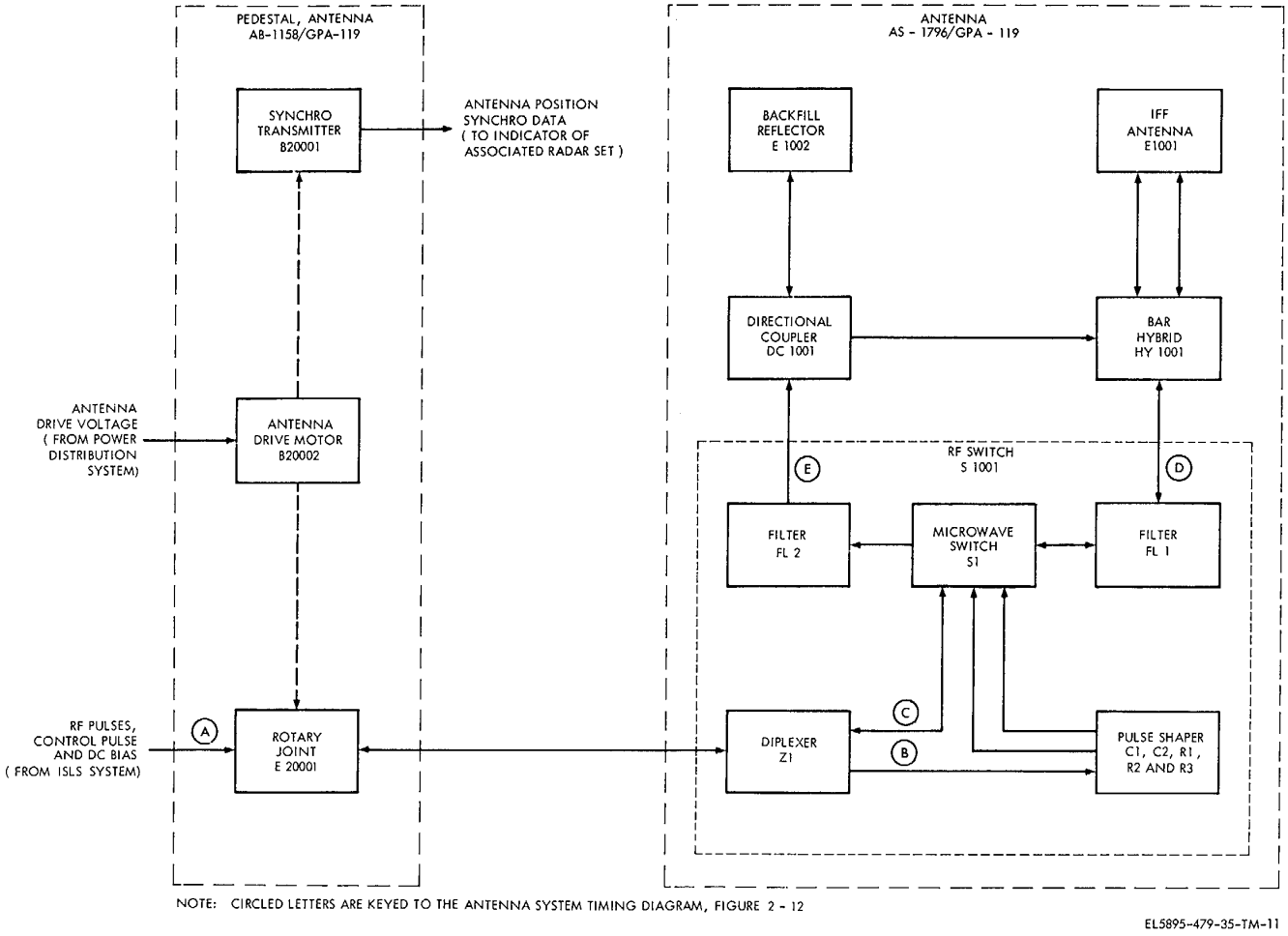


Figure 2-11. Antenna system, block diagram.

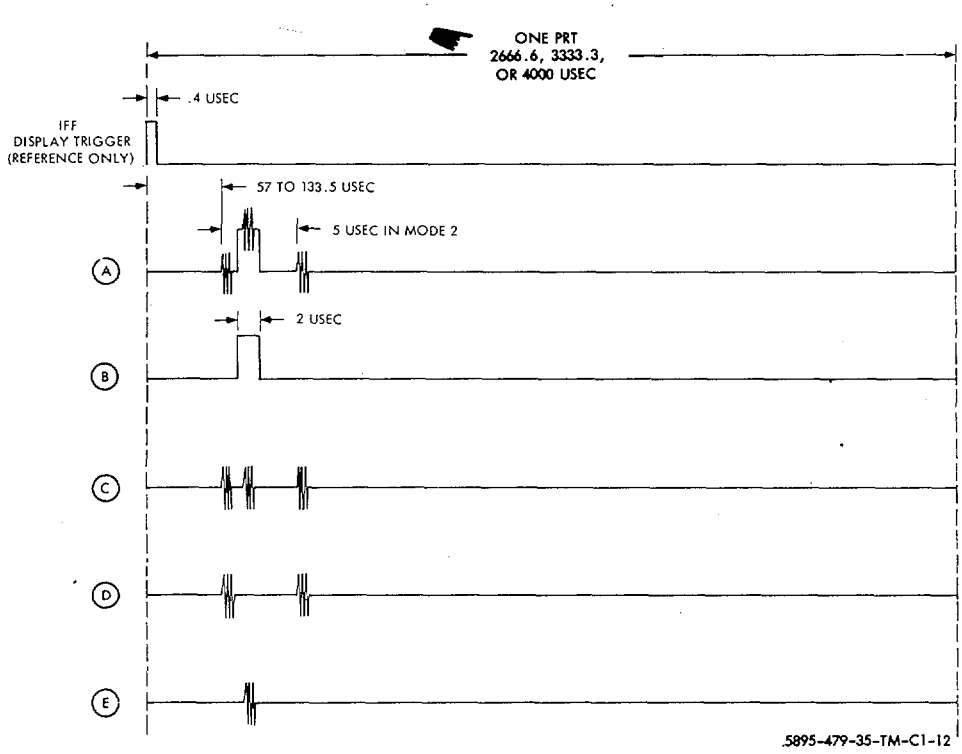


Figure 2-12. Antenna system, timing diagram.

generated by the coding system and brackets the P2 pulse. The RF and bias control pulse are combined in the isls system and separated in RF switch S1001 by diplexer Z1. The bias control pulse is connected to microwave switch S1 through pulse-shaping network resistors R1 through R3 and capacitors C1 and C2, which are located in RF switch S1001. During the time the control pulse is present, RF switch S1001 is biased to route the P2 RF pulse to the difference port of HY1001. When the control pulse is not present, the dc bias routes the RF energy to the sum port of bar hybrid HY1001. Filters FL1 and FL2 provide protection to microwave switch S1 from nearby high-powered radar sets. During nontransmitting periods, RF switch S1001 maintains continuity of the sum channel so return signals can be received. Bar hybrid HY1001 determines the phase in which the two elements of the AS-1796/GPA-119 are excited. Energy entering bar hybrid HY1001 through arm No. 1 (referred to as the sum port) will excite the two elements in phase; energy entering bar hybrid HY1001 through arm No. 4 (referred to as the difference port) will excite the elements 180 degrees out-of-phase. Directional coupler DC1001 is inserted in the difference pattern channel between RF switch S1001 and bar hybrid HY1001. Directional coupler DC1001 feeds a portion of the transmitted difference signal (P2 pulse), attenuated approximately 6 db, to backfill reflector E1002. Backfill reflector E1002 provides difference pattern RF energy in the rear hemisphere of IFF antenna E1001 to cover the back and side lobe energy radiated during the sum pattern from IFF antenna E1001.

2-7. Receiving System Functioning

a. General. The receiving system accepts a coded RF pulse train from the isls system and provides frequency conversion, detection, and amplification to produce a low-noise video representation of the received coded pulse train. The receiving system is contained in Receiver-Transmitter, Radio RT-264D/UPX-6, which also houses the transmitting system discussed in paragraph 2-5. The principle circuits of the receiving system include a direct crystal-controlled oscillator, a preselector assembly for image rejection, a crystal mixer, a 60-MHz IF amplifier which incorporates antijamming circuits, and a gate and gain time control (gtc) circuit which may be set to vary the receiver gain for distant or nearby targets. The reception time of the receiving system is established by the same coded pulse pair that triggers the transmitting system, thus providing for reception only during the time that the transmitting system is transmitting challenge signals. System operation of the receiving system is described in *b* through f below. A block diagram of the receiving system is shown in figure 2-13.

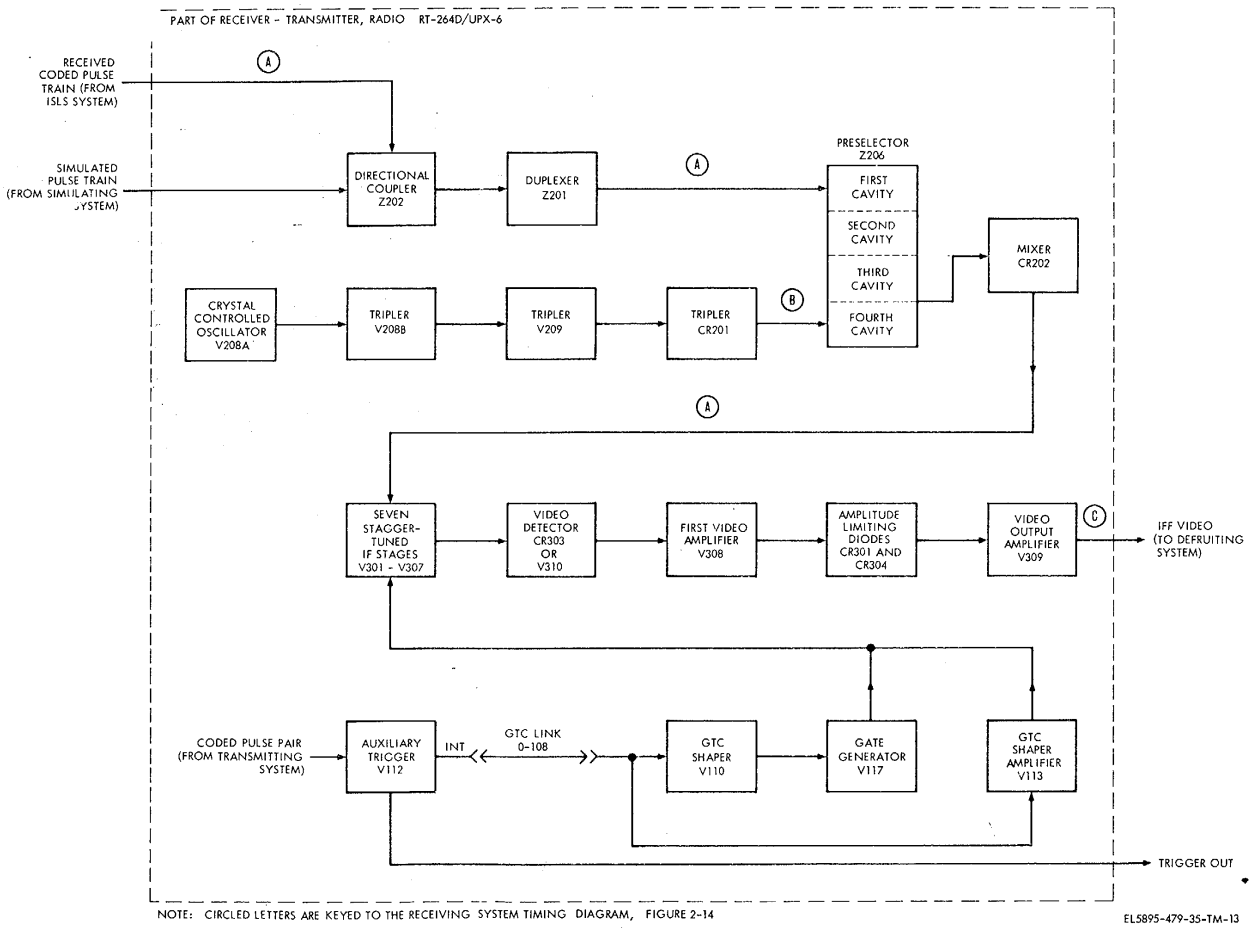


Figure 2-13. Receiving system, block diagram.

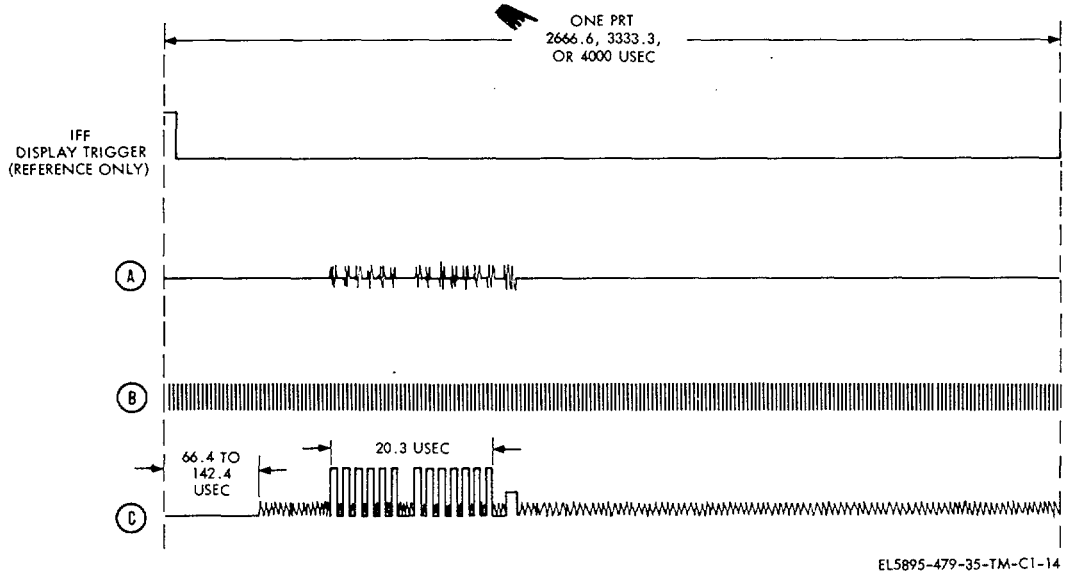


Figure 2-14. Receiving system, timing diagram.

b. Preselector. Coded RF pulse trains, coupled through the isls system are applied to the receiving system at directional coupler Z202. The RF pulses are fed through the directional coupler and applied to duplexer Z201 which routes the RF pulses directly to preselector assembly Z206. Preselector Z206 consists of four tuned cavity units. The first, second, and third cavities can be tuned to pass received signals within a frequency range of 1080 to 1130 MHz. Desired signals pass through the first three cavities with little attenuation while signals other than those of the desired frequency are attenuated greatly. Selective tuning by this method insures that only those IFF replies transmitted at the proper frequency appear at the output of the third cavity.

c. Oscillator-Multiplier and Mixer Circuits. The oscillator-multiplier circuit consists of crystal-controlled oscillator V208A, tripler V208B, tripler V209, and tripler CR201. Crystal-controlled oscillator V208A produces a stable crystal-controlled frequency which is applied to tripler V208B. This tripler stage is tuned to amplify the third harmonic of the crystal frequency which results in an output signal with a frequency three times that of the original crystal frequency. The signal is coupled to a second tripler stage V209 which also produces an output signal with a frequency three times that of its input. The resulting input to tripler CR201 is a signal with a frequency nine times that of the original crystal frequency. The fourth cavity of the preselector assembly, described in *b* above, functions as the tuned output circuit for CR201, and is tuned to the third harmonic of the input signal applied to CR201. The tuned output circuit is sufficiently selective to accept the third harmonic and reject all other harmonics. The resulting fourth cavity oscillations produce a signal frequency 27 times that of the original crystal frequency within a range of 1200 to 1250 MHz (dependent upon receiver crystal used). This signal, and the received signal present in the third cavity of the preselector, are coupled to mixer CR202. The mixer accepts the two input signals and produces a 60-MHz intermediate frequency (IF) resulting from the difference of the two input frequencies. All other modulation products, including the two injected frequencies, are greatly attenuated.

d. IF Amplifier and Video Circuits. The IF amplifier and video circuitry is comprised of seven stagger-tuned IF stages V301 through V307, a video detector CR303 or V310, first video amplifier V308, a limiting network, and video output amplifier V309. IFF signals received from mixer CR202 are amplified by the seven stages of IF amplifiers V301 through V307 and applied to video detector CR303 or V310. Detection at this stage is normally accomplished by diode CR303 for broadband operation. Narrow band operation is achieved by substituting tube V310 for diode CR303. The detected signal is applied to first video amplifier V308 where the first stage of IFF video amplification takes place. The output of V308 is

limited by CR301 and CR302 and applied to video output amplifier V309 for further amplification. The output of V309 is routed out of the receiving system and applied to the defruiting system as IFF video.

e. Gtc and Gate Circuits. The gtc and gate circuit places the negative (quiescent) bias on the grids of the second and fourth IF amplifiers sufficient to hold them at cutoff until the initiating trigger pulse is received from the transmitting system. This bias then is replaced during the reception period (gate interval) by a controlled gtc bias (a negative voltage that changes with respect to time). The need for the variable bias system arises from the fact that reply signals from distant aircraft are much weaker than those originating from nearby aircraft. Considerably more IF gain is required to make the weaker signals intelligible; however, if the receiver gain is adjusted sufficiently high for distant signals, strong signals from nearby sources will cause serious overloading with the IF section of the receiver. The objective of the gtc circuits, during the gate interval (the period during which the cutoff bias is removed), is to vary the receiver gain so that the distant signals can be amplified sufficiently to be used for identification without overloading the receiver with strong signals from relatively close aircraft. Auxiliary trigger tube V112 receives coded pulse pairs from the transmitting system and produces a trigger pulse in each pulse pair. One trigger output of V112 is routed out of the receiving system to provide an external trigger for testing purposes. The other trigger output from V112 is applied to gtc shaper V110 and gate generator V113. Gate generator V113 is a monostable multivibrator, which in its untriggered condition, applies a negative bias gate to the second and third IF stages holding them at cutoff. When gate generator V110 is triggered by the output of V112, the cutoff gate is removed. Simultaneously, gtc shaper, which is also triggered by the output of V112, produces a positive going voltage which is inverted, shaped, and amplified by gtc shaper amplifier V117. The resulting negative-going voltage at the output of V117 is applied to the second and fourth IF amplifier stages to replace the cutoff bias from V113 and accomplish gtc action.

f. Simulated Signal Injection. A simulated pulse train from the simulating system may be applied to the receiving system for t-sting purposes when actual aircraft replies cannot be obtained. The simulated pulse trains are applied to the receiving system at directional coupler Z202. The receiving system processes the simulated pulse trains in the same manner as actual pulse trains and produces IFF video at its output. Through applied troubleshooting and testing techniques, the absence or presence of this video at various points throughout the IFF system may be used to analyze the performance of the coding, receiving, defruiting and transmitting systems.

2-8. Defruiting System Functioning

a. The defruiting system accepts incoming IFF video from the receiving system and by process of comparison, eliminates nonsynchronous signals. The system is essentially comprised of coincidence and video amplifying circuits on the processor (chassis series No. 30800) which is contained in the Blanker, Interference MX-8795/TPX-41. Delay line DL31101, also a part of the MX-8795/TPX-41 and defruiting system, provides the delay necessary to accomplish video and trigger comparison from one pulse period to the next. Trigger and gating signals essential for synchronous operation of the defruiting system are provided by the timing system, discussed in paragraph 2-2, which is also contained in the MX-8795/TPX-41. System operation of the defruiting system is described in *b* through *j* below. A block diagram of the defruiting system is shown in figure 2-15.

b. The IFF video input from the receiving system is applied to threshold limiter Q1 and emitter follower Q8. The limiting action of Q1 removes most of the noise from the video train. The positive output of Q1 is dc-coupled to quantizer Q2. The output of Q2 is amplified to a limiting level to provide a positive video train of equal pulse amplitude. The positive output of Q2 is coupled to inverter Q3. The negative output of Q3 is coupled to Q4 at logic AND gate Q4 and Q17.

c. The IFF input enable gate from the timing system (para *3-2b)* is also dc-coupled to Q17 of the logic AND gate. If both signals are present at the logic AND gate at the same time, the output of Q4 is inverted, and direct-coupled to Q5 at logic OR gate Q5 and Q6. The output from Q5 is a series of negative pulses.

d. The positive circulating pretrigger from the timing system is dc-coupled to the logic OR gate at

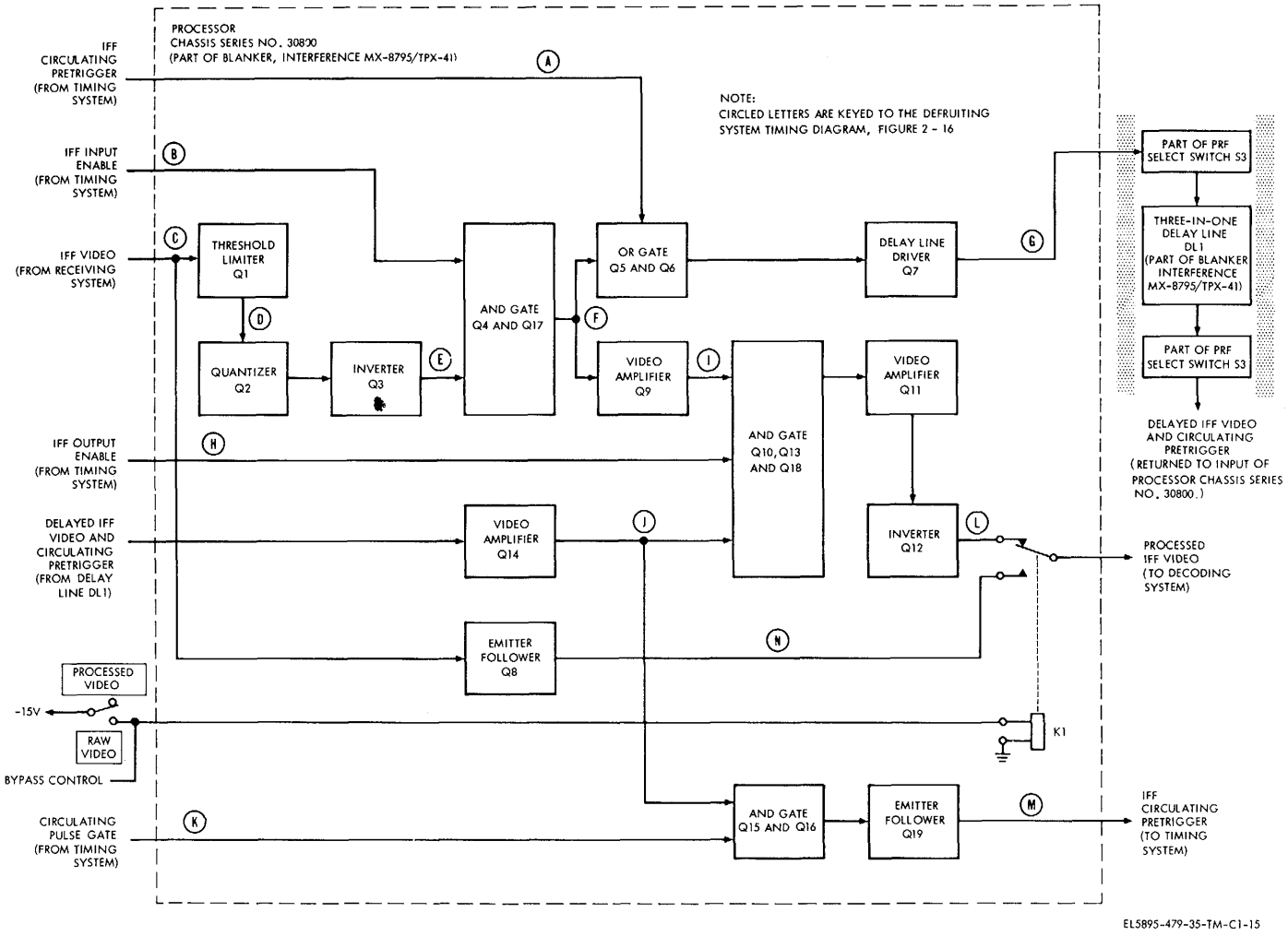


Figure 2-15. Defruiting system, block diagram.

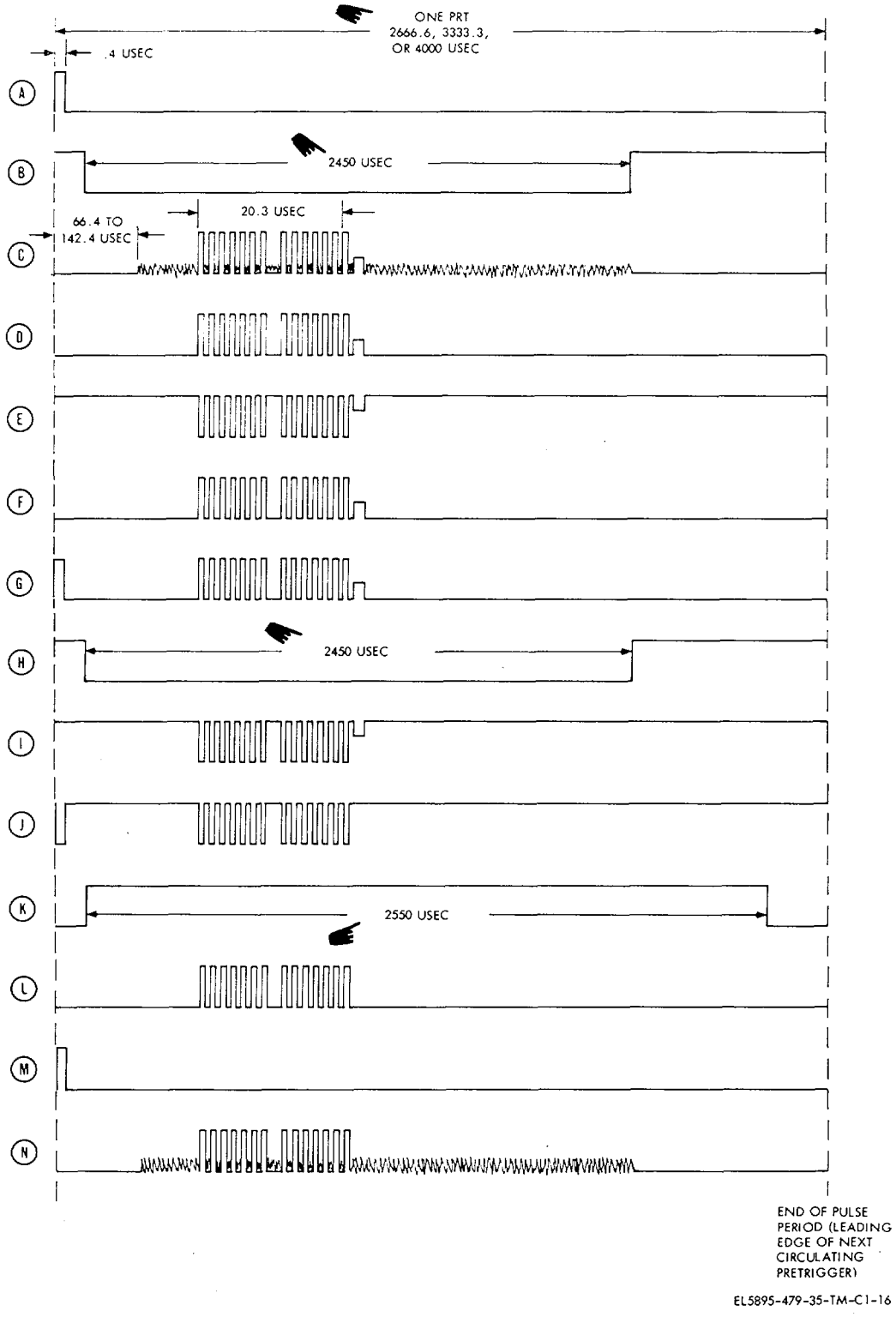


Figure 2-16. Defruiting system, timing diagram.

Q6. The circulating pretrigger is present at Q6 before the video train is available from the logic AND gate at Q5. Any positive input to the logic OR gate will produce a negative pulse output which is coupled to delay line driver Q7.

e. The negative output of the logic OR gate is inverted through Q7. The positive output of Q7, consisting of one video pulse train preceded by the circulating pretrigger, is coupled through PRF SEL switch S3 to DLI. PRF SEL switch S3 is connected to both the input and output terminals of delay line DLI. The setting of S3 determines which one of three delay lines, contained within DLI, will be used to establish the system prf. Position I of the switch provides a 2666.6gsec delay and a prf of 375 pps. Position 2 of the switch provides a 3333.3Iksec delay and prf of 300 pps. Position 3 of the switch provides a 4000-g, sec delay and a prf of 250 pps.

f. The positive output from DLI is delayed one interpulse period (2666.6, 3333.3, or 4000 usec). The delayed positive output of DLI is coupled through S3 to the input of the processor (chassis series No. 30800) and applied to video amplifier Q14.

g. At the end of the 2666.6-, 3333.3-, or 4000, sec delay, video from the next pulse period is present in the positive output of logic AND gate Q4 and Q 17. Video amplifier Q9 inverts the input from the AND gate and the negative pulses are then coupled to logic AND gate Q10, Q13, and Q18.

h. The positive IFF output enable gate from the timing system begins approximately 1.5 μsec after the circulating pulse, due to action of delay line DL30901 in the timing system, and is coupled to logic AND gate Q10, Q13, and Q18.

i. The delayed IFF video coupled to video amplifier Q14 is inverted, and coupled to logic AND gate Q13. Coincident pulses from the delayed and undelayed video will permit a positive train to be coupled to video amplifier Q11. Nonsynchronous pulses do not permit operation of the logic AND gate, and are eliminated from the video train.

j. The video train, inverted by video amplifier Q11 and inverter Q12, appears as processed positive pulses at terminal 1 of bypass relay K1. Positive raw IFF video input is coupled to emitter follower Q8. The positive raw video pulses are directly connected to terminal 5 of K 1. If defruiting is not desired; raw IFF video can be selected by placing PROCESSED VIDEO-RAW VIDEO switch S31102 to RAW VIDEO, which permits the bypass control voltage to energize K1. The output of K 1I is routed out of the defruiting system and the MX-8795/TPX-41 and applied to associated remoting equipment for routing to the decoding system as IFF video.

k. The circuits that produce the circulating pretrigger to the timing system consist of logic AND gate QS5 and Q16, and emitter follower Q 19.

The negative portion of the positive circulating pulse gate is dc-coupled to Q16. The positive delayed circulating pulse is inverted by Q14. The negative pulse from Q14 is coupled to Q15. An output from the logic AND gate is possible only during coincidence of the delayed circulating pretrigger and the negative portion of the circulating pulse gate. Output from the logic AND gate ceases during the positive portion of the circulating pulse gate, and delayed IFF video is not passed. The positive output from the logic AND gate is directly connected to emitter follower Q19. The positive circulating pulse output of Q 19 is routed out of the defruiting system and applied to the timing system to initiate the trigger for the next pulse period.

2-9. Decoding System Functioning

a. General. The decoding system electronically analyzes IFF video pulse trains from the defruiting system and produces decoded video to represent various types of aircraft identification. The principle circuits of the decoding system are contained in Decoder, Video KY-593/TPX-44. These circuits include pulse train amplifying and shaping circuits that amplify and shape the video pulse trains from the defruiting system, code selecting and pulse train analyzing circuits that establish codes and produce outputs in response to IFF replies which correspond to the selected codes, reply generating circuits that generate signals necessary for distinction between the various types of identification video, identification-of-position circuits that produce identification-of-position video, and emergency and bracket video circuits that produce emergency and bracket video. The primary control functions of the decoding systems are on Control, Remote Switching C-7014/TPX44 which is directly connected to the KY593/ TPX-44. System operation of the decoding system is described in *b* through e below. A block diagram of the decoding system is shown in figure FO-2.

b. Pulse Train Amplifying and Shaping Circuits. The input to Decoder,VideoKY593/ TPX-44 is a train of positive video pulses from the defruiting system. The video pulse train applied to inverter amplifier Q30001 is amplified and inverted. The output of Q30001, a train of negative pulses, is applied to amplifier Q30002 where it is shaped, amplified, and inverted. The

output of Q30002, a train of positive pulses, is applied at a low impedance level to delay line DL201 on the main chassis. To compensate for attenuation of pulses in DL201, a tap near the center of the line delivers these pulses to another amplifying and shaping network. This network consists of inverter amplifier Q30003 and amplifier Q30004. The output of Q30004. a train of positive video pulses. is reintroduced into the delay line. When the pulses in the video pulse train are deployed along DL201 so that each pulse is coincident with the tap associated with its characteristic spacing. a time coincident series of pulses. comprised of all the pulses in the pulse train, is applied to the diode matrix in the code selecting and pulse train analyzing circuits, described in c below.

c. Code Select and Pulse Train Analyzing Circuits.

(1) Video delay line DL201 and associated diode matrix CR205 through CR234 comprise the heart of the decoding system. The coded video pulse train is delayed in DL201 in accordance with the time spacing between pulses or pulse slots. The instant that the first bracket pulse reaches the termination of DL201, the remaining pulses are deployed along DL201 until each is coincident with the tap associated with its characteristic spacing. The output taps on DL201 are spaced at the same time interval as the spacing of the time slots in the coded pulse train.

(2) The preselected code setting is established at Control, Remote Switching C-7014/TPX-44.

When the code switch for the mode of operation being used corresponds to the makeup of the coded video pulse train along DL201, the diode matrix permits a single voltage pulse (code correct) to be developed for input to clipper amplifier Q30111 on the coincidence amplifier subassembly. Each section of the matrix routes the pulse from a tap on DL201, either to a coincidence line (code correct) or to kill line (incorrect I or incorrect 2/ 3) depending on the setting of the code select switches. Coincidence requires that all selected pulses be present at their respective output points from DL201 at the same time; therefore, this condition indicates that no coincident signal is present, and no signal on the code correct line is available until both bracket and code pulses are present in their respective matrix inputs. When a pulse appears in a time slot which is not selected in the code, a kill pulse (incorrect signal) will inhibit the coincidence (code correct signal). The diode matrix (CR205 through CR234) that is connected to the terminals of DL201 determines when the code is correct. *For example.* if the pulse train from the defruiting system consists of more pulses than required to satisfv the preselected code setting. diode matrix CR205 through CR234 will also permit a voltage pulse to be developed on one of the kill bus lines and to be delivered as a kill pulse to emitter followers Q30113 (incorrect 1) or Q30114 (incorrect 2 / 3) on the coincidence amplifier subassembly. If the coded input train consists of fewer pulses required to satisfy the preselected code setting. diode matrix CR205 through CR234 will not permit a voltage pulse (code correct) of sufficient amplitude to be developed on the coincidence bus.

(3) When a code correct pulse (coincidence) is delivered to clipper amplifier Q3011 1, it is amplified, inverted, and coupled to inverter amplifier Q30112. The signal is amplified and inverted by Q30112 and routed to shaper amplifiers Q30101 and Q30102. At this time. the pulse is shaped (to restore its necessary square wave characteristics), amplified. inverted, and coupled to gate amplifier Q30103 in logic AND gate Q30103, Q30106, and Q30109 as a negative pulse.

(4) If a kill pulse was not developed, gate amplifier Q30106 and Q30109 in the logic AND gate are cut off and Q30103 is conducting. The negative pulse at the input of Q30103 causes it to cut off, and the logic AND gate output is a positive pulse which is coupled as decoded video to gate amplifier Q30301 and CR30101.

(5) If a kill pulse was coupled to either emitter follower Q30113 orQ301 14, the pulse is shaped by Q30104 and Q30105, or Q3010-7 and Q30108. The shaped pulse causes Q30106 or Q30109 in the logic AND gate to conduct. If either of these transistors is conducting, the code correct pulse at the input of Q30103 will not appear at the output of the logic AND gate.

d. Reply Generating Circuits.

(1) The code correct (coincidence) line from diode matrix CR205 through CR234 carries one

pulse when there is a pulse present in each pulse slot selected by code selector switches S40301, S40302, and S40303 located on Control, Remote Switching C-7014/TPX-44. The single code correct pulse is the output of the logic AND diodes of diode matrix CR205 through CR234. The kill pulses (incorrect 1 or incorrect 2/3) originate at the logic OR circuits of the diode matrix. If a pulse or pulses of the incoming pulse train is present at a pulse slot where no pulse is expected, a kill pulse (incorrect 1 or incorrect 2/3) is generated on the incorrect pulse lines at these taps on delay line DL201. But when code 7777 is selected, no pulses can be generated on either of the incorrect lines because all taps on DL201 have been selected for use. Any other selected code can produce pulses on the incorrect lines. *For example,* when the selected code is 7763, all taps on DL201 are used except taps C1 and D4; therefore, the entire pulse train (12 pulses) is present at each of the logic OR diodes, except CR206 and CR229. If the airborne transponder sends a code train on 7777, a kill pulse occurs on the incorrect lines from logic OR gate CR256 and CR229 at the same instant as coincidence of the code-correct pulse occurs. A kill pulse generated at DL201 will not permit production of a decoded video pulse at the output of the logic AND gate at the coincidence amplifier subassembly. The coincidence amplifier subassembly produces a decoded video pulse only when

(a) There *is* a code-correct pulse input.

(b) There *is not* an incorrect 1-pulse input.

(c) There *is not* an incorrect 2/3-pulse input.

(2) The logic AND gate amplifiers Q30103, Q30106, and Q30109 at the output of the coincidence amplifier subassembly conduct through the same collector resistor, and they must be turned off at the same time to produce a positive output signal. When an output from the logic AND gate is obtained, the positive decoded video pulse from the coincidence amplifier subassembly is coupled to gate amplifier Q30301 at the video mixer subassembly. Gate amplifier Q30301 is part of logic OR gate Q30301, Q30308, and Q30309. Gate amplifier Q30301 inverts the positive decoded video pulse; the negative pulse, developed at a common collector resistor, triggers 1-psec multivibrator Q30311 and Q30312, and 10-#usec multivibrator Q30302 and Q30303. In the bracket function, multivibrator Q30311 and Q30312 can also be triggered by gate amplifier Q30310. When BEACON ASSIST switch S40306 on the C-7014/TPX-44 is used, decoded IFF video is a 10-, sec pulse, except for incorrectly coded replies when the bracket function has been selected by BRACKET-OFF switch S40305 on the C-7014/TPX-44. The positive output of either the 1or 10-, sec multivibrator is coupled by gate drivers Q30305 and Q30313 to a logic OR gate consisting of gate diodes CR30305 and CR30309. The positive signal developed across the logic OR gate load resistor is applied to operate-test relay K201.

(3) When OPERATE-TEST switch S40307 on the C-7014/TPX-44 is placed to OPERATE, relay K201 on the main chassis of the KY-593/TPX-44 is not energized. The positive IFF video pulse is connected through K201 to line drivers Q30306 and Q30307. The output of Q30306 and Q30307 is connected to the associated radar set to be displayed on the plan position indicator (ppi).

(4) When OPERATE-TEST switch S40307 on the C-7014/TPX-44 is placed to TEST, relay K201 on the main chassis of the KY-593/TPX-44 is energized. In the test function, K201 connects raw IFF, as selected by UNDLYD-DLYD switch S30001, from emitter follower Q30012 on the video amplifier subassembly to line drivers Q30306 and Q30307, as indicated in (2) above.

e. Identification-of-Position Circuits.

(1) During i/p transmission from the airborne transponder on mode 2 or mode 3, the first pulse displayed on the associated radar indicator is the decoded IFF signal. The decoded IFF signal (normal code train) is also compared for coincidence with the i/p reply pulse to obtain the second pulse and assure positive aircraft identification using the preselected code. The i/p pulse received is located 4.35 , sec after the second bracket pulse. The determination that an i/p pulse is present is made by comparison of undelayed raw IFF video with decoded video. If an i/p pulse is present, it occurs at the same instant in the undelayed video train as the decoded video pulse is produced at the output of the coincidence amplifier subassembly (c above). The undelayed video used for comparison is designated i/p video. The i/p video is taken from the collector of amplifier Q30011 at the video

amplifier subassembly. The positive decoded video pulse at the output of logic AND gate Q30103, Q30106, and Q30109, is developed at a common collector load resistor. The positive decoded video pulse is applied to gate diode CR30101 in logic AND gate, CR30101 and CR30102. The i/p video from amplifier Q30011 in the video amplifier subassembly is applied to gate diode CR30102 in the logic AND gate in the coincidence amplifier subassembly. The i/p trigger is produced by logic AND gate CR30101 and CR30102 when i/p video and the decoded video signal are coincident.

(2) The single positive i/p trigger is coupled to the ident-emergency generator subassembly to trigger two delay multivibrators: 24.65-, usec multivibrator Q30202 and Q30203, used to produce the i/p video signal, and 14-psec multivibrator Q30207 and Q30208 used in the emergency circuits. The negative i/p video output of Q30201 triggers delay monostable multivibrator Q30302 and Q30203, which is adjusted for a positive gate deviation of 24.65 , sec. The gate is differentiated at the output of Q30202 and Q30203 and applied to gate amplifier Q30204 in logic AND gate Q30204 and Q30205.

(3) During mode 2 or 3 operation, the input to the logic AND gate at Q30205 is grounded through relay K40305 on Control, Remote Switching C-7014/TPX-44, to keep Q30205 cut off. Gate amplifier Q30204 is conducting and must be cut off to produce a positive decoded i/p video pulse at the output of the logic AND gate. Gate amplifier Q30204 is turned off by the negative trailing edge of the differentiated 24.65-usec gate from Q30202 and Q30203. The output of the logic AND gate is a positive video pulse produced 24.65 Asec after normal IFF video. In mode 1, two coded pulse trains are transmitted by the airborne transponder for an i/p video reply, and both code trains will be decoded to produce two IFF video signals 24.65 usec apart. In mode 1 the output of the logic AND gate is disabled by a mode 1 i/p off input from K40305 to Q30205.

(4) In mode 1 operation, the two decoded video pulses generated from the two pulse trains received are coupled to gate amplifier Q30301. Gate amplifier Q30301 is part of logic OR gate Q30301, Q30308, and Q30309 located on the video mixer subassembly. In mode 2 or 3 operation when a single i/p pulse is transmitted by the transponder, the decoded video pulse from the 2-28 single pulse train received is coupled as the first pulse to Q30301. The positive decoded i/p video pulse from gate amplifier Q30204 on the ident emergency generator subassembly is coupled as the second pulse to logic OR gate amplifier Q30308. Gate amplifier Q30309 is used during emergency operation *(e* below). Negative pulses from logic OR gate Q30301 and Q30308, which are 24.65 usec apart, are developed at a common collector load resistor to trigger 1-, usec multivibrator Q30311 and Q30312, and 10-, sec multivibrator Q30302 and Q30303. Signal distribution of pulses to the associated radar set ppi is discussed in c(2) and (3) above.

f. Emergency and Bracket Video Circuits.

(1) During emergency operation, the airborne transponder sends an emergency reply which consists of a normal code train followed by three sets of bracket pulses. When this reply is decoded, the emergency display consists of four pulses spaced 24.65 usec apart. These four video pulses are provided for display on the associated radar ppi by the KY-593/TPX-44. The first video pulse is produced by decoding the code pulse train through the normal video decoding circuits discussed in b and c above. The second video pulse is produced by the identification-of-position (i/p) circuits described in *d* above. The third and fourth video pulses are produced by the emergency circuits ((2) through (9) below).

(2) The positive i/p trigger is coupled to trigger amplifier Q30201 on the ident-emergency generator subassembly to produce the second video pulse (d(2) above). The i/p trigger is also coupled to an OR gate at trigger amplifier Q30206. The logic OR gate, which consists of trigger amplifier Q30206 and gate amplifier Q30210, is located in the ident-emergency generator subassembly. The negative pulse from Q30206 is coupled to trigger 14-, usec multivibrator Q30207 and Q30208. The positive gate output from this multivibrator is adjustable from a minimum width of approximately 14 usec. The positive gate from the 14-usec multivibrator is partially differentiated by capacitor C30212 and resistor R30230 before being coupled to logic AND gate Q30209, Q30213, and Q30214 located in the ident-emergency generator subassembly. Capacitor C30212 charges rapidly through Q30209, but discharges through R30230 to achieve the required time constants. Conducting gate amplifier Q30209 is not affected by the

leading edge of the differentiated pulse, but is turned off by the trailing edge of the partially differentiated positive gate from the 14-/, sec multivibrator at Q30208, and held off by the discharge of C30212 across R30230 until another cycle is initiated at the 14-, usec multivibrator. This condition ensures that Q30209 is cut off when the emergency video pulse is to be produced ((4) below).

(3) Logic AND gate CR207 and CR233, located within the diode matrix, develops a pulse whenever two bracket pulses (PF1 and PF2) are received. The resulting single bracket video pulse (PF video) from the logic AND gate is amplified by differential amplifier Q30007 and Q30008 and inverter amplifier Q30009 on the video amplifier subassembly. The positive bracket pulse (VB identification) from Q30009 is coupled to amplifier Q30212 on the ident-emergency generator subassembly. The bracket pulse (VB identification) occurs 24.65 psec after the first bracket pulse reply (PF1 and PF2) is received from the airborne transponder and, in the case of an emergency reply, a third and fourth bracket pulse reply (PF1 and PF2) occur after the third and fourth time periods of 24.65 /sec.

(4) To obtain an emergency video output from logic AND gate Q30209, Q30213, and Q30214 located on the ident-emergency generators subassembly, all three transistors must be cut off. Gate amplifier Q30209 is held at cutoff by the discharge of capacitor C30212 previously discussed (para (2) above). Use of the C-7014/TPX-44 EMER-OFF switch S40304 insures that Q30214 remains cut off in the emergency function by application of ground to its base. The positive bracket pulse (VB identification) at the input of amplifier Q30212 ((3) above) is inverted and the negative pulse is applied to the input of gate amplifier Q30213 at the logic AND gate. The negative pulse cuts Q30213 off and, with Q30214 cut off by the EMER-OFF control on the C-7014/TPX-44, and Q30209 cut off ((2) above), a positive emergency video pulse is produced at the output of the logic AND gate.

(5) The positive emergency video pulse is coupled to gate amplifier Q30309 in logic OR gate Q30301, Q30308, and Q30309 on the video mixer subassembly. The positive emergency video is also coupled to a feedback circuit that includes capacitor C30218 and resistor R30239. The feedback circuit places a negative bias at the input of gate amplifier Q30211. The first positive bracket emergency video pulse will arrive at the logic OR gate on the video mixer at Q30309 at the same time as the positive decoded i/p video pulse arrives at Q30308. The presence of these pulses at the OR gate is unimportant at this time, since the positive i/p trigger was originally required to initiate the first cycle of the 14-usec multivibrator located on the ident-emergency generator subassembly.

(6) After the first positive pulse of emergency video has been coupled to the OR gate ((5) above), the negative bias input to gate amplifier Q30211 cuts off Q30211. The positive output pulse of Q30211 is inverted through gate amplifier Q30210 of the logic OR gate. The negative output pulse from Q30210 retriggers the 14-, usec multivibrator before the second set of bracket pulses are processed to arrive at the AND gate ((4) above).

(7) The second set of bracket pulses (PF1 and PF2) are processed and arrives at Q30213 ((3) and (4) above). With Q30214 still cut off ((4) above), and Q30209 again cut off by the discharge of Q30212, the emergency video from the AND gate becomes the third pulse of the emergency reply, and also retriggers the 14-μsec multivibrator ((5) above).

(8) The third set of bracket pulses (PF1 and PF2) arrives at Q30213 ((3) and (4) above), and the logic AND gate located on the ident-emergency generator subassembly generates the fourth pulse of the emergency reply. The emergency video is again coupled to retrigger the 14-psec multivibrator; however, since only three sets of bracket pulses (PF1 and PF2) were received from the airborne transponder, there is no input which can turn off Q30213 ((4) above) and the logic AND gate returns to the quiescent state. During emergency operation, an output from the logic OR gate on the video mixer subassembly is accomplished as described in d(3) above.

(9) An IFF video pulse may be displayed from any aircraft, regardless of the code used, whenever an IFF challenge is answered. The C-7014/TPX-44 BRACKET-OFF switch must be set to BRACKET. The two bracket pulses (PF1 and PF2) are present in every reply. Bracket pulse PF1 and PF2 (terminals 21 and 6 on delay line DL201) are connected to AND circuit CR207 and CR233 and cannot be switched off; consequently,

a single bracket video pulse (PF video) is produced each time the two bracket pulses (PF1 and PF2) are at the designated pulse slots on DL201. The resultant positive bracket pulse (PF video) is coupled to differential amplifier Q30007 and Q30008, and on to the inverter amplifier subassembly. The positive bracket signal (VB identification) taken directly from the collector of Q30009 is used to develop the third and fourth video pulse of the emergency display at the associated ppi ((3) above). When The C-7014/TPX-44 BRACKET-OFF switch S40305 is placed to OFF, +12 volts is applied to the base of gate driver Q30010 causing the stage to conduct. Gate driver Q30010 conducts through collector load resistor R30031 and prevents switch gate CR30004 from passing the positive output from the collector of Q30009. When switch S40305 is set to BRACKET, the base of Q30010 is returned to ground and is turned off. Switch gate CR30004 will pass the positive gated bracket video to gate amplifier Q30310 in the video mixer subassembly. Gate amplifier Q30310 triggers 1-usec multivibrator Q30311 and Q30312 to produce the video display for the bracket function.

2-10. Simulating System Functioning

a. General. The simulating system is a miniaturized test set which provides a partial operational check of the AN/TPX-41 system. Under simulated operating conditions, the simulating system tests the performance of the coding, receiving, and decoding systems without the need for external transponder replies. The simulating system is contained in Simulator, Radar Signal SM-472/TPX-44 which mounts on the front of Receiver-Transmitter, Radio RT-264D/UPX-6. The appearance of the simulated reply on the associated radar set ppi display is dependent upon a correct MODE 2 coded pulse-pair output from the coding system (TRIG IN switch set to MODE 2), proper operation of the receiving system, and normal operation of the decoding system. When the TRIG IN switch is set to PULSE, the appearance of a simulated reply indicates proper operation of the receiving and decoding systems. When a correct MODE 2 pulse pair (TRIG IN switch set to MODE 2) or when a single or double pulse (TRIG IN switch set to PULSE) is present at the input, the SM-472/TPX-44 produces a 15-pulse RF wave train corresponding to code 7777 plus one pulse. The extra pulse occurs in the x-time slot in the wave train and has no effect upon the decoding system operation. The RF wave train is applied to 2-30 the receiving system to determine whether the receiving system and associated components are operating properly. System operation of the simulating system is described in *b* through *d* below. A block diagram of the simulating system is shown in figure 2-17.

b. Decoding Circuits. The trigger input must be a correctly spaced mode 2 coded pulse-pair signal (TRIG IN switch set to MODE 2) before an output can be obtained from the coincidence gate (part of integrated circuit Z2 and Z3). The pulse inhibit multivibrator (integrated circuit Z1) prevents the second pulse of the coded pulse pair from retriggering the inhibit multivibrator. The second pulse of the coded pulse-pair signal will arrive during an approximate 20-, usec period in which the pulse inhibit multivibrator is in the gated state produced by the first pulse of the coded pulse pair. During this time period, the pulse inhibit multivibrator is not sensitive to additional input trigger pulses. The leading edge of the positive gate, produced at the output of the pulse inhibit multivibrator, triggers the 5-psec multivibrator (part of integrated circuit Z2, switch Q3 and constant-current generator Q4 on the main chassis), producing a negative gate. The negative gate produced at the output of the 5-tusec multivibrator is differentiated, and the resultant positive pulse corresponding to the trailing edge of the 5-, usec gate pulse is applied to the coincidence gate (part of integrated circuit Z2 and Z3). The coded pulse pair from the coding system is coupled to the coincidence gate. The first pulse has no effect, but with a properly spaced mode 2 code input pulse, the second pulse will arrive at the coincidence gate at the same time as the positive pulse from the 5-, usec multivibrator. At this time, a positive pulse of 1-psec duration will be developed at the output of the coincidence gate which is connected to the delay multivibrator (integrated circuit Z4, switch Q5, and constant current generator Q6). The input of a positive pulse causes the delay multivibrator to produce a negative output gate. The duration of this negative output gate may be adjusted by the DELAY control between 120 and 240 μsec. Use of this control permits adjustment of the range at which the simulated reply will appear on the associated radar set ppi display.

c. Encoding Circuits. The duration of the positive output gate from the 20.3-usec gate multivibrator (integrated circuit Z5, switch Q11, constant current generator Q12, and emitter follower Q13) is adjusted by the COUNTDOWN ADJ

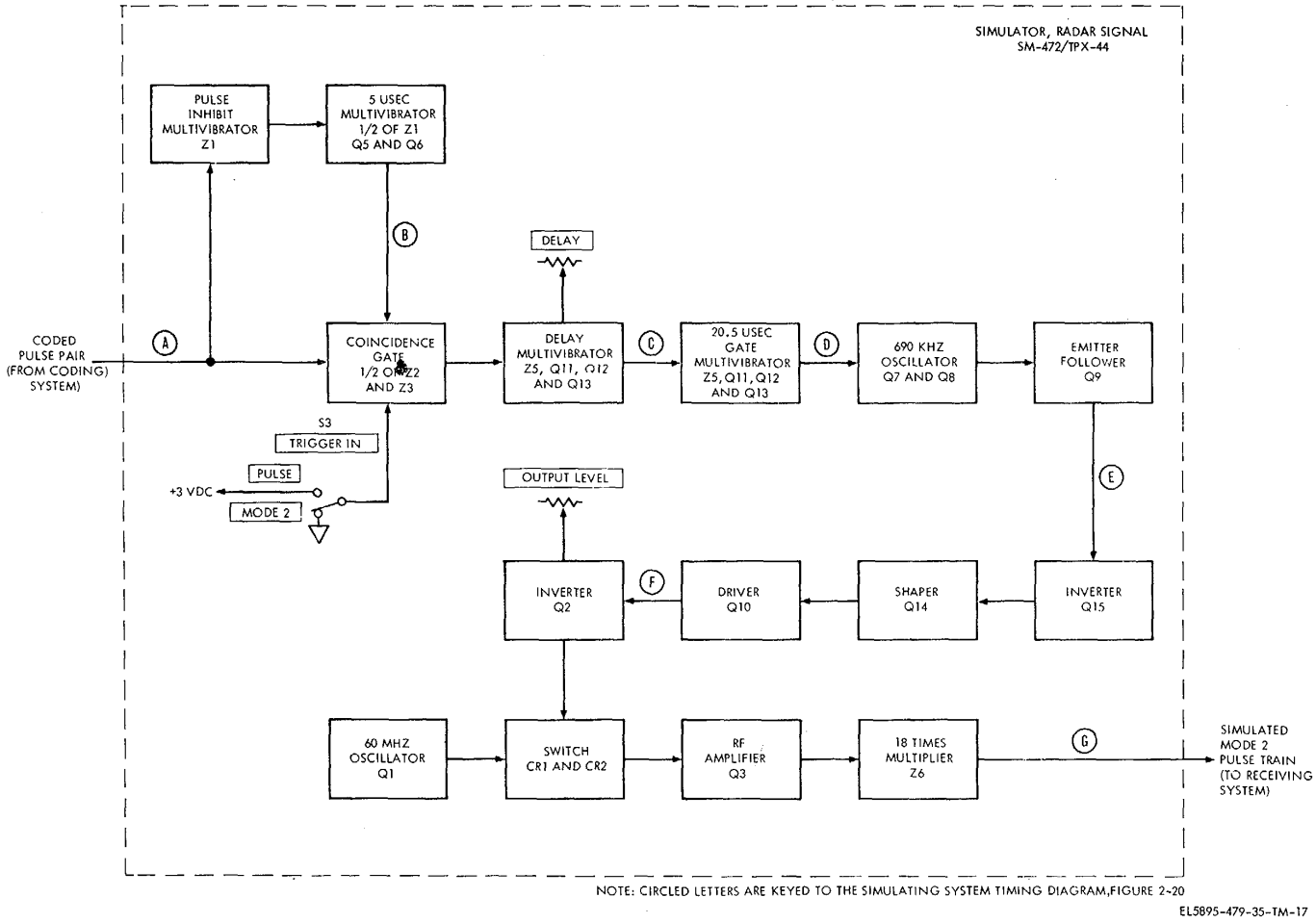


Figure 2-17. Simulating system, block diagram

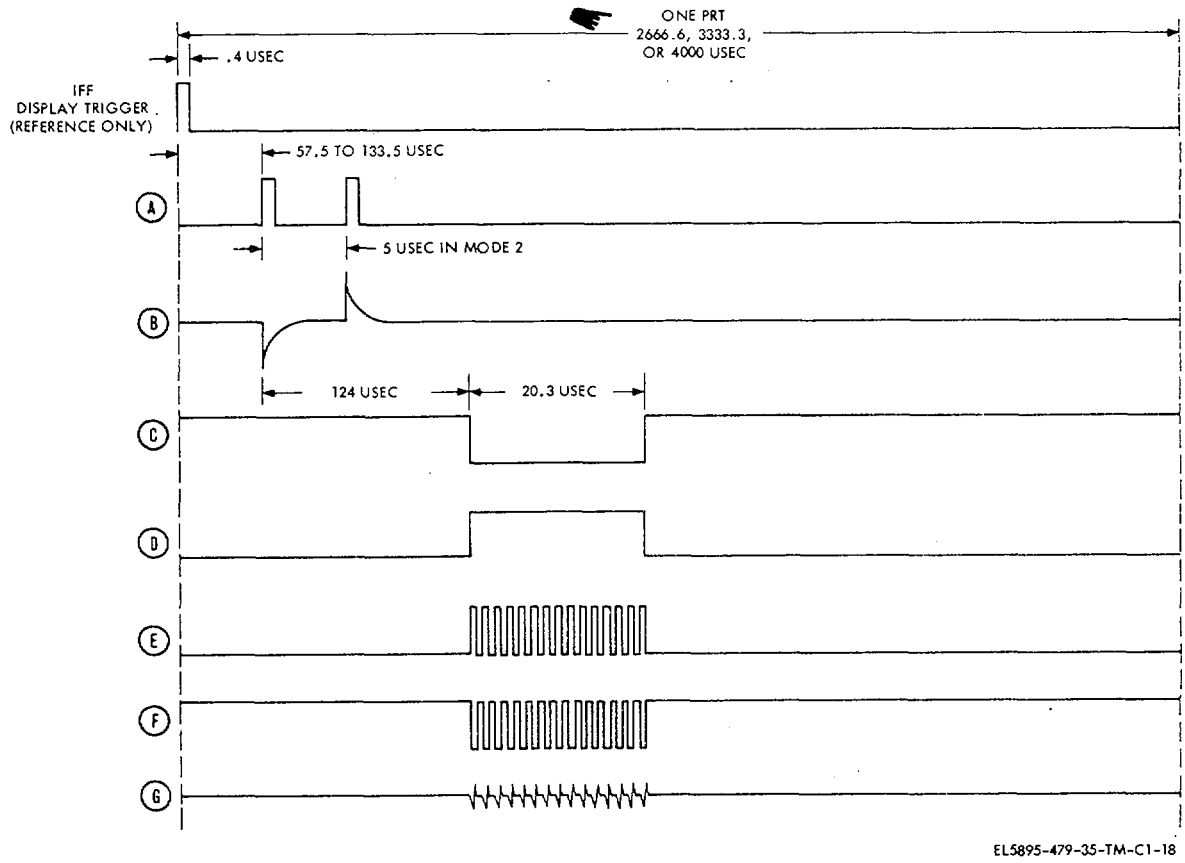


Figure 2-18. Simulating system, timing diagram.

control (R43) until the output is an adjusted positive gate of 20.3 psec nominal duration. The adjusted positive gate previously positioned by the DELAY control selects the time period during which the 690-kHz oscillator (consisting of switch Q7 and oscillator Q8) will produce exactly 15 pulses (half-cycles) spaced 1.45 usec apart. The 690-kHz oscillator is a modified Colpitts oscillator, with the operating period limited by the 20.3 /tsec gate multivibrator. The sinusoidal output of the 690-kHz oscillator is connected to emitter follower Q9, which is biased to permit only the positive half-cycles of the 15-cycle pulse train to pass. The positive rectified output of emitter follower Q9 is coupled to inverter Q15, shaper Q14, and driver Q10. During this time, the positive rectified signal is amplified and shaped, resulting in an output from driver Q10 of a coded pulse train of 15 previously shaped negative pulses.

d. RF Circuits. The negative coded pulse train from driver Q10 is coupled to inverter Q2 (located on the 60-MHz modulator subassembly). The amplitude of the positive coded pulse train from inverter Q2 may be adjusted by the OUTPUT LEVEL control on the SM-472/TPX-44 before connection to the diode switch (consisting of switches CR1 and CR2, located on the 60-MHz modulator subassembly). The 60-MHz oscillator (Q1) (located on the 60-MHz modulator subassembly) is a crystal-controlled modified Colpitts oscillator using a crystal cut for 60.5556 MHz. The 60.5556-MHz output of the 60-MHz oscillator is coupled to the diode switch. The diode switch functions as a gate that permits the 60.5556-MHz pulse wave train output signal to pass only during the time when the 15-pulse code train is present. The amplitude of the pulse wave train is adjusted by the OUTPUT LEVEL control. RF amplifier Q3 (located on the 60-MHz modulator subassembly) amplifies the 60.5556-MHz RF pulses the amount required to drive the 18-times multiplier (Z6). The 18-times multiplier consists of a high-pass filter network and step recovery diode, driving a matching section containing tuned lines cut to the 18th harmonic of 60.5556 MHz, and an impedance

matching output circuit. The output of the step recovery diode is a rectified 60.5556-MHz signal (including many harmonics). The rectified 60.5556-MHz output, including harmonics, is applied to the matching section and causes the tuned lines in the matching section to resonate at 18 x 60.5556 MHz, or 1090 MHz. The resultant 1090-MHz RF pulse train output is routed to the receiving system for testing purposes.

2-11. Power Distribution System

a. General. The power distribution system controls and distributes system power to the various units of the AN/TPX-41. The switching and connecting circuitry required to accomplish controlled application of system power is contained in Interconnecting Box J-2945/TPX-41. All of the major components of the AN/TPX-41 operate on single-phase, 120-volt, 50/60-Hz. When switches on the J-2945/TPX-41 are set properly, power is applied to the antenna system drive motor and the following major components at the receiver transmitter site: (1) Blanker, Interference MX-8795/ TPX-41.

(2) Coder-Control KY-97C/TPX-41.

(3) Modulator, Pulse MD-638/TPX-41.

(4) Receiver-Transmitter, Radio RT-264D/ UPX-6.

(5) Simulator, Radar Signal SM-472/ TPX-44.

Decoder, Video KY-593/TPX-44, located at the indicator site, receives power from a separate ac power source also located at the indicator site. Most of the components of the AN/TPX-41 contain power supplies which convert ac system power to controlled voltages for use within the individual component. System operation of the power distribution system and the functioning of component power supplies are described in *b* through *i* below. A block diagram of the power distribution system is shown in figure 2-19.

b. Power Application. Interconnecting Box J-2945/TPX-41 receives 117-volt, 50/60-Hz power from the primary power source of the associated landing control central. When the IFF POWER ON-OFF switch on the J-2945/TPX-41 is placed to ON, 117-volt, 60-Hz power is simultaneously applied to power supplies of the following components:

(1) Blanker, Interference MX-8795/ TPX-41.

(2) Coder-Control KY-97C/TPX.

(3) Modulator, Pulse MD-638/TPX-41.

(4) Receiver-Transmitter, Radio RT-264D/ UPX-6.

(5) Simulator, Radar Signal SM-472/ TPX-44.

Application of antenna drive voltage, which is also 117-volt, 50/60-Hz, requires that the SCAN OPERATE-SAFE switch be placed to OPERATE and the SCAN ON-OFF switch be placed to ON. Decoder, Video KY-593/TPX-44 receives 120volt, 50/60-Hz input power from a convenience outlet located at the indicator site.

c. Antenna Drive. Antenna drive voltage routed from the J-2945/TPX-41 is applied to relay K20001 in Pedestal, Antenna AB-1158/ GPA-119. This causes the relay to energize and antenna drive voltage is applied to antenna drive motor B20002. On application of antenna drive voltage, the motor provides rotational drive to turn the IFF antenna at a constant rate of 15 rpm.

d. Blanker, Interference MX-8795/TPX-41 Power Supply. During normal operation, 117-volt, 50/60-Hz power from the J-2945/TPX-41 is applied to the +15 and -15-volt power supplies in Blanker, Interference MX-8795/TPX-41. These power supplies provide +15 and -15 volts at their respective outputs. The +15 volt output is applied to regulators CR31101, CR31102, and CR31103 which in turn produce regulated dc outputs of +15, +10, +6 and +3 volts. The output of the-15 volt-power supply is applied to regulators CR31104 and CR31105 which produce -15, -10, and -6-volt outputs. The positive and negative voltage outputs of the two regulating networks are used to supply circuits of the timing system discussed in paragraph 2-2 and the defruiting system discussed in paragraph 2-8.

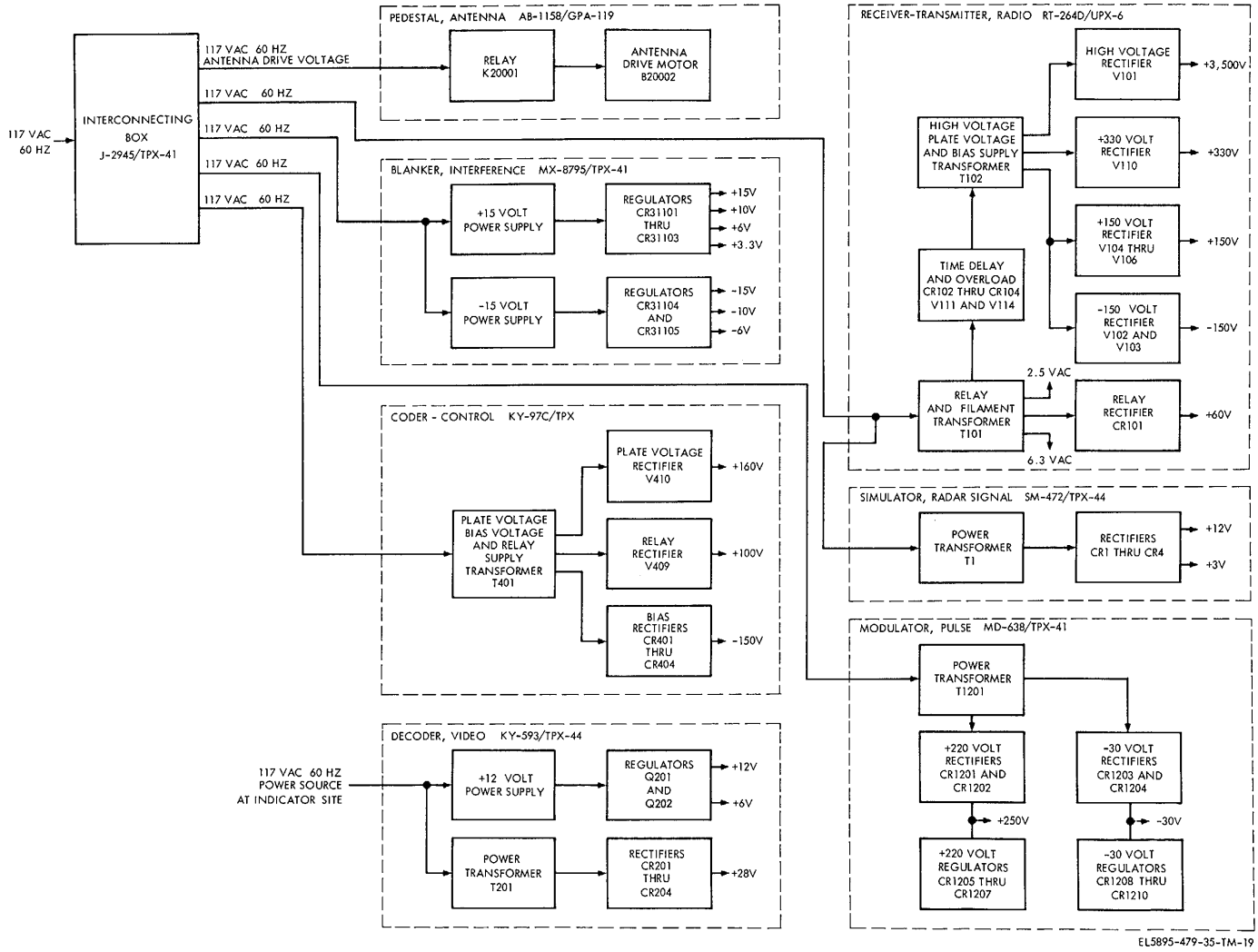


Figure 2-19. Power distribution system, block diagram

e. Coder-Control KY-97C/TPX Power Supply. The plate voltage, bias voltage, and relay supply transformer T401 in Coder-Control KY-97C/TPX receives 117-volt, 50/60-Hz power from the J-2945/TPX-41. The secondary of transformer T401 is tapped to provide voltage inputs to plate voltage rectifier V410, relay rectifier V409, and bias rectifiers CR401, CR402, CR403, and CR404. The plate voltage rectifier provides a +160-volt output, the relay rectifier provides a +100-volt output, and the bias rectifier network provides a -150-volt output. These dc voltages are used for operation of the coding system discussed in paragraph 2-3.

f. Modulator, Pulse MD-638/TPX-41 Power Supply. Power transformer T1201 in Modulator, Pulse MD-638/TPX-41 receives 117-volt 50/60-Hz power from the J-2945/TPX-41. The secondary of T1201 supplies voltage inputs to +220 volt rectifiers CR1201 and CR1202, 'and -30 volt rectifiers CR1203 and CR1204. Regulators CR1205, CR1206 and CR1207 provide regulation of the +220 volts produced by the +220-volt rectifiers. Regulators CR1208, CR1209, CR1210 provide regulation of the -30 volts produced by the -30-volt rectifiers. These voltages are used for operation of the isls system described in paragraph 2-4.

g. Receiver-Transmitter, Radio RT-264/ UPX-6 Power Supply. Relay and filament transformer T101 in the RT-264D/UPX-6 receives 117-volt, 50/60-Hzpowerfromthe J-2945/TPX-41. The secondary of T101 is tapped to provide 6.3-volt filament voltage and 2.5-volt for high voltage rectifier V101 filaments. Additional taps on T101 provide input voltage to relay rectifier CR101 which develops +60 volts for use as relay energizing voltage. The primary winding of T101 is connected in parallel with transformer T102 through a time-delay and overload circuitry consisting of CR102, CR103, CR104, V111 and V114. The time-delay circuit allows all tubes a 60-second warm-up period before application of plate voltage. The overload circuit removes power in the event of excessive current in the high voltage circuit. After the 60-second time delay elapses, 117-volt, 50/60-Hz power is applied to high voltage, plate voltage, and bias supply transformer T102. This transformer is tapped to provide voltage inputs to high voltage rectifier V101, +350-volt rectifier V110, +150 volt rectifier V104 through V106, and -50-volt rectifiers V102 and V103. These rectifier circuits produce voltage outputs of +3500, +330, +150, and -150 volts, respectively. The voltages are used in operation with transmitting and receiving systems described in paragraphs 2-5 and 2-7, respectively.

h. Decoder, Video KY-593/TPX-44 Power Supply. The KY-593/TPX-44 receives 117-volt, 50/60-Hz input power from a convenience outlet located at the indicator site. The input power is applied to a +12-volt power supply and power transformer T201. The output of the +12-volt power supply is connected to regulators Q201 and Q202 which in turn produces regulated dc outputs of +12 and +6 volts. Transformer T201 is tied to a bridge rectifier consisting of CR201, CR202, CR203, and CR204. This bridge network produces +28 volts. The +12-, +6-, and +28-volt outputs are used for operation of the decoding system described in paragraph 2-9.

i. Simulator, Radar Signal SM--472/TPX-44. The SM-472/TPX-44 receives 117-volt, 50/60-Hz input power from a convenience outlet located on the front panel of the RT-264/UPX-6. The input power is applied to power transformer T1. The secondary of T1 is connected to a bridge rectifier network consisting of CR1 through CR4. This bridge rectifier produces +12and +3-volt outputs for operation of the simulating system described in paragraph 2-10.

Section II. MAJOR COMPONENTS CIRCUIT ANALYSIS

2-12. Introduction

This section provides detailed explanation and analysis of the circuits contained within the major components of Interrogator Set AN/TPX-41. When circuit analysis of a specific component is contained in a separate manual, the applicable TM is referenced as necessary.

2-13. Blanker, Interference MX-8795/TPX-41

a. General Blanker, Interference MX-8795/TPX-41 contains the circuitry of the timing system (discussed in para 2-2) and the defruiting system (discussed in para 2-8). The principle components that comprise these systems

are contained on three circuit card assemblies; processor (chassis series No. 30800), trigger/gate generator (chassis series No. 30900) and synchronizer multiplier (chassis series No. 31000). Circuits which supply and regulate power for operation of the timing and defruiting systems are located on the main chassis of the MX-8795/TPX-41, (chassis series No. 31100). A delay line, used in conjunction with the defruiting system, and a band pass filter, used in conjunction with the timing system, are also mounted on the main chassis of the MX-8795/TPX-41. Functional operation of the circuits contained with in the MX-8795/TPX-41 is discussed in *b* through *e* below.

b. Power Supply and Regulating Circuits (Chassis Series No. 31100). The power supply circuits of Blanker, Interference MX-8795/TPX-41 consist of a regulated power supply module for both positive and negative output voltage (unrepairable, sealed unit) and voltage regulators. These circuits provide circuit supply, biasing, and indicator lamp voltages for the MX-8795/TPX-41, and require 117-volt, single-phase, 50/60or 400-Hz input power. Input power applied to AC POWER connector J1 on the front panel of the MX-8795/TPX-41 is connected through POWER switch S1 and fuse Fl. When S1 is placed to ON, the ac input is connected in parallel, with ac common to pin C and 120 volts ac to pin A on power supplies PS1 and PS2. Power indicator lamp DS1 is connected across the ac line, and application of power causes it to light green. Power supplies PS1 and PS2 provide the necessary stepdown, rectification, and regulation within a nonrepairable sealed unit. Power supply PS1 provides regulated +15 volts for circuit operation and external regulator circuits to obtain bias voltages of +10, +6, and +3.3 volts. Power supply PS2 provides regulated -15 volts for circuit operation and the voltage regulator networks to obtain bias voltages of -10 and -6 volts for circuit operation. Functional operation of power supply and regulating circuits is described in (1) through (8) below. A schematic diagram showing interrelationships of the power supply circuits with other circuits of the MX-8795/TPX-41 is shown in figure FO-10.

(1) Power input circuits. Ac power obtained from a suitable power source is applied to pins A and B of AC POWER connector J1 on the rear panel of the MX-8795/TPX-41. When POWER switch S1 is placed to the ON position, both power supply PS1 and power supply PS2 are energized. A 1/2-ampere fuse, Fl (slo-blo type) is inserted in series with S1, PS1, and PS2 for protection against circuit overloads. POWER indicator lamp DS1 is turned on when alternating current is applied to PS1 and PS2 by S1.

(2) *Power supply PS1.* Power supply PS1 is a nonrepairable sealed unit, containing a stepdown transformer, a full-wave bridge rectifier, and a series voltage regulator. Power supply PS1 is energized when POWER switch S1 is placed to ON, connecting 117 volts to pins A and C. Pin D connects ground to the case and the input transformer shield on PS1. Pins J and H are connected to external resistors R1 and R9. The +15V ADJ control, R1, permits adjustment of the series voltage regulator at PS1 to +15 volts. The output voltage from PS1 appears at pin F and +15V test point TP2. Pins R and N (negative output) are interconnected at POWER SUP COM test point TP1 (ground) to establish a ground reference to the positive output at pin F. The input to voltage regulator network CR1 through CR3 is +15 volts, which may be observed at +15V test point TP2. If PS1 should be overloaded, an internal current limiting device will maintain the current below the maximum permissible output of 250 ma. When the overload condition is corrected, PS1 will resume normal operation.

(3) *Positive 10-volt regulator.* The +15 volts from power supply PS1 is applied to resistor R3, which serves as a current limiting resistor for voltage-regulating Zener diode CR1. A regulated +10 volts at the junction of R3 and CR1 is filtered by capacitor C1 to become the +10-volt output of the regulator.

(4) *Positive 6-volt Regulator.* The +15 volts from power supply PS1 is applied to resistor R4, which serves as a current limiting resistor for voltage-regulating diode CR2. A regulated +6 volts at the junction of R4 and CR2 is filtered by capacitor C2 to become the +6 volt output of the regulator.

(5) *Positive 3.3-volt regulator.* The +15 volts from power supply PS1 is applied to resistor R5, which serves as a current-limiting resistor for voltage-regulating Zener diode CR3. A regulated +3.3 volts at the junction of R5 and CR3 is filtered by capacitor C3 to become the +3.3-volt output of the regulator.

(6) Power supply PS2. Power supply PS2 is a nonrepairable sealed unit, containing a stepdown transformer, a full-wave bridge rectifier, and a series voltage regulator. When POWER switch SI is placed to ON, PS2 is energized connecting 120 vac to pins A and C. Pin D connects ground to the case and the input transformer shield on the power supply. Pins J and H are connected to external resistors R2 and R100. The --15V ADJ control, R2, permits adjustment of the series voltage regulator in PS2 to -15 volts. The output voltage from PS2 appears at pins R and N, which are interconnected at -15V testpoint TP6. The -15volt output is applied to -6-volt and -10-volt regulator circuits. Pin F (positive output) is grounded to establish a ground reference to the negative -15-volt output at pins R and N. If PS2 should be overloaded, an internal current-limiting device will maintain the current below the maximum permissible output of 250 ma. When the overload condition is corrected, PS2 will resume normal condition.

(7) *Negative 6-volt regulator.* The negative 15 volts from power supply PS2 is applied to resistor R6, which serves as a current-limiting resistor for voltage-regulating Zener diode CR4. A regulated -6 volts at the junction of R6 and CR4 is filtered by capacitor C4 to become the -6-volt output of the regulator.

(8) *Negative 10-volt regulator.* The negative 15 volts from power supply PS2 is applied to resistor R7, which serves as a current-limiting resistor for voltage-regulating Zener diode CR5. A regulated--10 volts at the junction of R7 and CR5 is filtered by capacitor C5 to become the -10-volt output of the regulator.

c. Trigger/ Gate Generator (Chassis Series No. 30900). The trigger gate generator (chassis series No. 309001 is a circuit card assembly which comprises the principle components of the timing system. Functional operation of the trigger/ gate generator is described in (1) through (14) below. A schematic diagram of the trigger gate generator is shown in figure FO-10.

(*1) Astable multivibrator QI and Q2.* Astable multivibrator QI and Q2 has a natural frequency of approximately 182.5 Hz, but is synchronized by the circulating pulse at 375, 300, or 250 Hz. To analyze QI and Q2 as an astable multivibrator, assume Q2 is conducting and Q1 is cut off. Transistor Q, I is cut off because its base is always referenced at ground potential by resistor R1 and a positive voltage is coupled to the emitter of QI through capacitor C3 by the conduction of Q2; however, Q1 cannot remain cut off since C3 will try to charge to the potential difference of voltage developed by Zener diode CR1 and the voltage at the emitter of Q2. The reverse bias on QI decreases as the charge on C3 increases. When the voltage at the emitter of QI reaches a point slightly below zero, Q1 begins to conduct. causing a voltage drop across resistor R4. The voltage drop across R4 will cut off Q2. With Q2 cut off, C3 will start to discharge through resistors R6 and R3. This discharge current must also flow through Q1 and R4. As C3 discharges. the positive potential on the emitter of Q2 decreases to forward-bias Q2, and the current through R6 is now through Q2 instead of QI. This reduces the current through R4, causing the voltage at the base of Q2 to go more positive, increasing the conduction of Q2 and the voltage across R6. The increased potential across R6 reduces the conduction of Q1. This regenerative cycle cuts QI off completely capacitor C3 starts to charge and the emitter voltage of Q1 beings to decrease until Q1 is again turned on and the complete action is repeated again. Capacitor C4 and resistor R2 form a decoupling network. After the initial application of power, the first pretrigger is generated and routed through the processor, PRF SEL switch S3. and delay line DL31101. The output of the delay line is routed through the contacts of S3, back through the processor, and is coupled to the base of QI via capacitor C1 to control the conduction time of the multivibrator. Control pulse (CP) test-point TP2 permits observation of the circulating pulse with an oscilloscope. The rectangular waveshape from QI and 02 is applied to trigger shaper Q3.

(2) *Trigger shaper Q3.* Trigger shaper Q3 is normally conducting since its base is connected to a positive voltage through resistor R8 and P W ADJ control R7. When the negative half-cycle gate from multivibrator QI and Q2 is applied to the base of Q3 through resistor R5 and capacitor C5, Q3 cuts off. When Q3 cuts off, its collector rises toward + 6 volts. The time that the negative half-cycle can hold Q3 cut off is determined by the adjustment of R7. The output of Q3 is a positive 6-volt pulse adjusted to a 0.5-, sec duration by R7. Resistor R9 provides a load for the collector of Q3. The output of Q3 is applied to emitter follower Q4, delay line driver Q5, and inverter Q14.

(3) *Emitter follower Q4.* The positive pulse output of trigger shaper Q3 is coupled through capacitor C6, developed across R10, and applied to the base of emitter follower Q4. The output of Q4 is developed across resistor R11 and applied to the processor and trigger generator as the pretrigger / circulating pulse. PRE-TRIG test point TP3 permits observation of the pretrigger/circulating pulse on an oscilloscope.

(4) IFF enable gate generator. The IFF enable gate generator consists of delay line driver Q5, switchQ6.1100-µsec monostable multivibrator Q7 and Q8, and amplifiers Q9 and QI0. The input to the delay line driver is the positive pulse from trigger shaper Q3. The IFF input and output enable gates are taken from the amplifiers and applied to the processor subassembly.

(5) Delay line driver Q5. The positive pulse from trigger shaper Q3 is coupled through capacitor C, . developed across resistor R12 and applied to the base of delay line driver Q5. Delay line driver Q5 conducts through resistor R13 and delay line DLI, causing the pulse to be delayed by 1.5 µsec. The delay establishes proper relative timing of the IFF enable and circulating pulse enable gates utilized in the processor subassembly. The positive output of delay line DLI is applied to inverters Q6 and QII.

(6) *Inverter Q6.* The positive pulse from the output of delay line DLI is direct-coupled through resistor R14, developed across resistor R15 and applied to the base of inverter Q6. The negative pulse output of inverter Q6 is applied to monostable multivibrator Q-7 and Q8. Diode CR7 prevents the positive pulse applied to the base of inverter Q6 from exceeding the base-to-emitter rating of Q6.

(7) Monostable multivibrator Q7 and Q8. The normal state of monostable multivibrator Q7 and Q8 is Q7 cut off and Q8 conducting. The negative bias voltage applied to the base of Q7 through resistors R 7 and R5 I maintains Q7 in the cutoff state. Capacitor C 17 and resistor R5 1 form a decoupling network. Transistor Q8 is allowed to conduct by the positive bias voltage applied to its base through resistors R19 and R50 and IFF GATE control R20. Capacitor C16 and resistor R 50 form a decoupling network. The conduction of transistor Q8 drops essentially all of the +6 volts available across resistor R21; therefore no positive bias current is available through resistor R18, and transistor QT7 is cut off. With Q7 cut off, capacitor C8 is charged to + 6 volts. The negative pulse from inverter Q6 is coupled through capacitor C8 to the base of Q8. This cuts off Q8 causing its collector to rise sharply toward + 6 volts. The sharp rise in positive voltage is applied to the base of Q7 through capacitor C9 and resistor R18, causing Q7 to conduct. With Q7 conducting, capacitor C8 discharges through resistors R19 and R20, maintaining Q8 in the cutoff state. The discharge time of capacitor C8 is determined by network C8, R19, and R20, and is determined by the adjustment of IFF GATE control R20. When C8 has discharged, QT and Q8 return to their normal states. Capacitor C9 accelerates the return by coupling a negative voltage spike to the base of Q7 when the collector of Q8 starts to swing back in the negative direction. The output of Q8 is a positive gate adjusted for 2600 µsec by R20 and is applied to inverter-amplifiers Q9 and Q10. Diode CR3 prevents the negative voltage developed by the discharge of C8 from exceeding the base-to-emitter rating of Q8.

(8) Inverter amplifier Q9 and Q10. The positive gate from monostable multivibrator QT7 and Q8 is routed through resistor R22. developed across resistor R23. and Applied to the base of amplifiers Q9 and QIO through resistors R24 and R2T respectively. The output of each amplifier is a negative 2600sec gate, designated IFF input enable gate from Q9 and IFF output enable gate from QIO. These enable gates are applied to the processor subassembly I *e* below). Resistors R25 and R28 provide loads for the collectors of Q9 and QIO respectively. Diode CR5 prevents the positive pulse applied to the base of Q9 from exceeding the base-emitter rating of Q9. Diode CR6 prevents the positive pulse applied to the base of QIO from exceeding the base-to-emitter rating of QIO.

(9) *Inverter Q11.* The positive pulse from the output of delay line DLI is direct-coupled through resistor R30, developed across resistor R31, and applied to the base of inverter Q11. The negative pulse output of QII is applied to monostable multivibrator Q12 and Q13. Diode CR8 prevents the positive pulse applied to the base of Q11 from exceeding the base-to-emitter rating of Q11.

(10) Monstable multivibrator Q12 and Q13. The normal state of monostable multivibrator Q12 and Q13 is Q12 cut off and Q13 conducting. The negative bias voltage applied to the base of Q12 through resistors R33 and R 51maintains Q12in the cutoff state. Transistor Q13 is allowed to conduct by the positive bias voltage applied to its base through resistors R35 and R50 and CP GATE control R36. The conduction of QI3 develops a voltage drop approximately +6 volts across resistor R37; therefore, no positive bias current is available through resistor R34 and Ql2 is cut off. With Q12 cut off, capacitor CI 0 is charged to + 6 volts. When the negative pulse from switch Q11 is coupled through CIO0 to the base of Q13, is cut off immediately. With Q13 cut off, its collector rises sharply toward + 6 volts. The sharp rise in positive voltage is applied to the base of Q12 through capacitor CII and resistor R34, causing Q12 to conduct. With Q12 conducting. capacitor C12 will begin to discharge through resistors R35 and R36, maintaining Q13 in the cutoff state. The discharge

time of capacitor C10 is determined by rc network C10, R35, and R36. Discharge time is determined by adjustment of CP GATE control R36. With C10 discharged, Q12 and Q13 return to their normal state. Capacitor C11 speeds the return by coupling a negative voltage spike to the base of Q 12 when the collector of Q13 starts to swing back in the negative direction. The output of Q13 is the positive circulating pulse gate adjusted for 3000 μsec by R36 and is applied to the processor as the circulating pulse gate. Diode CR4 prevents the negative voltage developed by the discharge of capacitor CIO0 from exceeding the base-to-emitter rating Q13. Control pulse (CP GATE) testpoint TP4 is provided for observation of the circulating pulse gate with an oscilloscope.

(11) *Inverter Q14.* The positive pulse from trigger shaper Q3 is coupled through capacitor C12 and resistor R38, developed across resistor R39, and applied to the base of inverter Q14. The negative pulse output of Q14 is applied to monostable multivibrator Q15 and Q16. Diode CR9 prevents the positive pulse applied to the base of Q14 from exceeding the base-to-emitter rating of Q14.

(12) *Monostable multivibrator Q15 and Q16.* The normal state of monostable multivibrator Q15 and Q16 is QI5 cut off and Q1 conducting. The positive voltage at the base of Q 16, developed across resistor R43, diode CR2, and DELAY ADJ control R42, allows Q16 to conduct. The conduction of Q16 develops a voltage drop of approximately + 6 volts across resistor R45. Therefore, no positive bias current is available through resistor R41, and Q15 is cut off. With Q15 cut off, capacitor C13 is charged to +6 volts. The negative pulse from switch Q14 will back-bias CR2, which cuts off Q16 by removing its positive bias voltage. With Q16 cut off, its collector rises sharply toward + 6 volts. The sharp rise in positive voltage is applied to the base of QI5 through C14 and R41, causing Q15 to conduct. With Q15 conducting, C13 begins to discharge through R42 and R43, maintaining Q16 in the cutoff state. The discharge time of C13 is determined by rc network C13, R42, and R43, and is set by the adjustment of DELAY ADJ control R42. When C13 has discharged, QI5 and Q16 return to their normal states. Capacitor C 14 speeds the return by coupling a negative voltage spike to the base of Q15 when the collector of Q16 starts to swing back in the negative direction. The output of Q16 is a positive gate adjusted by R42 and is applied to amplifier Q17.

(13) *Inverter amplifier Q17. The* positive gate from monostable multivibrator Q15 and Q16 is direct-coupled through resistor R 46 and applied to the base of amplifier Q17. The negative output gate of Q17 is applied to emitter follower Q18. Resistor R17 provides a load for the collector of Q1.

(14) *Emitter follower Q18.* The negative gate from amplifier QI7 is differentiated by capacitor C 15 and resistor R48, and the positive trailing edge is applied to the base of emitter follower Q18, causing QIS to conduct. The conduction of Q18 produces a positive pulse on its emitter, delayed from the input of switch Q14. This pulse is designated delayed trigger, and is applied to the synchronizer multiplier. The DLYD TRIG testpoint TP5 is provided for observation of the delayed trigger with an oscilloscope. Resistor R49 provides a load for the emitter of Q18.

d. Synchronizer Multiplier (Chassis Series No. 31000). The synchronizer multiplier (chassis series No. 310-00) is a circuit card assembly which comprises the circuits required to develop the IFF trigger and 1500-Hz radar sync outputs of the timing system. Functional operation of these circuits is described in (1) through (5) below. A schematic diagram of the synchronizer multiplier is shown in figure FO-10.

((*1) Amplifier Q1 and Q2.* The delayed trigger from the trigger gate generator is applied to PI-W of the synchronizer multiplier. The trigger is developed across resistors RI and R2 and applied to the base of amplifier QI. Amplifier Q1 inverts and amplifies the delayed trigger to produce a negative trigger at its collector. This trigger is recoupled through C17, C1, and R5 to the base of amplifier Q2. The fast time constant provided by C1 and R5 reduces the trigger fall time, thereby decreasing the trigger pulse width to 0.5 sec. Amplifier Q2 provides a final stage of amplification and inversion to produce a positive trigger output at its collector. This trigger is routed out of the synchronizer multiplier at PI-X as the IFF trigger at a pulse repetition rate of 300 pps. The IFF TRIG testpoint TP3 is provided for observation of the trigger with an oscilloscope.

(2) Monostable multivibrator Q5 and Q6. The IFF circulating pretrigger from the trigger gate generator is applied to P -U of the synchronizer multiplier. The trigger is developed across R41, CR1, and R19 and applied to the base of transistor Q5. Transistors Q5 and Q6 form a monostable multivibrator. Diodes CRI and CR2 are connected in series with the bases of Q5 and Q6 respectively. This insures that Q5 and Q6 are not driven by a voltage which exceeds their emitter-to base breakdown ratings. Prior to application of the IFF circulating pretrigger, Q5 is cut off and Q6 is

conducting. The positive IFF circulating pretrigger applied to the base of Q5 causes the stage to conduct; causing the voltage on the collector of Q5 to drop from approximately + 10 volts to near zero. The negative voltage swing is coupled through capacitor C8 and applied to the base of Q6. The negative-going voltage cuts Q6 off, causing its collector to rise to approximately + 10 volts. The l 0-volt rise forms the leading edge of the multivibrator pulse output. The positive voltage at the collector of Q6 is also coupled across R20 and C9, and is applied to the base of Q5 to hold the stage in conduction. This condition continues until capacitor C8 charges to a level capable of causing Q6 to conduct. The charge time of C8 is determined by the re time constant of C8, R18, and DELAY ADJ control RI7. The DELAY ADJ control is adjusted for a charge rate that permits Q6 to conduct after approximately 450 + 90 to 670 /µsec to cutoff time. When Q6 returns to conduction, its collector voltage falls to approximately zero, forming the trailing edge of the multivibrator pulse output. The negative-going voltage drop at the collector of Q6 is also coupled across network R20 and C9 as a negative spike. This negative spike is applied to the base of Q5 to cut the stage off and return the multivibrator to its initial state. The DELAY GATE testpoint TP2 is provided for observation of the pulse with an oscilloscope.

(3) Twin-T oscillator Q7, Q8. and Q9. The pulse output of multivibrator Q5 and Q6 is differentiated by C19 and R45 and ac coupled through CR3, R44, C13, and C15 to the base of amplifier Q8. Amplifier Q8 is part of twin-T oscillator comprised of Q7, Q8, and Q9. The input to the base of amplifier Q8 comprises the input to the oscillator. Oscillator feedback required to sustain oscillations and the negative differentiated pulse from monostable multivibrator Q5 and Q6 are applied to the base of Q8 to establish the phase relation and set the operating frequency of the oscillator. The sine wave output at the collector of Q8 is coupled to the base of phase-splitter Q9. The phase-splitter provides positive voltage in phase with the input to the base of Q8 and negative voltage out-of-phase with the input to Q8. The in-phase and out-of-phase outputs of Q9 are applied to separate legs of a twin-T network comprised of R24, R26. R27, R30, C100 C11, and C14. The positive in-phase signal at the emitter of Q9 is applied to one leg of the twin-T network at the junction of R30 and R24. The negative out-of-phase signal at the collector of Q9 is applied through LEVEL control R37 to the second leg of the twin-T network at the junction of R26 and C14.

The output of the twin-T network is taken from the junction of R27 and CI I and applied to the gate of source follower Q7. The resultant output of the source follower is coupled through capacitor C15 and applied to the base of amplifier Q8 as feedback.

The FREQ control R24 in the twin-T network is adjusted to attain an oscillator operating frequency of 1500 Hz. Frequency stabilization is achieved by the action of the twin-T network. The twin-T network passes the positive in-phase output of phase-splitter Q9 only when oscillation occurs at the specific frequency established by the setting of R24.Thisin-phasesignal comprises the regenerative feedback that is coupled through Q7, C1, and applied to the base of amplifier Q8 to sustain oscillation. The negative differentiated pulse from monostable multivibrator Q5 and Q6 is applied to the base of amplifier Q8 to synchronize the oscillator output with the IFF pretrigger. The negative pulse causes amplifier Q8 to produce a negative swing of the 1500-Hz oscillator signal at IFF pretrigger time. In this manner, phase correction is accomplished every 4, 5, or 6 cycles of the 1500-Hz signal; once every IFF pretrigger interpulse period.

(4) *Emitter follower Q3.* The 1500-Hz since wave output of Q8 is coupled to the base of emitter follower Q3. The output of Q3 is developed across R9 and applied to transistors Q4 and QIO through capacitors C3 and C4 respectively.

(5) *Complementary pair amplifier Q4 and QO1. Transistors* Q4 and Q10 form a complementary pair amplifier which provides amplification to insure sufficient amplitude of the 1500-Hz sine wave output. The BAL control R39 is adjusted to obtain symmetry of the 1500-Hz sine wave output. The output of the complementary pair amplifier is developed across R14 and routed out of the synchronizer multiplier at P1-Z as the 1500-Hz radar synchronizing signal. The 1500 CPS testpoint TP4 is provided for observation of the signal with an oscilloscope. The 1500-Hz synchronizing signal is applied to band-pass filter FL 31101 on the main chassis of the MX8795 / TPX-41 before final routing out of the MX8795 / TPX-41 to the associated radar equipment.

e. Processor (Chassis Series No. 30800) and Delay Line DL31101. The processor (chassis series No. 30800) is a circuit card assembly that comprises the principle circuits of the defruiting system. Delay Line DL31101 is located on the main chassis of the MX-8795/TPX-41 and is used in conjunction with the processor to accomplish the defruiting process. Functional operation of the processor and delay line DL31101 is described in (1 through (18)} below. A schematic diagram of the processor is shown in figure FO-10.

(1) Video standardization and mixing. The

video standardization and mixing circuitry consists of threshold limiter Q30801, quantizer Q30802, inverter amplifier Q30803. AND gates Q30804 and Q30817. OR gates Q30805 and Q30806, delay line driver Q30807, and delay line DL31101 on the main chassis. The input to threshold limiter Q30801 is raw iff video from the receiving system. The output of delay line DL31101 is applied to video amplifier Q30814.

(2) Threshold limiter QI. Positive raw IFF video from the receiving system is coupled through capacitor C1. developed across resistor R3, and applied to the base of threshold limiter QI. Resistor R2 sets the bias level for Q1. Resistors R4 and R5 form a voltage divider which applies additional cutoff bias to QI. Any signal greater than l-volt amplitude is passed through QI. The raw IFF video may be observed with an oscilloscope at IFF VID IN testpoint TP3.

(3) *Quantizer Q2.* Positive IFF video output from threshold limiter Q1 is direct-coupled through resistor R 6 to the emitter of quantizer Q2. Resistor R6 and diode CRI set the bias level for Q2. Resistor R7 provides a load for the collector of Q2. The limited positive pulse output of Q2 is applied to inverter amplifier Q3.

(4) *Inverter amplifier Q3.* The positive pulse output from quantizer Q2 is coupled through capacitor C2 and rc network C3 and R9, developed across resistor RIO, and applied to the base of inverter amplifier Q3. Capacitor C3 passes the higher frequencies and restricts the gain for lower frequencies. The rise and fall time of the video pulses is thereby improved. Resistor R 1 provides a load for the collector of Q3 (5) *AND gate Q4 and Qf7.* The 2600Asec IFF input enable gate from the trigger/gate generator subassembly is direct-coupled through resistor R45 and applied to the base of AND gate Q17. The negative pulse out from inverter amplifier Q3 is coupled through capacitor C4 to the base of AND gate Q4. Resistor R13 sets the bias level for Q4 and resistor R14 provides a load for the collectors of Q4 and Q17. With negative pulses applied simultaneously to the base of AND gates Q4 and Q17, the output of the AND gate that is applied to OR gate Q5 will be positive IFF video pulses. In the absence of simultaneous negative pulses, either or both stages will conduct heavily and the junction of R 14 and the collector of Q4 and Ql7 will be near ground potential.

(6) *OR gate Q5 and Q6.* The positive pulse from AND gate Q4 is applied to the base of OR gate Q5. The positive pulse is inverted and coupled through capacitor C5 and applied to line delay driver Q7. The positive pretrigger / circulating pulse from the trigger/gate generator subassembly is direct-coupled through resistor R26, developed across resister R27 and applied to the base of OR gate Q6. The positive pulse is inverted and applied to delay line driver Q7. An input to either Q5 or Q6 at any time will produce an output.

(7) Delay line driver Q7. The negative pulses from OR gates Q5 and Q6 are coupled through capacitor C5 and applied to the base of delay line driver Q7. The delay line input from delay line driver Q., which may be viewed at DLY LINE IN testpoint TP2. is coupled through capacitor C18 to delay line DL31 101 on Blanker, Interference MX8795 / TPX-41 main chassis.

(8) *Delay line DL31101 and PRF , SEL switch S31103.* Magnetostrictive delay line DLI is physically located on Blanker, Interference MX8795/TPX-41 chasses. The delay line contains three delay lines, the inputs and outputs of which are selected by PRF SEL switch S3. The positive delay line input pulse, from delay line driver Q30807 in the processor subassembly. is applied through S3 to delay line DLI, where it is delayed 2666.6, 3333.3, or 4000 Asec (one interpulse period). The output of DLI (delayed IFF video) is applied through S3 to video amplifier Q30814 in the processor subassembly.

(9) *Processed video generator circuits.* The processed video generator circuitry consists of video amplifiers Q9. Q11, and Q14; AND gates QIO, QI3, and QI8; and inverter amplifier Q12. The positive processed video from inverter amplifier Q12 is applied to bypass relay K1.

(10) Video amplifier Q9 and Q14. The IFF video output from AND gate Q4 and QI7 is applied to the base of video amplifier Q9. Resistor R18 provides a load for the collector of Q17. The positive delayed IFF video from delay line DL31101, which may be viewed at DLYD IFF VID testpoint TP5, is applied to the base of video amplifier Q14 through capacitor C12 and resistor R33 and developed across resistor R34. Video amplifier Q14 amplifies and inverts the delayed IFF video. Resistor R35 provides a load for the collector of Q14.

(11) *AND gates Q10, Q13, and Q18.* The negative IFF video from video amplifier Q9 is coupled through capacitor C7 to the base of AND gate QIO. Current through resistor R20 and the base of QIO0 turns that stage on. The negative 2600t sec IFF output enable gate from the trigger / gate generator subassembly, which may be viewed at IFF ENABLE testpoint TP7, is coupled through resistor R46 to the base of AND gate Q18. Diode CR 4 protects the base-emitter junction of Q 18. The negative output of video amplifier Q14 is coupled

through capacitor C13 to the base of AND gate Q13. Current through R38 and the base of Q13 turns that stage on. Negative pulse input must be present at the bases of Q10. Q13, and QI8 before output signals can be produced.

(12) *Video amplifier Q11.* The positive pulse (IFF video from AND gates Q100, Q13, and Q18 is coupled through capacitor C8, developed across resistor R23 and applied to the base of video amplifier Q11.

(13) *Inverter amplifier Q12.* The negative pulse from video amplifier Q 1I is direct-coupled through resistor R25 to the base of inverter amplifier Q12. Resistor R24 sets the bias level for Q12. Resistor R30 provides a load for the collector of Q12. The positive pulse from Q12 is applied to contact I of bypass relay KI.

(14) *Unprocessed video circuit.* The raw IFF video. from the receiving system, is applied to the base of emitter follower Q8 through capacitor C6 and developed across resistor R31. Resistor R32 provides a load for the emitter of Q8. The output (raw IFF video) of emitter follower Q8 is applied to contact 5 of bypass relay K1.

(15) *Bypass relay K1.* Bypass relay KI is shown in the deenergized state. Relay KI is energized by placing PROCESSED VIDEO-RAW VIDEO switch S31102, located on the front panel of the MS-8795/TPX-41, to the RAW VIDEO position. In the RAW VIDEO position, negative 15 volts (bypass control) is routed through switch S31102, through the windings of relay K1 to ground. Contact 7 of relay KI is tied to ground. With relay K1 energized. the raw IFF video present at contact 5 of relay K1 is coupled through capacitor CII and out of the MS-8795 / TPX-41 at IFF VID OUT connector J31103. The video is then applied to associated remoting equipment for routing to decoder, Video KY-593 / TPX-44. The raw IFF video may be viewed at IFF VID OUT testpoint TP6. With relay K1 deenergized, the processed video present at contact of relay K1 is coupled through capacitor C1 and out of the MX8795/TPX-41 at IFF VID OUT connector J31103. The processed video is then applied to associated remoting equipment for routing to Decoder, Video KY-593 / TPX-44. The processed video may be viewed at IFF VID OUT testpoint TP6. The --15 volts present at PI-D on the main chassis of the MS-8795 / TPX-41 may be used for connection of a remote bypass switch. By connecting this switch between PI-D and C, control of bypass relay K1 may be accomplished from a remote position.

(16) Circulating pulse generator circuits. The circulating pulse generator circuit consists of logic'

AND gate Q15 and Q16, and emitter follower Q19. The positive circulating pulse output from emitter follower Q19 is applied to the trigger/gate generator assembly.

(17) *AND gate Q15 and Q16.* The positive circulating pulse gate is direct-coupled through resistors R42 and R44, developed across resistor R43 and applied to the base of AND gate Q16. Diode CR2 protects AND gate Q16 base-emitter junction. The output of video amplifier Q14 is negative delayed IFF video coupled through capacitor C14 and resistor R39, and applied to the base of AND gate Q15. Negative pulse inputs must be present at the base of both Q15 and Q16 before output signals can be produced.

(18) *Emitter follower Q19.* The output of AND gate Q15 and Q16 is applied to the base of emitter follower Q19, whose positive circulating pulse output developed across resistor R50 is fed back to the trigger/gate generator subassembly. The circulating pulse output may be viewed at CP OUT testpoint TP4.

2-14. Coder-Control, Interrogator Set KY-97C/TPX

Coder-Control, Interrogator Set KY-97C/TPX contains the principle circuits of the coding system (para 2-3). For detailed analysis of the circuits contained within the KY-97C/TPX, refer to TM 11-5895-201-35.

2-15. Control, Remote Switching C-1271A/TPX-22

a. General. Control, Remote Switching C-1271A/TPX-22 contains control and switching circuits to permit control of coding system functions from a position convenient to the radar operator. The controls on the C-1271A/TPX-22 are similar in construction and identical in function to those located on the Coder-Control KY-97C/TPX. A schematic diagram of the remote switching control, is shown in figure FO-11. Connection between the C-1271A/TPX-22 and the KY-97C/TPX may be achieved by means of a direct cable connection or through remoting equipment supplied with the AN/TPX-41 as additional equipment. In addition to providing duplicate control and indicating functions of the coding system, the C-1271A/TPX-22 provides a mode of interlock circuit which coordinates operation of the coding and decoding systems. This mode interlock circuit is described in *b* below (fig. FO-11).

b. Mode Interlock Circuit. The mode interlock circuit consists of a secondary set of contacts on MODE SELECTOR SWITCH S731. Contacts 2, 3, and 4 of S731 provide the primary ground connections to establish the interrogation code setting in Coder-Control KY-97C/TPX. Contacts 8, 9, and 10 comprise the mode interlock portion of the switch. When MODE SELECTOR switch S731 is placed to the MODE 1 position, ground is applied to contact 2 of the switch and connected to the KY-97C/TPX to establish MODE 1 coding. In this position, ground is also applied to contact 8 of S731. The ground at contact 8 is connected to the return side of a set of mode 1 select relays in the C-7014/TPX-44. This ground connection allows these relays to energize, thereby establishing mode I operation of the KY-593/TPX-4. When MODE SELECTOR switch S731 is placed to the MODE 2 position, ground is applied to contacts 3 and 9 of S731. These contacts provide no connectiontotheKY-97C/TPXor C-7014/TPX-44. Code select relay logic within theKY-97C/TPXandC-7014/TPX-44 interprets the absence of a ground connection as a MODE 2 command and MODE 2 operation is established in both the KY-97C/TPX and KY-593/TPX-44. When the MODE SELECTOR switch S731 is placed to the MODE 3 position, ground is connected to contacts 4 and 10 of S731. The ground on contact 4 is applied to the KY-97C/TPX to establish MODE 3 interrogation coding. The ground on contact 10 of S731 is connected to the return side of a set of MODE 3 select relays in the C-7014/TPX-44. This ground connection allows these relays to energize, thereby establishingMODE3operationofthe KY-593/TPX-44. This method of interlocking the coding and decoding systems can only be accomplished when LOCAL-REMOTE switch S402 on the KY-97C/TPX is placed to the REMOTE position. When S402 is placed to the LOCAL position, mode selection is accomplished locally at the KY-97C/TPX and the position of S731 on the C-1271A/TPX-22 has no bearing on the selected mode of interrogation. No mode interlock connection exists between the KY-97C/TPX and the C-7014/TPX-44. For this reason, the MODE SELECTOR switches on the KY-97C/TPX and the C-1271A/TPX-22 must be set in the same positions to accomplish successful

interrogation and decoding when LOCAL-REMOTE switch S402 is placed to the LOCAL position.

2-16. Modulator, Pulse MD-638/TPX-41

a. General. Modulator, Pulse MD-638/TPX-41 contains the circuitry of the isls system (para 2-4). The principle circuits which accomplish the basic functions of the isls system are located on the pulse generator processor (chassis series No. 1300). Diplexer Z1201 and the circuits which supply and regulate power for the isls system are located on the main chassis of the MD-638/TPX-41 (chassis series No. 1200). Functional operation of the circuits contained within the MD-638/TPX-41 is discussed in *b* through *e* below.

b. Power Supply and Regulating Circuits (Chassis Series No. 1300). The power supply for the isls system consists of a regulated +250 volt module and a regulated -30-volt module. These modules provide circuit supply, biasing, and regulation for the isls system and and required 120-volt, single-phase, 60or 400-Hz input power. Switching circuitry for application of input power is located on the pulse generator processor. For operation of these circuits, see the pulse generator processor schematic diagram shown in figure FO-12. Functional operation of the power supply and regulating circuits, which are located on the main chassis of the MD-638/TPX-41, is described in (1) and (2) below. A schematic diagram of the MD-638/TPX-41 main chassis is shown in figure FO-12.

(1) Plus 250-volt supply. The voltage applied to the primary of transformer T1201 is connected through POWER switch S1301 when S1301 is placed to the ON position. A 1/2-ampere fuse, F1301, (slo-blo type) is inserted in series with POWER switch S1301 for protection against circuit overloads. The voltage across secondary windings 3, 4 and 5 of T1201 is full-wave rectified by diodes CR1201 and CR1202 and filtered by inductor L1201 and capacitor C1201. Resistor R1201 acts as a current limiter. The voltage developed across Zener diodes CR1205, CR1206, and CR1207 provides the regulated +250 volt output. Capacitor C1202 provides additional filtering while resistor R1202 acts as a bleeder resistor. A 1/8-ampere fuse, F1302, provides protection against circuit overload of the +250-volt power supply.

(2) *Minus 30-volt supply.* The voltage across secondary winding 6, 7, and 8 of T1201 is full-wave rectified by diodes CR1203 and CR1204 and filtered by capacitor C1203. Resistor R1203 acts as a current limiter. The voltage developed across Zener diodes CR1208, CR1209, and CR1210 provides the regulated -30 volt output. Capacitor C1204 provides additional filtering while resistor R1204 acts as a bleeder resistor. A 1/2-ampere fuse, F1303, provides protection against circuit overload of the -30-volt power supply.

c. Delay Ramp Generator Circuits (Chassis Series No. 1300). The delay ramp generator circuits are contained in the pulse generator processor. These circuits provide the linear ramp required to produce the delayed isls (P2) pulse. Functional operation of the delay ramp generator circuits is described in (1) through (4) below. A schematic diagram of the pulse generator processor is shown in figure FO-12.

(1) Amplifier Q1. The positive coded pair of pulses received from the coding system, located in the KY-97C/TPX is applied to the base of amplifier Q1 through energized relay K1, SLS switch S2 when placed to the ON position, resistor R3, and capacitor C1. Relay K1 is energized by the interlock circuit (e(9) below). Resistors R3 and R62 form a voltage divider which protects Q1 from the wide range of coded pair pulse amplitudes which may be encountered in the various systems in which the MD-638/TPX-41 is used. Resistor R4 establishes the base bias voltage of Q1, near cutoff. Amplifier Q1 inverts the pulses and couples them to the base of transistor Q3 through capacitor C2. Resistor R5 provides a collector load for Q1 and transistor Q2.

(2) *Monostable multivibrator Q2 and Q3.* Multivibrator Q2 and Q3 is a monostable (one-shot) multivibrator, with Q2 normally cut off and Q3 normally conducting. Resistor R8 draws sufficient current through the base of Q3, turning Q3 on. Approximately -30 volts appears at the collector of Q3, and no base current is drawn from Q2; therefore, transistor Q2 is cut off. Diode CR3 drops half the signal voltage when it is applied to Q3 which provides protection for this stage. Resistors R5 and R9 are collector load resistors of Q2 and Q3, respectively. This first negative pulse at the base of Q3 will cut off Q3. With Q3 cut off, Q2 will begin conducting and the collector of Q2 will

drop from 0 to about 30 volts. Transistor Q3 will be held in the cutoff state until capacitor C2 charges to the new voltage through resistor R8, which occurs in approximately 35 μsec. A positive gate, approximately 60 psec in duration, is developed at the collector of Q3 and applied to diode CR4.

(3) *Constant current generator Q4.* Constant current generator Q4 allows capacitor C3 to develop a linear ramp. When transistor Q3 is conducting, diode CR4 provides a path for -30 volts to capacitor C3. When Q3 is cut off, the positive gate at its collector will back-bias CR4, and allow C3 to charge toward ground through Q4 and resistor R11. Zener diode CR6 maintains the base of Q4 at a constant voltage and, therefore, provides constant current through R11, Q4, and C3 throughout the charge time of C3. Since the charge current does not decrease with time, the ramp produced is linear rather than exponential. Diode CR5 provides temperature compensation to the voltage regulator circuit. The voltage drop across resistor R12 places a 2-volt step on the leading edge of the ramp. The resulting positive-going linear ramp at the collector of Q4 is direct-coupled to emitter follower Q5.

(4) *Emitter follower Q5.* Emitter follower Q5 prevents level detectors Q6 and Q16 from shunting the charge current of C3 and impairing the linearity of the ramp. The linear ramp from constant current generator Q4 is applied to the base of Q5, causing Q5 to conduct. The ramp developed at the emitter of Q5 is applied to the base of Q6 through resistors R13 and R16, and P2 DELAY ADJ control R15. Also, the ramp is applied to the base of Q16 *(e(1)* below) through resistors R13 and R42 and CP DELAY ADJ control R43.

d. P2 Pulse Generator Circuits (Chassis Series No. 1300). The P2 pulse generator circuits are contained in the pulse generator processor. These circuits produce the isls (P2) pulse that is transmitted with the coded pulse pair to accomplish isls action. Functional operation of the P2 pulse generating circuits is described in (1) through (7) below. A schematic diagram of the pulse generator processor is shown in figure FO12.

(1) Level detector Q6. When emitter follower Q5 is near cutoff, very little current is provided through resistors R14 and R16 and P2 DELAY ADJ control R15. The small amount of current present, passes through the relatively low impedance of CR7 and CR8 and level detector Q6 is cut off. As the voltage rises during the development of the ramp, CR7 and CR8 continue to shunt the current until tunnel diode CR7 is moved into the negative resistance region. The continued increase in ramp voltage decreases the current through CR7 (negative resistance). The current, no longer shunted out, now flows through the base of Q6, and Q6 is turned on. The point in time (along the ramp) at which this occurs is determined by P2 DELAY ADJ control R15. A negative pulse is produced at the collector of Q6, delayed from the start of the ramp to the pick-off point as determined by the setting of R15. Resistor R17 provides a load for the collector of Q6. Diode CR8 provides current temperature compensation for CR7.

(2) *Inverter Q7.* The negative pulse from the collector of level detector Q6 is coupled through capacitor C4, developed across resistor R18, and applied to the base of inverter Q7. The positive pulse at the collector of Q7 is applied to diode CR12 and switch Q12. Resistor R19 provides a load for the collector of Q7. Diode CR9 protects the base-to-emitter junction of Q7 from excessive signal swing.

(3) *Ramp generator Q8.* The positive pulse from the collector of inverter Q7 back-bias is diode CR12, permitting capacitor C5 to charge through resistor R22, P2 PULSE WIDTH ADJ control R21, and diode CR11 to the 11 volts established by Zener diode CR10. The time constant for the charge circuit is adjusted by R21. Adjustment of R21 varies the steepness of the leading edge of the ramp voltage developed by C5. The emitter of ramp generator Q8 starts going positive with the ramp voltage when C5 begins to charge. Capacitor C6 couples the positive-going voltage from the emitter of Q8 to the cathode of CR11, back-biasing CR11. Back-biased CR11 disconnects R21 from the 11-volt supply of CR10. Since the amplitude of the ramp coupled to the cathode of CR11 is nearly equal to the amplitude of the ramp signal on CR5, the dc voltage (difference in dc level of the two ramps) remains near 11 volts, the charge current is nearly constant, and a linear ramp is produced. Capacitor C5 discharges when Q7 again conducts, terminating the ramp. A linear increasing ramp voltage is produced at the emitter of Q8.

(4) *Schmitt trigger generator Q9 and Q10.* The ramp voltage from the emitter of ramp generator Q8 is routed through resistor R23, developed across resistor R24, and applied to the base of transistor Q9. The bias established for transistor Q10 by resistors R25, R27, and R28 normally, permits Q10 to conduct. The conduction of Q10 develops a bias voltage across resistor R26 to hold Q9 cut off. As soon as the ramp voltage applied to the base of Q9 overcomes the bias level, Q9 conducts. The negative pulse developed at the collector of Q9 is coupled to the base of Q10 through capacitor C7, cutting off Q10. The positive pulse developed at the collector of Q10 is applied to emitter follower Q11 through resistor R30. Resistor R29 provides a load for the collector of Q10. The point in time at which the ramp turns Q9 on and produces the pulse output from Q10 is determined by the slope of the ramp. Ramp slope is adjusted by P2 PULSE WIDTH ADJ control R21.

(5) *Emitter follower Q11*. The positive pulse from transistor Q10 is coupled through emitter follower Q11 and capacitor C9 to the gate of silicon-controlled switch CR14. Resistor R31 provides a load for the emitter of Q1l.

(6) Switch Q12. The positive pulse from the collector of inverter Q7 is applied to the base of switch Q12 through resistor R33. The negative pulse at the collector of Q12 is inverted through transformer T1 and the resultant positive signal at pin 6 of T1 is applied to the gate of silicon-controlled switch CR16. Diode CR15 absorbs the negative overshoot at the trailing edge of the pulse to prevent distortion of the output signal from the next stage. Transformer coupling is used to isolate Q12 from the 250-volt pulse circuitry and to keep the on-gate signal line referenced to the cathode of CR16 during the pulse. Diode CR13 protects Q12 from the negative overshoot when the pulse voltage on T1 collapses Resistor R32 and capacitor C8 form a decoupling network.

(7) *Silicon-controlled switch generator CR14 and CR16.* When silicon-controlled switch CR16 is gated-on by the positive pulse applied to its gate, the full anode potential of CR16 is coupled through diode CR18 and dropped across resistor R37. This voltage drop across R37 develops the leading edge of the P2 pulse. The discharge of capacitorC10holdsCR16onuntil silicon-controlled switch CR14 is gated on. The positive pulse from emitter follower Q11 is developed across resistor R34 and applied to the gate of CR14. This positive pulse gates CR14 on, shorting the anode supply of CR16 to ground. When the anode voltage is removed, CR16 ceases to conduct, causing a sharp drop in the voltage across R37. This sharp voltage drop creates the trailing edge of the P2 pulse. When C10 is discharged through CR14, the holding current supplied to CR14 is limited by resistor R36 to a point below the minimum holding current requirements, causing CR14 to cut off, and the circuit returns to its initial state. Resistor R35 also acts as a current limiter. Diode CR17 clamps the junction of CR15, CR16, and CR18 to ground. The P2 pulse is coupled through capacitor C11 and routed to the RT-264D/UPX-6. The P2 MOD testpoint TP5 is provided for convenient observation of the P2 pulse with an oscilloscope.

e. Control Pulse Generator and Interlock Circuits (Chassis Series No. 1300) and Diplexer Z1201 (Chassis Series No. 1200). The control pulse generator and interlock circuits are contained in the pulse generator processor (chassis series No. 1300). These circuits operate in conjunction with diplexer Z1201 (located on the MD-638/TPX-41 main chassis) to supply the bias level required for beam pattern switching in the antenna system. Functional operation of the pulse generator and interlock circuits and diplexer Z1201 is described in (1) through (9) below. A schematic diagram of the pulse generator processor is shown in figure FO-12.

(1) *Level detector Q16.* When emitter follower Q5 is near cutoff, there is very little current through resistors R14, R42, and CP DELAY ADJ control R43. The remaining current path is through the relatively low impedance of CR20 and CR21, consequently level detector Q16 is cut off. As the voltage rises with the development of the ramp at the output of Q5, CR20 and CR21 continue to shunt the current until tunnel diode CR20 is moved into the negative resistance region. The continued increase in ramp voltage decreases the current through CR20 (negative resistance). The current, no longer shunted out, now flows through the base of Q16, and Q16 is turned on. The point in time (along the ramp) at which this occurs is determined by CP DELAY ADJ control R43. A negative pulse is produced at the collector of Q16, delayed from the

start of the ramp to the pickoff point as determined by the setting of R43. Resistor R44 provides a load for the collector of Q16. Diode CR21 provides current temperature compensation for CR20.

(2) *Inverter Q1 7.* The negative pulse from the collector of level detector Q16 is coupled through capacitor C12, developed across resistor R45, and applied to the base of inverter Q17. The positive pulse at the collector of Q17 is applied to diode CR24 and switch Q22. Resistor R46 provides a load for the collector of Q17. Diode CR22 protects the base-to-emitter junction of Q17 from excessive signal swing.

(3) *Ramp generator Q18.* The positive pulse from the collector of inverter Q17 back-biases diode CR24, permitting capacitor C13 to charge through resistor R47 and diode CR23 to the 11 volts established by Zener diode CR10. The emitter of ramp generator Q18 starts going positive with the ramp voltage when C13 begins to charge. Capacitor C14 couples the positive voltage from the emitter of Q18 to the cathode of CR24, back-biasing CR24. Back-biased CR24 disconnects R47 from the 11-volt supply of CR10. Since the amplitude of the ramp coupled to the cathode of CR24 is nearly equal to the amplitude of the ramp on C13, the dc voltage (difference in dc level of the two ramps) remains near 11 volts, the charge current is nearly constant, and a linear ramp is produced. C13 discharges when Q17 again conducts, terminating the ramp. A linear increasing ramp voltage is produced at the emitter of Q18.

NOTE

In equipment containing a CP WIDTH ADJ control R63, capacitor C13 also charges through resistor R63 to the 11 volts established by CR10. The adjustment of R63 determines the slope of the ramp developed by C13.

(4) *Schmitt trigger generator Q19 and Q20.* The ramp voltage from the emitter of ramp generator Q18 is routed through resistor R48, developed across resistor R49, and applied to the base of transistor Q19. The bias established for transistor Q20 by resistors R50, R52, and R53 normally permits Q20 to conduct. Conduction of Q20 develops a bias voltage across resistor R51 to hold Q19 cut off. As soon as the ramp voltage applied to the base of Q19 overcomes the bias level, Q19 conducts. The negative pulse developed at the collector of Q19 is coupled to the base of Q20 through capacitor C15, cutting off Q20. The positive pulse developed at the collector of Q20 is applied to emitter follower Q21 through resistor R55. Resistor R54 provides a load for the collector of Q20. The point in time at which the ramp turns Q19 on and produces the pulse output from Q20 is determined by the preset slope of the ramp.

(5) *Emitter follower Q21.* The positive pulse from transistor Q20 is coupled through emitter follower Q21 and capacitor C17 to the gate of silicon-controlled switch CR26. Resistor R56 provides a load for the emitter of Q21.

(6) *Switch Q22.* The positive pulse from the collector of inverter Q17 is applied to the base of switch Q22 through resistor R58. The negative pulse at the collector of Q22 is inverted through transformer T6 and the resultant positive signal at pin 6 of T6 is applied to the gate of silicon-controlled switch CR28. Diode CR27 absorbs the negative overshoot at the trailing edge of the pulse to prevent distortion of the signal output of the next stage. Transformer coupling is used to isolate Q22 from the 250-volt pulse circuitry and to keep the on-gate signal line referenced to the cathode of CR28 during the pulse. Diode CR25 protects transistor Q12 from the negative overshoot when the pulse voltage on T6 collapses. Resistor R57 and capacitor C16 form a decoupling network.

(7) *Silicon-controlled switch generator CR26 and CR28.* When silicon-controlled switch CR28 is gated-on by the positive pulse applied to its gate, the full anode potential of CR28 is dropped across the primary of transformer T3. This voltage drop across the primary of T3 develops the leading edge of the control pulse. The discharge of capacitor C18 holds CR28 on until silicon-controlled switch CR26 is gated on. The positive pulse from emitter follower Q21 is developed across resistor R59 and applied to the gate of CR26. The positive pulse gates CR26 on, shorting the anode supply of CR28 to ground. When the anode voltage is removed, CR28 ceases to conduct, causing a sharp drop in the voltage across the primary of T3. This sharp voltage drop creates the trailing edge of the control pulse. When C18 is discharged through CR26, the holding supplied to CR26 is limited by resistor R61 to a point below the minimum holding

current requirements, causing CR26 to cut off and the circuit returns to its initial state. Resistor R60 also acts as a current limiter. Diode CR29 clamps the cathode of CR28 to ground. The control pulse is coupled through T3 and routed to the diplexer (Z1201). Test point TP6 permits observation of the control pulse with an oscilloscope. Capacitor C19 provides filtering to prevent the control pulse from appearing at the collector of transistor Q15.

(8) *DiplexerZ1201.*DiplexerZ1201 combines the train of three RF pulses developed by the RT-264D/UPX-6 with the RF switch bias and the control pulse. The diplexer consists of two sections, a high frequency section consisting of a series of capacitors and a low frequency section consisting of an inductance. The train of three RF pulses is applied to the high frequency section and the RF switch bias, and the control pulse is applied to the low frequency section. The outputs of the two sections are combined at the point where the train of three RF pulses and the RF switch bias and control pulse are mixed. The combined output is routed to the AB-1158/CPA-119.

(9) Interlock circuit Q13, Q14, Q15 and K1. The interlock circuit consisting of transistors Q13, Q14, Q15, and relay K1 provides protection to RF switch S1001 in Antenna AS-1796/GPA-119. RF switch S1001 must be in either the sum or difference condition during RF transmission or serious damage to RF switch S1001 may result. Since the difference condition occurs during the relatively short isls pulse (P2) transmission period, continuous bias current must be provided to maintain the RF switch in the sum condition. The bias current is provided by the -30 volts applied through resistor R40, the secondary of transformer T3, and the control pulse line to S1001. Routing the bias current through R40 also provides the necessary bias to maintain conduction of Q14. With Q14 conducting, a base return for Q15 is established, causing Q15 to conduct. Resistor R38 provides a load for the emitter of Q14. Once the circuit is turned on, Q14 and Q15 complement each other and the conduction level of both transistors is only limited by the resistance in series with their respective conduction paths. When Q15 is conducting, the voltage drop across resistor R41 is sufficient to cause a difference of potential across Zener diode CR19 great enough to break down CR19. When CR19 breaks down, base current is supplied to transistor Q13 through CR19 and 2-48 resistor R39. The base current turns Q13 on and the total emitter voltage of -30 volts is supplied to energize interlock relay K1. Diode CR1 damps out any voltage spikes that might be generated in the relay solenoid circuit. Resistor R1 acts as a current limiter. When K1 is energized, a path is provided for the coded-pair from the KY-97C/TPX. If the bias current to RF switch S1001 in Antenna AS-1796/GPN-119 is interrupted due to a short or open on the line, the forward bias for the transistors in the interlock circuit is removed and K1 deenergizes. This interrupts the coded-pair, removing the RF from S1001. The BIAS ON lamp DS1 indicates when K1 is energized. Transformer T3 adds the 55-volt peak control pulse to the bias line during the period in which the isls pulse (P2) is transmitted. Since nearly 10 volts is dropped across R40, the bias voltage swings from approximately -20 volts to +35 volts during the control pulse time.

2-17. Receiver-Transmitter, Radio RT-264D/UPX-6

Receiver-Transmitter, Radio RT-264D/UPX-6 contains the circuitry of the transmitting system (para 2-5) and the receiving system (para 2-7). For detailed analysis of the circuits contained within the RT-264D/UPX-6, refer to TM 11-5895-245-35.

2-18. Pedestal, Antenna AB-1158/GPA-119

a. General. Pedestal, Antenna AB-1158/GPA-119 is part of the antenna system described in paragraph 2-6. The principle components which provide antenna drive, rotary coupling, and synchro data transmission are contained in the AB-1158/GPA-119. Functional operation of the circuits in the AB-1158/GPA-119 is described in *b* through *d* below. A schematic diagram of the AB-1158/GPA-119 is shown in figure FO-13.

b. Antenna Drive. Antenna drive is provided by antenna drive motor B20002 which is mechanically linked to the antenna drive shaft through a reduction gear train assembly. Antenna drive voltage, consisting of single-phase, 117-volt, 50/60-Hzpower is applied to the AB-1158/GPA-119 at pins H and J of connector P20004. The drive voltage is applied through current sensing relay K20001 to pin A of drive

motor connector J20001. On application of 117-volt, 50/60-Hz power, the motor draws maximum current and the start winding produces the torque required to start the motor. During this high current condition, K20001 is energized connecting capacitors C1 and C2 in parallel with the motor start winding. As B20002 approaches its running speed, current through the motor start winding decreases to a level that allows current sensing relay K20001 to deenergize. When K20001 deenergizes 117-volt, 50/60-Hz power is applied to capacitor C2 in parallel with the motor run winding. Pins A and B of connector P20001 are connected to the run winding of antenna drive motor B20002 to provide the running torque required to drive the IFF antenna at a constant 15 rpm rate. Pins C and D of connector J20001 provide ac common connections for the motor starts and run windings.

c. Rotary Coupling. Rotary joint E20001 provides the means of transferring RF energy and control signals from the stationary cable to rotating IFF antenna E1001. Rotary joint E20001 differs from conventional rotary joints in that it is dc contacting. Electrical continuity (dc) is provided between the stationary and rotary sections of the joint to provide a method of coupling the dc bias (switch command signal) to rotating RF switch S1001.

d. Synchro Data Transmission. Synchro data transmission is accomplished by synchro transmitter B20001. The stator of control transmitter B20001 has three windings (S1, S2, and S3) physically displaced 120 degrees apart. The rotor has one rotatable winding mechanically linked to the IFF antenna at a 1:1 ratio. Excitation voltage for the rotor consists of 117-volt, 50/60-Hz power, applied to the rotor at terminals R1 and R2 from pins E and D respectively of connector J20004. The amplitude of the voltages at S1, S2 and S3 is determined by the angular position of the rotor windings in respect to the synchro rotor winding. This data, available at B20001, terminals S1, S2, and S3 is routed out of the AB-1158/GPA-119 at pins A, B, and C of connector J20004. This output is applied to the indicator of the associated radar as an error signal. The error is translated into antenna position data and used to synchronize the IFF sweep with antenna rotation.

2-19 Antenna AS-1796/GPA-119

a. General. AntennaAS-1796/GPA-119is part of the antenna system described in paragraph 2-6. The elements that provide propagation and reception of RF energy and beam pattern switching for isls operation are contained within the AS-1796/GPA-119. Functional operation of the elements and circuits contained in the AS-1796/GPA-119 is described in *b* through *e* below. A schematic diagram of the AS-1796/GPA-119 is shown in figure FO-14.

b. RF Switch S1001. RF switch S1001 consists of diplexer Z1101, microwave switch S1101, a pulse shaper, and filters FL1101 and FL1102. RF switch S1001 provides rapid switching of the incoming transmitter signal to either the sum (ARM 1) or difference (ARM 4) ports of bar hybrid HY1001 as instructed by a switch command generated by the MD-638/TPX-41. The switch command is active only during the second pulse period. At this time, the transmitter power is connected to the difference port of HY1001. At all other times, including nontransmitting times, S1001 is connected to the sum port.

(1) Diplexer Z1101. The transmitter output signal and the switch command signal (control pulse) are combined in the MD-638/TPX-41 and coupled through the rotary joint to diplexer Z1101. Diplexer Z1101 separates the two signals, routing the switch command to the pulse shaper and the transmitter output to S1101.

(2) *Pulse shaper.* The pulse shaper consists of two rc networks used to restore the received control pulse; one network shapes positive pulses and the other, negative pulses. The positive shaper consists of capacitor C1102 and resistor R1103. The negative shaper consists of capacitor C1101, and resistors R1101 and R1102. In the positive shaper, C1102 begins charging as the received control pulse is applied from diplexer Z1101. The resultant output of the positive pulse shaper is a pulse 1.2 usec in duration with a rise time of 0.2 , usec, for application to microwave switch S1101. The negative shaper functions in the same manner as the positive shaper.

(3) *Microwave switch S1101.* Microwave switch S1101 performs the actual switching function of RF switch S1001.Operation is controlled by the switch command signal which is positive during the second pulse period (difference condition) and negative at all other times. A -20-volt dc bias voltage originating in the MD-638/TPX-41 is applied to S1101. If this bias voltage is removed, S1101 will fail to maintain S1001 in the proper condition (para 2-22). In operation, S1101 presents a high impedance to the open channel and provides a low insertion loss path for the selected channel.

(4) *Filters F1101 and F1102.* Filters F1101 and F1102 on switch S1101 output line attenuate all signals in the 1280 to 11, 000-MHz range by 50 db minimum isolation, and pass the 1030 MHz (transmit) and 1090 MHz (receive) signals by 1 db maximum insertion loss. This placement of the filters prevents possible switch burnout caused by radiation from very high-power adjacent radars.

c. Coupling Subsystem. The coupling subsystem consists of directional coupler DC1001 and bar hybrid HY1001. This subsystem acts as a link between IFF antenna E1001, backfill reflector E1002, and RF switch S1001.

(1) Directional coupler DC1001. Directional coupler DC1001 is an RF directional coupler which channels the transmitter output signals to IFF antenna E1001 and backfill reflector E1002 during the propagation of the difference pattern (second pulse period). Directional coupler DC1001 provides a signal to E1002 6 db below the signal provided to E1001.

(2) Bar hybrid HY1001. Balanced bar hybrid HY1001 performs the power dividing and phase shifting functions necessary to obtain the sum and difference pattern outputs from E 1001. Transmitter power applied to the sum port of HY1001causes an in-phase signal to be coupled to the two antenna feed cables. Upon receipt of the transmitter output signal at the difference port, HY1001 splits the signal, phase shifts one signal 180 degrees, and then applies the shifted signal to one port and the unshifted signal to the other port.

d. IFF Antenna E1001. IFF antenna E1001 is a dual aperture, longitudinal shunt, slot array antenna designed to transmit and receive L-band signals (1030 MHz transmit and 1090 MHz receive). IFF antenna E1001 consists of two independent radiating elements divided by a metal wall. When in-phase signals are coupled to the antenna feed cables, the radiating element functions as an integral element and the antenna propagates a conventional radiating pattern with the power concentrated at beam center (sum pattern). When the inputs to the antenna are not in-phase, the septum isolates the two radiating elements and causes the propagation of a pattern with a deep null at beam center (difference pattern).

(1) The sum pattern is transmitted at 1030 MHz and is a vertically polarized, 8 degree azimuth beam width (at 3-db point) signal. IFF antenna E1001 is tilted 10 degrees in the elevation plane and has an elevation beam width of 45 degrees (at 3-db point). The side-lobe level of the sum pattern is a minimum of 23 db below the main lobe of the sum pattern.

(2) The difference pattern is also transmitted at 1030 MHz and has the same polarization and elevation beam width as the sum pattern, The null depth of the difference pattern, when measured at boresight (center of the main sum lobe) with respect to the sum pattern main lobe is a minimum of 25 db.

e. Backfill Reflector E1002. Backfill reflector E1002 transmits a portion of the difference pattern in the back-direction, the hemisphere 180 degrees behind the normal line of propagation of IFF antenna E1001. This transmission provides sufficient suppression pulse power in the back-direction to prevent nearby reflections of the sum pattern from causing spurious responses from aircraft transponders in the rear hemisphere of IFF antenna E1001. The amount of power propagated by backfill reflection is affected by local environmental conditions, and is regulated by the attenuation of directional coupler DC1001.

2-20. Decoder, Video KY-593/TPX-44

Decoder, Video KY-593/TPX-44 contains the principle circuits of the decoding system described in paragraph 2-9). For detailed analysis of the circuits contained within KY-593/TPX-44, refer to TM 11-5840-309-35.

2-21. Control, Remote Switching C-7014/TPX-44 Control, Remote Switching C-7014/TPX-44 contains the switching and control circuits that provide the primary control functions of the decoding system described in paragraph 2-9. For detailed circuit analysis of circuits contained withinC-7014/TPX-44,refertoTM 11-5840-309-35.

2-22. Simulator, Radar Signal SM-472/TPX-44 Simulator,RadarSignalSM-472/TPX-44 contains circuits of the simulating system described in paragraph 2-10. For detailed analysis of circuits contained within the SM-472/TPX-44, refer to TM 11-5840-326-35.

2-23. Interconnecting Box J-2945/TPX-41

a. General .Interconnecting Box J-2945/TPX-41 contains the principle switching and control circuits of the power distribution system described in paragraph 2-11. Functional operation of circuits contained within the J-2945/TPX-41 is described in *b* through d below. A schematic diagram of the J-2945/TPX-41 is shown in figure FO-15.

b. System Power Application. 117-volt, 50/60-Hz primary power is applied to Interconnecting Box J-2945/TPX-41 at connector J8603, pin A. Chassis ground is connected to pin C of J8603 and ac common is connected to pin B. When IFF POWER circuit breaker CB8601 is placed to the ON position, 117-volt, 50/60-Hz power is applied to terminals 4, 5 and 6 of terminal board TB8601. These connections provide power distribution to the following major components of the AN/TPX-41:

(1) Receiver-Transmitter, Radio RT-264D/UPX-6 receives 117-volt, 50/60-Hz power across terminals 5 and 7 of TB8601.

(2) Coder-Control KY-97C/TPX receives 117-volt, 50/60-Hz power across terminals 5 and 7 of TB8601.

(3) Modulator,PulseMD-638/TPX-41 receives 117-volt, 50/60-Hz power across terminals 5 and 7 of TB8601.

(4) DemultiplexerTD-99/Greceives 117-volt, 50/60-Hz power across pins A and B of connector J8601. Pin A of J8601 is connected to terminal 4 of TB8601 and pin B of J8601 is connected to terminal 8 of TB8601.

(5) Blanker, Interference MX-8795/TPX-41 receives 117-volt, 50/60-Hz power across pins A and B of connector J8602. Pin A of J8602 is directly connected to terminal 4 of TB8601 and pin B of J8602 is connected to terminal 9 of TB8601.

c. Antenna Power Application. The ac common for antenna drive (para *2-18b)* is connected to pin J of connector J8601 as an output from J-2945/TPX-41.Antennadrivevoltage, consisting of 117-volt, 50/60-Hz power is taken from terminal 6 of TB8601 and applied to a contacts Al and B1 of IFF SCAN relay K8601. Positive energizing voltage for K8601 is supplied by an external source and applied to pin C of J8601. When SCAN switch S8601 is placed to the ON position, +28 volts is applied to the OPERATE contact of IFF SCAN switch S8602. Positive 28 volts from a remote SCAN switch may also be applied to the OPERATE contact of IFF SCAN switch S8602 through pin G of connector J8601. As long as IFF SCAN switch S8602 remains in the SAFE position, IFF SCAN relay K8601 cannot be energized and no antenna drive voltage is routed out of the J-2945/TPX-41. When IFF SCAN switch S8602 is placed in the OPERATE position, K8601 energizes, and 117-volt, 50/60-Hz power is routed out of the J-2945/TPX-41 at pin H and J of connector J8601 as antenna drive voltage.

d. Bypass Interconnection. The straight-through connections in the J-2945/TPX-41 between J8601-F and J-8602-C, and J8601-D and J8602-D may be used for interconnection of a remote bypass switch (para 2-13e(15)).

CHAPTER 3
DIRECT SUPPORT MAINTENANCE

Section I. General

3-1. Scope of Direct Support Maintenance

The specific maintenance duties of the direct support maintenance repairman are listed in *a* through *d* below with references to the paragraphs covering the specific maintenance function. Ideally, the performance of these duties will entail only those maintenance operations designated specifically for direct support maintenance. However, some minor equipment problems which are correctable at the lower levels of maintenance may be referred to direct support maintenance due to the difficulty involved in identifying the problem. For this reason, the maintenance duties of the direct support maintenance repairman also include the maintenance responsibilities of the operator and organizational maintenance repairman described in TM 11-5895-479-12.

a. Troubleshooting (para 3-3).

b. Adjustment and alignment (para 3-13).

c. Repair (para 3-28).

d. Removal and replacement (para 3-33).

3-2. Tools, Test Equipment, and Materials Required

a. Tools. Tools required for direct support maintenance are listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

b. Test Equipment. Test equipment required for direct support maintenance is listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

c. Materials. The applicable repair parts allocated for direct support maintenance are listed in TM 11-5895-479-35P.

Section II. DIRECT SUPPORT TROUBLESHOOTING

3-3. General

This section contains pertinent data to aid the direct support repairman in the rapid identification and correction of equipment malfunctions.

Specific types of data that serve as effective troubleshooting aids are listed in *a* through i below with references to the paragraphs covering the specific data subjects.

a. Troubleshooting techniques (para 3-4).

b. Identification of intermittents (para 3-5).

c. Diagrams (para 3-6).

d. Reference designations (para 3-7).

e. Voltage and resistance measurements (para 3-8).

f. Parts substitution (para 3-9).

g. Waveform Analysis (para 3-10).

h. System troubleshooting chart (para 3-11).

i. Major component troubleshooting (para 3-12).

3-4. Troubleshooting Techniques

a. General. Effective troubleshooting must be systematic. It is seldom possible to observe a symptom of trouble and immediately diagnose the cause. Generally, it will be necessary to perform a sequence of operational checks, observations, and measurements before the cause of trouble is revealed. If the proper sequence is followed, the trouble will be traced first to a system or a component, then to a portion of the system or component, and finally to the defective part. The sequence of steps is referred to commonly as sectionalization, localization, and isolation of trouble. The repairman can obtain helpful information by questioning organizational maintenance personnel, by reading the complaint notice attached to the equipment, and by reading the equipment log. The more information the repairman can gather, the more accurate his diagnosis will be and the sooner repairs can be made.

b. Sectionalization. Sectionalization consists of determining which major component or section of the overall system contains the trouble. The first evidence of an equipment malfunction is usually identified when the equipment fails to perform normally during actual operation. The initial identification of an equipment problem is usually accomplished by the operator. The operator should ensure that the problem is not due to misadjusted controls and attempt to further identify the problem through various simple checks and inspections. The first stage of sectionalization usually occurs at the organizational maintenance level. Since this level of maintenance has access to only a limited amount of test equipment, maximum use must be made of visual indications obtained from the radar ppi and equipment indicating devices. The organizational troubleshooting chart in TM 11-5895-479-12 provides an aid to repairman in the identification of troubles through the use of ppi presentation and equipment indicators. When a problem cannot be identified through the use of these indicators, sectionalization may be required at the direct support level. The system troubleshooting chart, contained in paragraph 3-11, provides an aid to the direct support repairman in the sectionalization of equipment troubles.

c. Localization. Localization consists of tracing a trouble to a specific location (circuit card, IF strip, power supply, etc.) within a major component of the system. Once a problem has been sectionalized to a major component, the trouble must be localized. The system troubleshooting chart (para 3-11) references applicable major component troubleshooting charts or technical manuals that provide information for localizing equipment troubles.

d. Isolation. Isolation consists of determining which specific part or parts is the cause of the trouble. After trouble has been localized to a portion of a major component, use visual inspection, waveform analysis (para 3-10), voltage and resistance measurements (para 3-8), and parts substitution (para 3-9) to determine the defective part.

3-5. Identification of Intermittents

a. If the operation of a component is intermittently faulty, the trouble may be difficult to locate when the component is functioning normally. Such troubles can often be found by lightly tapping each part in the suspected stage or portion of the component with a nonmetallic pencil or insulated rod and, at the same time, watching the associated radar ppi screen. Lightly tap all of the parts including transistors and wiring. If the scope presentation remains normal, repeat the tapping process at adjoining stages until the normal indications change.

b. Intermittent operation can be caused by loose connections, broken wires or parts with internal defects. Sometimes intermittent trouble can be located by observing erratic behavior of one of the controls.

3-6. Diagrams

The various types of diagrams contained within this manual and TM 11-5895-479-12 will serve as an invaluable aid in troubleshooting. The purposes and specific applications of these diagrams are described in *a* through i below.

a. Block Diagrams. The troubleshooting block diagram, contained in TM 11-5895-479-12, depicts the electrical and mechanical interrelationships among the systems, components, and stages of the AN/TPX-41. By observing the

symptoms and reasoning possible causes, it is often possible to trace the cause of faulty operation to trouble in a particular block.

b. Cabling Diagrams. These diagrams, contained in TM 11-5895-479-12, show the cabling between components of the AN/TPX-41 and the associated equipment. This type of diagram can be used to check the cabling.

c. Interconnection Diagram. The diagram shows all of the interconnections between components of the AN/TPX-41 and the associated radar set and remoting equipment. It shows the wiring between receptacles in one component and receptacles in another component. The diagram is especially useful for tracing trouble between components.

d. Complete Schematic Diagrams. A complete schematic diagram is provided for each major component. The schematic diagram shows all of the circuitry in the component and can be used to determine the faulty part in a particular component.

e. Voltage and Resistance Charts. Voltage and resistance charts are provided for the timing, defruiting, and isls systems. These charts provide normal voltage and resistance measurements at all transistor and diode connections and give normal resistance measurements at all switches and relays in the AN/TPX-41. They are helpful when making voltage and/or resistance measurements to trace the fault to a specific part. When using these charts, carefully read the text and duplicate the conditions exactly under which the readings were obtained.

Waveform Illustrations. Simplified drawings are provided of actual waveforms present at significant points in the circuits of the timing, defruiting, and isls systems. A departure from the normal waveform indicates trouble between the point at which the normal waveform is observed and the point at which the abnormal waveform is observed.

g. Resistor and Capacitor Color Code Diagram. The resistor and capacitor color code diagram (fig. FO-1) enables the repairman to estimate the approximate values of military standard resistors and capacitors from the color bands or dots painted on them. The diagram is most useful when trouble within a component is traced to a particular resistor or capacitor.

h. Parts Location Illustrations. Parts location illustrations aid the repairman in locating the various components and parts of the equipment to be aligned, tested, removed, replaced, adjusted, or repaired. Parts location illustrations are also an aid to the repairman when troubleshooting equipment and/or checking equipment performance.

i. Wiring Diagrams. Wiring diagrams show all wire connections between discrete components of the major components in the AN/TPX-41. These diagrams are especially useful when tracing trouble between components of suspected integral subassembles.

3-7. Reference Designations

a. General. To aid in parts location, a block of reference designation numbers is assigned to each major component of the AN/TPX-41. *For example,* all parts in Coder-Control KY-97C/TPX are numbered from 401 to 460; that is, resistors in this component are designated R401, R402, etc., and capacitors are designated C401, C402, etc. The following chart lists the block of reference designation numbers assigned to each major component.

b. Block Reference Designation Numbers.

Reference designation numbers	*Components*
1 -99----------	Simulator, Radar Signal SM-472/TPX-44
201-263----------	Decoder, Video KY-593/TPX-44
30001-30052----------	Video amplifier (part of KY-593/TPX-44)
30101-30157----------	Coincidence amplifier (part of KY-593/TPX-44)
30201-30247----------	Ident-emergency generator (part of KY-593/TPX-44)
30301-30339----------	Video mixer (part of KY-593/TPX-44)
101-179----------	Receiver-Transmitter, Radio RT-264D/UPX-6

Reference designation numbers	*Components*
201-277	Receiver-Transmitter, Radio RT-264D/UPX-6
301-370----------	Receiver-Transmitter, Radio RT-264D/UPX-6
401-460----------	Coder-Control KY-97C/TPX
731-734----------	Control, Remote Switching C-1271A/TPX-22
1001-1099----------	Antenna AS-1796/GPA-119
1101-1199----------	RF Switch (part of AS-1796/GPA-119)
1201-1299----------	Modulator, Pulse MD-638/TPX-41
1301-1399----------	Pulse generator processor (part of MD-638/TPX41)
8601-8699----------	Interconnecting Box J-2945/TPX-41
20001-20099----------	Pedestal, Antenna AB-1158/GPA-119
31101-31199----------	Blanker, Interference MX-8795/TPX-44
30801-30899----------	Processor (part of MX-8795/TPX-44
30901-30999----------	Trigger/gate generator (part of MX -8795/TPX-44)
31001-31099----------	Synchronizer-Multiplier (part of MX -8795/TPX-44)
40301-40307----------	Control, Remote Switching C-7014/TPX-44

3-8. Voltage and Resistance Measurements

a. Voltage and resistance measurements aid in determining circuit conditions and in evaluating symptoms in the course of troubleshooting. Multimeter ME-26B/U should be used to measure these quantities. Detailed instructions for operating theME-26B/U are contained in TM 11-6625-200-15. Pertinent voltage and resistance data is contained in TM 11-5895-245-35 for the receiving, transmitting, and RF systems; in TM 11-5895-201-35 for the coding system; in TM 11-5840-309-35 for the decoding system; and in TM 11-5840-326-35 for the simulating system.

b. Compare the measured values of voltage and resistance with the normal values given in the voltage and resistance charts. When making resistance measurements at transistor pins or other test points connected to crystal diode circuits, the ME-26B/U lead connections will determine whether the forward or backward resistance of the diode is included in the resistance reading.

c. The resistance characteristics of the various silicon and germanium crystal diodes located in the AN/TPX-41 may be checked with the ME-26B/U. The failure of a crystal diode in a circuit is not always easily discovered during routine troubleshooting procedures. However, if it is suspected that operational difficulties are caused by one of these diodes, disconnect the leads (be sure to dissipate excessive heat with a pair of pliers or other suitable tool when unsoldering diode leads), and check the resistance characteristics. The forward resistance of all crystal diodes should not be greater than 0.5K (500 ohms). When checking the backward resistance of the crystal diodes, a reading close to infinity should be observed. When checking diodes, the ME-26B/U should not be used on any ohms scale less than RX100.

d. When measuring voltages on the AN/TPX41, insulate the entire test probe except for the extreme tip, with tape or sleeving, since a momentary short will damage the transistors.

NOTE

The characteristics of transistors may cause the emitter and base voltage readings to vary somewhat from one transistor to another in the same circuit without affecting operation. Collector voltages of transistors should be relatively stable.

e. Before taking any resistance measurements, ensure that all ac power is removed from the AN/TPX-41.Also,removeeachplug-in subassembly from suspected components in the AN/TPX-41 before any resistance checks are attempted. Insulate the ME-26B/U test leads *(d* above) and check the applicable resistance chart for meter scale settings. To protect the transistor, never connect the ME-26B/U until it has been verified that the proper meter scale is selected.

3-9. Parts Substitution

a. Do not substitute parts indiscriminately. Substitute only when *all* of the following conditions are satisfied:

(1) The trouble has been isolated to a specific stage.

(2) All voltage readings are normal.

(3) All resistance readings are normal.

(4) The transistor has been replaced.

b. Types of trouble that would satisfy all of the above conditions are-open bypass or coupling capacitors, capacitors that have changed value, and an interstage transformer with shorted turns.

c. When an *open* capacitor is suspected, connect a known good capacitor of equal value across the capacitor and check the operation of the component.

d. When all other possibilities of trouble are ruled out, substitute a good part for the one suspected of being defective.

e. A type of defective component that may not be uncovered by the above procedures may be a capacitor that has changed value.

3-10. Waveform Analysis

a. General. Waveform illustrations contained in this manual show typical waveforms taken at jacks, testpoints, and other significant points throughout the AN/TPX-41 system. Through applied troubleshooting and testing techniques, the absence or presence of these waveforms at various points throughout the IFF system, may be used to analyze system performance and determine trouble sources. The waveforms shown in figure 3-1 are related directly to the system troubleshooting chart (para 3-11). These waveforms consist of significant input and output signals that are connected between the major components of the AN/TPX-41. When used in conjunction with the system troubleshooting chart, these waveforms should be an invaluable aid in trouble sectionalization. The waveforms shown in figure 3-3 are related to the Modulator, Pulse MD-638/TPX-41 troubleshooting charts and the waveforms shown in figure 3-2 are related to the Blanker, Interference MX-8795/TPX-41 troubleshooting charts. These waveforms will aid the repairman in the localization and isolation of troubles within the MD-638/TPX-41 and MX-8795/TPX-41. Test equipment required for the observation of waveforms consists of Oscilloscope AN/USM-140B and Delay Generator MX-2962/USM. General instructions for preparing the test equipment for use and making test connections are given in b and c below. For detailed instructions covering the operation of the AN/USM-140B and MX-2962/USM, refer to TM 11-6625-535-15-1. Waveform observation and the various conclusions that can be drawn from indications obtained are given in d below.

b. Preparing the Oscilloscope for Use. Prepare the AN/USM-140B and MX-2962/USM for use as follows:

(1) Turn INTENSITY control fully ccw.

(2) Connect oscilloscope to 117-volt power source and place POWER switch to ON. Allow 5 minutes warm-up.

(3) Set HORIZONTAL DISPLAY switch to X1; VERNIER control to CAL.

(4) Set SWEEP TIME switch to .5 MILLISECONDS/CM; VERNIER control to CAL.

(5) Set SWEEP MODE control to PRESET; TRIGGER SOURCE switch to INT.

(6) or operation without delay function, place SWEEP SELECTOR on MX-2962/USM to MAIN SWEEP. For operation with delay function, refer to instructions in TM 11-6625-535-15-1 to attain desired results.

(7) Connect test probe BNC terminal to CHANNEL A INPUT connector.

(8) Place vertical presentation switch to CHANNEL A..

(9) Place CHANNEL A SENSITIVITY switch to .05 (VOLTS/CM).

(10) Place CALIBRATOR switch to 2.

(11) Connect test probe tip to CALIBRATOR VOLTS connector.

(12) Rotate INTENSITY control cw until trace appears. If CRT remains blank, press BEAM FINDER pushbutton.

(13) Adjust HORIZONTAL POSITION and CHANNEL A VERTICAL POSITION controls until trace is centered on screen. If necessary, readjust INTENSITY.

(14) Adjust FOCUS and ASTIGMATISM controls to obtain thin trace.

(15) Loosen knurled locknut behind rear flange on probe.

(16) Holding vinyl sheath behind locknut, rotate rear flange to obtain best square wave. Check that vertical deflection is 4 cm (corresponding to 0.05 volt/cm sensitivity with 2-volt calibrator output and 10:1 attenuation in probe).

(17) Tighten probe locknut without changing adjustment.

(18) Rotate vertical presentation switch to CHANNEL B. Repeat procedure of steps (9) through (17) above for channel B and other test probe.

(19) Repeat procedure with vertical presentation switch placed to ALTERNATE and with both probes connected to calibrator (one driving channel A and one driving channel B) to test both channels simultaneously.

(21) Follow instructions in c below to connect AN/USM-140B to desired point of test.

c. Connecting the Oscilloscope. The AN/USM-140B is supplied with the MX-2817/U test probe for connection to testpoints. To use the MX-2817/U, connect the test probe BNC terminal to the CHANNEL A INPUT or CHANNEL B INPUT connector on the AN/USM-140B and connect the test probe tip to the desired testpoint. For the waveforms shown in figure 3-1 a standard test cable, fabricated from a 6-foot length of RG-59/U and 2 BNC connectors, should be used. To use this cable, connect one end to the CHANNEL A INPUT or CHANNEL B INPUT connector on the AN/USM-140B. At the test point, disconnect the equipment cable connector and connect the other end of the test cable. After observing waveforms, reconnect equipment cabling.

d. Waveform Observation. Before comparison between waveforms obtained and normal waveforms as shown in the illustrations, carefully read the notes on the waveform illustrations and exactly duplicate the conditions under which the normal waveforms were obtained. A departure from the normal waveform indicates trouble between the point at which a normal waveform is observed at the input of a stage and an abnormal waveform at the output of the same stage. The condition indicates the trouble is in that stage. When trouble is indicated in a stage, take voltage and resistance measurements at the transistor pins (para 3-8).

3-11. System Troubleshooting Chart

The primary purpose of the system troubleshooting chart (below) is to aid repairman in the sectionalization (para 3-4b) of equipment troubles. The trouble symptom column contains abnormal indications that may appear during equipment turn-on or actual operation. The probable trouble, checks, and corrective measures column indicates the probable cause for a specific symptom and gives applicable checks and corrective measures to correct the fault. Items 1 through 10 in the system troubleshooting chart list troubles directly related to the application of power. Checks and corrective measures for these troubles are given on the basis that all related cables, cabling, fuses, and indicator lamps were checked at the lower levels of maintenance. Prior to troubleshooting, make preliminary control settings and perform the starting procedure as instructed in TM 11-5895-479-12.

CAUTION

If burned or overheated components are observed or a pungent, burning odor is detected, remove power immediately and check for shorts. Equipment damage may result from continued operation.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
1	0n Interconnecting J-2945/TPX-41, when IFF POWER switch is placed to ON, SCAN switch is placed to ON, and IFF SCAN switch is placed to OPERATE, Antenna AS-1796/ GPA-119 does not rotate	Box On Pedestal Antenna AB-1158/GPA-119, disconnect connector P20004 and use Multimeter ME-26B/U to check for 117 vac across pins J and G of P20003. *a.* If voltage is present, trouble is in antenna system. Refer to para 3-12f(3). *b.* If voltage is not present, trouble may be in J-2945/TPX-41. Refer to para 3-12j(2).
2	0 n Modu1ator, Pulse MD-638/TPX-41, red BIAS ON indicator does not light when POWER switch is placed to ON.	Trouble is in MD-638/TPX-41. Refer to para 3-12d(2).
3	On Receiver-Transmitter, Radio RT-264D/UPX-6, when POWER switch is placed to ON, blower B101 does not operate and POWER Indicator lamp E120 does not light.	Check power switch S104; if not faulty, check interlock switch S102; if not faulty, check connection of plug P107 and jack J207 on RF subassembly. If above checks do not reveal problem, refer to TM 11-5895-245-35.
4	On Receiver-Transmitter, Radio RT-264D/UPX-6, when POWER switch is placed to ON, POWER indicator lamp E120 does not light, but blower B101 begins to operate.	Check overtemperature thermostat switch S103 and check for +60v at jack J109. *a.* If voltage at J109 is +60v, troubleshoot time-delay and overloa d circuits (TM 11-5895-245-35). *b.* If abnormal, check transformer T101 and selenium rectifier CR101.
5	On Receiver-Transmitter Radio RT-264D/UPX-6, when POWER switch is placed to ON, POWER indicator lamp E120 lights, but B101 does not begin to operate.	Check blower B101 and wiring from POWER switch S104 to blower B101. If blower B101 and wiring to blower B101 are not faulty, check starting capacitor C130 and undertemperature thermostat S101.
6	On Coder-Control KY-97C/TPX, red POWER indicator lamp does not light when POWER switch is placed to ON.	Trouble is in KY-97C/TPX. Refer to TM 11-5895-201-35.
7	0 n Decoder, Video KY-593/TPX-44, red POWER indicator lamp does not light when POWER switch is placed to ON.	Disconnect connector P203 and check for 117 vac. If voltage is present, trouble is in KY-593/TPX-44. Refer to TM 11-5840-309-35.
8	On Control, Remote Switching C-1271A/TPX-22, amber RT POWER indicator lamp does not light when RT-264D/UPX-6 POWER switch is placed to ON.	Temporarily place LOCAL-REMOTE switch on KY-97C/TPX to LO-CAL. If amber RT POWER indicator lamp on KY-97C/TPX lights, trouble may be in C-1271A/TPX-22. Refer to para 3-12c(2).
9	On Control, Remote Switching C-7014/TPX-44, green MODE 2 indicator lamp and green OP-ERATE-TEST indicator lamp do not light.	Trouble may exist in either C-7014/TPX-44 or KY-593/TPX-44. Refer to TM 11-5840-309-35.
10	0 n BIanker, Interference MX-8795/TPX-41, POWER and DL HTR indicator lamps do not light when POWER switch is placed to ON.	Trouble is in MX-8795/TPX-41. Refer to para 3-12a(3).

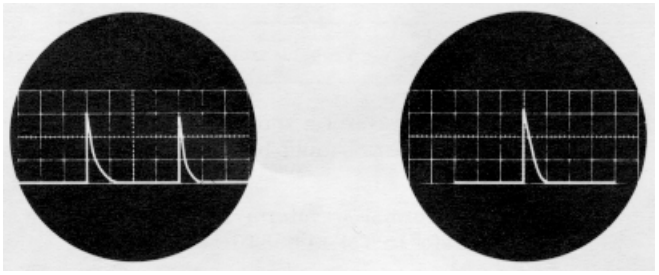
Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
11	No interrogation. CHALLENGE indicators on RT-264D/UPX-6 and C-1271A/TPX-22 do not light, and no IFF replies appear on ppi	RT-264D/UPX-6 is not transmitting. Observe waveform output at connector J1209 on MD-638/TPX-41. Waveform should be pair of pulses as shown in A of fig. 3-1. *a.* If normal waveform is present, trouble exists in RT-264D/UPX-6. Refer to TM 11-5895-245-35. *b.* If normal waveform is not present, refer to item 12.
12	No pulse-pair output from MD-638/TPX-41 at connector J1204.	Observe waveform output at connector J403 on KY-97C/TPX. Waveform should be pair of pulses as shown in A of fig. 3-1. a. If normal waveform is present, trouble exists in MD-638/TPX-41. Refer to para 3-12d(3). *b.* If normal waveform is not present, refer to item 13.
13	No pulse pair output from KY-97C/TPX at connector J403	Observe waveform output at connector P31105 on MX-8795/TPX-41. Waveform should be trigger as shown in B of fig. 3-1. *a.* If normal waveform is present, trouble exists in KY-97C/TPX. Refer to TM 11-5895-201-35. *b;* If normal waveform is not present, trouble exists in MX-8795/TPX-41. Refer to para 3-12a(3).
14	No isls action when ISL switch on MD-638/TPX-41 is placed to ON	Observe waveform output at connector J1208 on MD-638/TPX-41. Waveform should be pulse as shown in C of fig. 3-1. a. If normal waveform is not present, trouble exists in MD-638/TPX-41. Refer to para 3-12d(3). *Note.* To observe waveform in d below, connect output at J213 RF PROBE 20 DB MID BAND ATTEN to R- F IN on Radar Test Set AN/UPM-6B and connect AN/UPM-140B, CHANNEL A INPUT to VIDEO OUT connector onAN/UPM-6B. *b.* If normal waveform is present at J1208, observe waveform at connector J213 RF PROBE 20 DB MID BAND ATTEN on RT-264D/UPX-6. Waveform should be three pulses as shown in D of fig. 3-1. (1) If center pulse (P2) is not present, trouble exists in P2 pulse input circuitry of RT-264D/UPX-6. Refer to TM 11-5895-245-35. (2) If waveform is normal, trouble may exist in MD-638/TPX-41 or Antenna Group AN/GPA-119. Troubleshoot MD-638/TPX-41 (para 3-12d(3)). If no trouble exists in MD-638/TPX-41, troubleshoot Antenna Group AN/GPA-119 (para 3-12f(3)).
15	IFF replies from responding aircraft do not appear on ppi. CHALLENGE indicator lamps on	On SM-472/TPX-44, place B+ ON switch to LOCAL and verify proper output of SM-472/TPX-44 per TM 11-5840-326-35. *a.* If simulated IFF replies appear on ppi, trouble exists in either RT-264D/UPX-6 and C-1271A/MD-638/TPX-41 or Antenna Group AN/GPA-119. Troubleshoot TPX-22 are lit MD-638/TPX-41 (para 3-12d(3)) If no trouble exists in MD-638/TPX-41, troubleshoot Antenna Group AN/GPA-119 (para 3-12f(3)). *b.* If no simulated IFF replies appear on ppi, place OPERATE-TEST switch on C-7014/TPX-44 to TEST. If this causes simulated IFF replies to appear, trouble exists in KY-593/TPX-44. Refer to TM 11-5840-309-35. If simulated IFF replies still do not appear, observe waveform output at connector J204 on KY-593/TPX-41. Waveform should be decoded video pulse as shown in E of fig. 3-1. (1) If normal waveform is present, trouble exists in Control-Indicator Group OA-2664A/FPN-40. Refer to TM 11-5840-293-35. (2) If normal waveform is not present, refer to item 16.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
16	No video output from KY-593/TPX-44 at connector J204	Observe waveform output at connector J31103 on MX-8795/TPX-41. Waveform should be simulated video pulse train as shown in F of fig. 3-1. a. If normal waveform is present, trouble exists in KY-593/TPX-44. Refer to TM 11-5840-309-35. *b.* If normal waveform is not present, refer to item 17.
17	No video output from MX-8795/TPX-41 at connector J31103	Observe waveform output at connector J103 on RT-264D/UPX-6. Waveform should be simulated video pulse train as shown in G of fig. 3-1. *a.* If normal waveform is present, trouble exists in MX-8795/TPX-41. Refer to para 3-12a(3). *b.* If normal waveform is not present, trouble exists in receiver section of RT-264D/UPX-6. Refer to TM 11-5895-245-35.
18	Simulated and actual IFF replies do not appear on ppi when PROCESSED VIDEO-RAW VIDEO switch on MX-8795/TPX-41 is placed to PROCESSED VIDEO.	Trouble exists in MX-8795/TPX-41. Refer to para 3-12a(3).
19	No defruiting action when PROCESSED VIDEO-RAW VIDEO switch on MX-8795/TPX-41 is placed to PROCESSED VIDEO (nonsynchronous replies appear on ppi).	Trouble exists in MX-8795/TPX-41. Refer to para 3-12a(3).
20	No IFF sweep on ppi----------	Observe waveform output at connector J31106 on MX-8795/TPX-41. Waveform should be IFF display trigger as shown in H of fig. 3-1. *a.* If normal waveform is not present, trouble exists in MX-8795/TPX-41. Refer to para 3-12a(3). b. If normal waveform is present, trouble exists in associated remoting equipment or indicator.
21	IFF replies do not appear at same azimuth as associated radar targets	Check for proper orientation of radar azimuth antenna (TM 11-5840-293-12). If radar antenna is not properly oriented, perform Antenna Group AN/GPA-119 orientation as instructed in TM 11-5895-479-12.

3-12. Major Component Troubleshooting

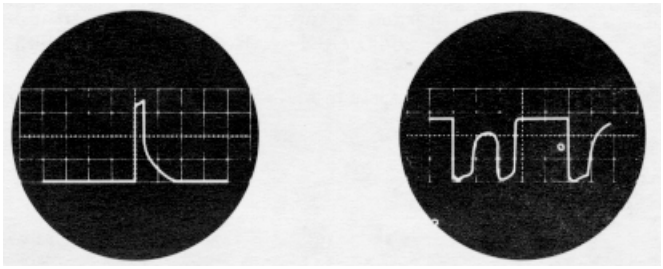
The information contained in a through i below will aid the repairman in locating and correcting equipment troubles that are sectionalized to a major component of Interrogator Set AN/TPX-41. The paragraphs pertaining to major components covered within this manual provide pertinent troubleshooting, voltage, resistance, and waveform data. Paragraphs pertaining to major components not covered in this manual provide references to applicable technical manuals.

a. Blanker, Interference MX-8795/TPX-41, Direct Support Troubleshooting. Direct support troubleshooting of the MX-8795/TPX-41 consists of tracing troubles to the discrete component level with the available test equipment. A prerequisite requires that the MX-8795/TPX-41 be properly installed in an operable AN/TPX-41 system. The instructions in (1) below cover preparational procedures that must be accomplished prior to troubleshooting the MX-8795/TPX-41. Parts location diagrams for the MX-8795/TPX are listed in (2) below. The



A. CODED PULSE PAIR
TESTPOINT: KY-97C/TPX, CONNECTOR J403
TESTPOINT: MD-638/TPX-41, CONNECTOR J1209
SENSITIVITY. 20
SWEEP TIME: 20
HORIZONTAL DISPLAY: X10

B. IFF TRIGGER
TESTPOINT: MX-8795/TPX-41, CONNECTOR J31105
SENSITIVITY: I
SWEEP TIME: 10
HORIZONTAL DISPLAY: X5



C. P2 PULSE
TESTPOINT' MD-638, /PX-41, CONNECTOR J1208
SENSITIVITY' 20
SWEEP TIME: 10
HORIZONTAL DISPLAY: X5

D. RF PULSES OUT (DETECTED)
TESTPOINT. RT-264D/UPX-6, CONNECTOR J213
SENSITIVITY: 2
SWEEP TIME: I
HORIZONTAL DISPLAY- X1

NOTES'

1. WAVEFORMS TAKEN WITH OSCILLOSCOPE AN/USM-140B USING TIME DELAY GENERATOR MX-2962/USM AND 1 TO I COAXIAL TEST CABLE.
2. SWEEP MODE: PRESET
3. TRIGGER SOURCE. EXT AC
4. DELAY FUNCTION' AS REQUIRED
5. DELAYING SWEEP TIME/CM AS REQUIRED
6. HORIZONTAL DISPLAY- AS REQUIRED
7. SENSITIVITY: VOLTS/CM
8. SWEEP TIME- USEC/CM

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Figure 3-1 (1). Interrogator Set AN/TPX-41, system waveforms (sheet I of 2).

Blanker, Interference MX-8795/TPX-41 direct support troubleshooting chart contained in (3) below, lists trouble symptoms, indicates the probable trouble for the symptom, and provides checks and corrective measures to remedy the problem. The information contained in (4) through (7) below consists of pertinent resistance and voltage data that supports the troubleshooting chart and also references applicable figures for parts location purposes.

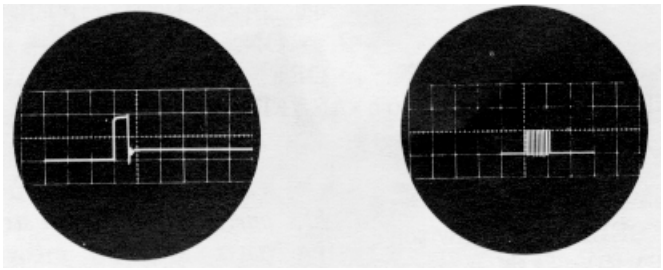
(1) *Blanker, Interference MX---8795/TPX--41, preparation for troubleshooting.* To accomplish effective troubleshooting of the MX-8795/TPX-41, follow the preparational instructions given below.

(a) Remove ac power from AN/TPX-41 and disconnect all cables that are connected on rear panel of MX-8795/TPX-41.

(b) Release four captive screws on front panel of MX-8795/TPX-41, and remove chassis from dust cover.

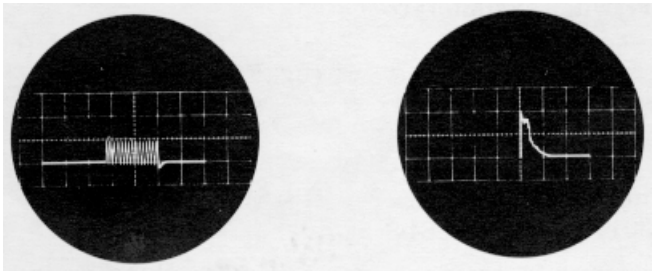
(c) Release cable clamps that secure cables removed in *(a)* above to IFF equipment rack and route cables to level area suitable for working on MX-8795/TPX-41.

(d) Place MX-8795/TPX-41 on work area cited in (c) above and reconnect cables removed in *(a)* above.



E. DECODED IFF VIDEO
TESTPOINT: KY-593/TPX-44, CONNECTOR J204
SENSITIVITY: 2
SWEEP TIME: 10
HORIZONTAL DISPLAY: X1

F. SIMULATED VIDEO OUTPUT
TESTPOINT: MX-8795/TPX-41, CONNECTOR J31103
SENSITIVITY: 5
SWEEP TIME: 50
HORIZONTAL DISPLAY. X2



G. SIMULATED VIDEO OUTPUT
TESTPOINT: RT-264D/UPX-6, CONNECTOR J103
SENSITIVITY' .5
SWEEP TIME: .2
HORIZONTAL DISPLAY' X20

H. IFF DISPLAY TRIGGER
TESTPOINT: MX-8795/TPX-41, CONNECTOR J31106
SENSITIVITY' 2
SWEEP TIME: 2
HORIZONTAL DISPLAY: X2

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Figure 3-1 (2). Interrogator Set AN/TPX-41, system waveforms (sheet 2 of 2).

(e) The MX-8795/TPX-41 contains three plug-in circuit cards consisting of the processor (chassis series No. 30800), trigger/gate generator (chassis series No. 30900), and synchronizer multiplier (chassis series No. 31000). Troubleshooting of these circuit cards necessitates the use of adapter, circuit card test extender, furnished as part of Multiplexer TD-991/G or Demultiplexer TD-992/G. To use extender card, remove ac power to MX-8795/TPX-41, release two snaplock fasteners on circuit card to be tested, remove card and install card extender. Install card to be tested in connector located on top of card extender.

CAUTION

For protection of transistors, before removing a circuit card or card extender from a connector, insure that power is removed.

(f) On Receiver-Transmitter, Radio RT-264D/UPX-6, install power attenuator Z501 and dummy load Z502 on ANTENNA connector J212.

(g) On Coder-Control KY-97C/TPX-44, place POWER switch (S407) to ON, CHALLENGE

switch (S404) to ON, and LOCAL-REMOTE switch (S402) to REMOTE.

(h) On Receiver-Transmitter, Radio RT264D/UPX-6, place POWER switch (S104) to ON.

(i) On Control, Remote Switching C1271A/TPX, place MODE SELECTOR switch (S701) to position 2, RECEIVER GAIN control (R701) to 10, GTC switch (S703) to SHORT, and CHOP switch (S702) to CHOP.

(j) On Control, Remote Switching C7014/TPX-44, place BEACON ASSIST switch (S40306) to OFF, EMER-OFF switch (S40304) to OFF, and BRACKET-OFF switch (S40305) to BRACKET.

(k) On Decoder, Video KY-593/TPX-44, place POWER switch (S201) to ON.

(l) On Modulator, Pulse MD-638/TPX41, place POWER switch (S1301) to ON, and SLS switch (S1302) to ON.

(m) On Blanker, Interference MX-8795/ TPX-41, place POWER switch (S31101) to ON, and PROCESSED VIDEO-RAW VIDEO switch (S31102) to RAW VIDEO.

(n) On Interconnecting Box J-2945/TPX41, place IFF POWER circuit breaker CB8601 to ON, insure SCAN switch S8601 is placed to OFF, and IFF SCAN switch S8602 is placed to SAFE.

(2) *Blanker, Interference MX-8795/TPX41, parts location illustrations.* Figures containing parts location information for components of the MX-879/TPX-41 consist of the following:

(a) Main chassis (chassis series No. 31100) (fig. 3-6).

(b) Processor (chassis series No. 30800) (fig. FO-4).

(c) Trigger/gate generator (chassis series No. 30900) (fig. FO-4).

(d) Synchronizer, multiplier (chassis series No. 31000) (fig. FO-4).

(3) *Blanker, Interference MX--8795/TPX41, direct support troubleshooting chart.*

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
1	POWER indicator lamp DS31101 does not light and POWER fuse F31101 is good	Check for ac input power on rear of connector J31101 across pins A and B. *a.* If no ac input power is present, check for proper mating of connectors P31101 and J31101. *b.* If ac power is present, check POWER switch S31101, fuse holder XF31101, and lamp holder XDS31101.
2	POWER indicator lamp DS31101 does not light and POWER fuse F31101 continues to blow.	Check dc resistance between terminal A and C on power supplies PS31101 and PS31102 (para 3-12a(4)).
3	POWER indicator lamp DS31101 lights but no outputs are present at J31103 (D, fig. 3-1), J31104 (K, J31103 (D, fig. 3--1), J31104 (K, fig. 3-2) fig. 3-2), J31105 (B, fig. 3-1) and J31106 (H, fig. 3-1)	Check for +15v between TP31101 and TP31102. a. If +15v is not present, check following: (1) Check R31101 and R31109. (2) Check PS31101 wiring (fig. FO-4). (3) If steps (1) and (2) are normal, check PS31101. *b.* If +15v is present, check between TP31101 and following testpoints for proper voltages. (1) Check TP31104 for +10 +1v. If abnormal, check following: (a) Check R31103.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
		(b) Check CR31101 (para 3-12a(5)). (c) Check C31101. (2) Check TP31106 for +6 t5v. If abnormal, check following: (a) Check R31104. *(b)* Check CR31102 (para 3-12a(5)). *(c)* Check C31102. (3) Check TP31108 for +3.3 +0.25v. If abnormal, check following: (a) Check R31105. *(b)* Check CR31103 (para 3-12a(5)). (c) Check C31103. Check for -- 5v between TP31101 and TP31103. *a.* If -15v is not present, check following: (1) Check R31102 and R31108. (2) Check PS31102 wiring (fig. FO-4) (3) If steps (1) and (2) are normal, check PS31102. *b.* If -15v is present, check between TP31101 and the following testpoints for proper voltages. (1) Check TP31105 for -10 +lv. If abnormal check following: *(a*) Check R31107. *(b)*Check CR31105 (para 3-12a(5)). *(c)*Check C31105. (2) Check TP31107 for -6 +0.5v. If abnormal check following: *(a*) Check R31106. *(b*) Check CR31104 (para 3-12a(5)). *(c)*Check C31104.
4	Timing and video outputs at connectors cited in item 3 above are present but unstable	Check dc voltages in item 3 above for proper levels. If voltage levels checked above are normal, trouble may exist in trigger/gate generator. Perform following checks to determine trouble source. *a.* Observe waveform at 'IP30903. Waveform should be stable pulse as shown in A, fig. 3-2. (1) If waveform is normal, refer to b below. (2) If waveform is abnormal, check following: *(a)* Check that PW ADJ control is properly adjusted per para 3-16. *(b*) Check Q30901, Q30902, Q30903, and Q30904 (para 3-12a(6)). *(c*) Check CR30901 (para 3-12a(5)). *b.* Observe waveform at TP30904. Waveform should be gate as shown in B, fig. 3-2. (1) If waveform is normal, refer to item 6 below. (2) If waveform is abnormal, check the following: *(a)* Check that CP GATE control R30936 is properly adjusted per para 3-16. *(b*) Check Q30905, Q30911, Q30912, and Q30913 (para 3-12a(6)). *(c)* Check delay line DL30901 (para 3-12a(4)).
5	Nonsynchronous replies at connector J31103.	*a.* Insure that PRF SEL switch is properly set. *b.* Check relay KS0801. Relay should be deenergized with PROCESSED VIDEO-RAW VIDEO switch set to PROCESSED VIDEO. (1) If relay operates normally, check AND gates Q30817 and Q30804 (para 3-12a(6)). (2) If (1) is normal, check AND gate Q30810, Q30813 and Q30818 (para 3-12a(6)).

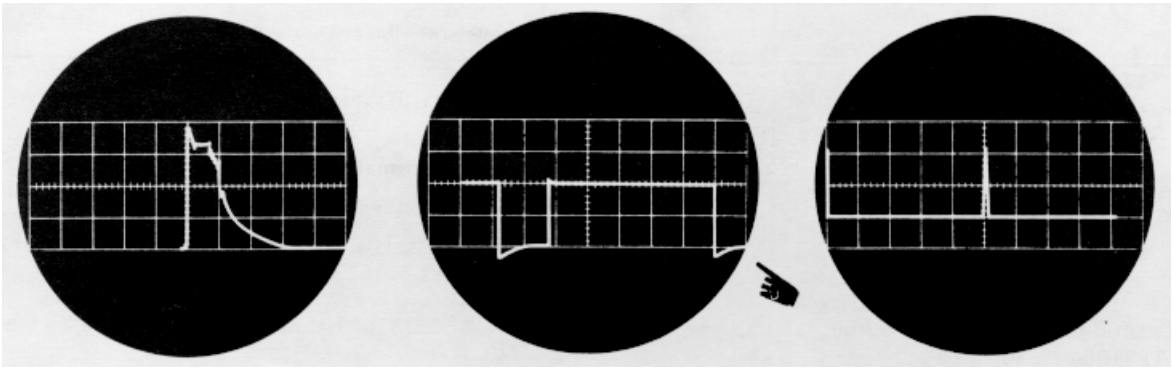
Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
6	No circulating pulse waveform at TP30804 (C, fig. 3-2)	Check Q30815, Q30816, and Q30819 (para 3-12a(6)). If transistors are good, observe waveform at TP30805. Waveform should be IFF video and control pulse as shown in D, fig. 3-2. *a.* If waveform is abnormal or absent, trouble may be related to DL31101. Refer to item 7. *b.* If waveform is normal, check Q30813 and Q30814 (para 3-12a(6)).
7	No output from DL31101 (observed at TP30805, D, fig. 3-2)	Check voltage levels in item 3 above. If all voltage levels are normal, observe waveform at TP30802. Waveform should be IFF video and circulating pulse as shown in E, fig. 3-2. *a.* If waveform is abnormal or absent trouble may exist in processor. Refer to item 8. *b.* If waveform is normal, check DL31101 (para 3-12a(4)).
8	No delay line input waveform at TP30804 (C, fig. 3-12)	Observe waveform at TP30803. Waveform should be IFF video as shown in F of fig. 3-2. *a.* If waveform is absent or abnormal, refer to item 9. *b.* If normal waveform is present, check the following: (1) Check Q30801 through Q30807 (para 3-12a(6)). (2) If transistors checked in (1) above are good , check Q30817. (3) If (2) is normal, observe waveform at TP30807. Waveform should be gate as shown in G, fig. 3-2. *(a)* If waveform is normal, check Q30909 in trigger/gate generator. *(b)* If waveform is abnormal, check Q30905 through Q30908 and Q30910 (para 3-12a(6)). *(c)* If (b) is normal, check DL30901 (para 3-12a(4)), and CR30905 and CR30907 (para 3-12a(5))
9	No IFF video at TP30803 (F, fig 3-2).	Check wiring between connectors J31102 and J31107 (fig. FO-4).
10	No IFF video output at TP30806 (H, fig. 3-2)	Check relay K30801 (para 3-12a(4)). *a.* If relay is good, check Q30817 and Q30812 (para 3-12a(6)). *b.* If a is normal, check Q30809, Q30810, Q30813, Q30814 and Q30818 (para 3-12a(6)). *c.* If transistors checked in b above are good, refer to probable trouble, checks, and corrective measures for item 6 above.
11	No IFF trigger output at connector J31103 (F, fig. 3-1)	Observe waveform at TP31003. Waveform should be IFF trigger as shown in I, fig. 3-2. *a.* If waveform is absent or abnormal, refer to item 12. *b.* If normal waveform is present, check wiring between connectors J31109 and J31105 (fig. FO-4).
12	No IFF trigger at TP31003 (I, fig 3-2)	Observe waveform at TP30905. Waveform should be trigger as shown in J, fig. 3-2. *a.* If waveform is absent or abnormal, refer to item 13. *b.* If normal waveform is present, check Q31001 and Q31002 (para 3-12a(6)).
13	No delayed trigger at TP30905 (J, fig 3-2).	Check Q30914 through Q30918 (para 3-12a(6)).

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
14	No 1500-Hz radar synch output at J31104 (K, fig. 3-2)	Observe waveform at TP31004. Waveform should be 1500-Hz sine wave as shown in L, fig. 3-2. *a.* If waveform is absent or abnormal, refer to item 15. *b.* If waveform is normal, check the following: (1) Check wiring between J31104, FL31101, and J31109 (fig. FO-4). (2) If (1) is normal check FL31101.
15	No 1500-Hz radar synch output at TP31004 (L, fig. 3-2).	Check Q31003, Q31004, and Q31007 through Q31010 (para 3-12a(6)).
16	Waveform at TP31004 (L, fig. 3-2) is not 1500 Hz.	Check adjustment of FREQ control R31024 (para 3-16).
17	1500-Hz radar synch at TP31004 (L, shown' fig. 3-2) is unstable	Observe waveform at TP31002. Waveform should be square wave as in M, fig. 3-2 DELAY *a.* If square wave duration is not correct, check adjustment DELAY ADJ control R31017 (para 3-16). *b.* If waveform is not present, refer to item 18. *c.* If waveform is normal, check Q31003, Q31004 and Q31007 through Q31010 (para 3-12a(6)).
18	No square wave (M, fig. 3-2) at TP31002	Observe waveform at TP30903. Waveform should be pulse as shown in A, fig. 3-2. *a.* If waveform is absent or abnormal, refer to step a(2) in item 4 above. *b.* If waveform is normal, check Q31005 and Q31006 (para 3-12a(6)).
19	No IFF display trigger output at connector J31106 (H, fig. 3-1)	Observe waveform at TP30903. Waveform should be pulse as shown in A, fig. 3-2. *a.* If waveform is absent or abnormal, refer to step a(2) in item 4 above. *b.* If waveform is normal, check wiring between J31106 and pin 2 on J31108 (fig. FO-4).
20	No raw video output at J31103 (F, fig 3-1) when PROCESSED VIDEO-RAW VIDEO switch is placed to RAW VIDEO	Check relay K30801 (para 3-12a(4)). *a.* If relay is good, check switch S31102. *b.* If switch is good, check associated wiring to insure proper connections (fig. FO-4).

(4) *Blanker, Interference MX-8795/TPX-41, dc resistances of delay lines, relays, and power supplies.* The following charts list the' delay lines, relays, and power supplies in the MX-8795/TPX-41, reference a figure that shows the location of each, and give the dc resistance of the windings between the terminals.

(a) General.

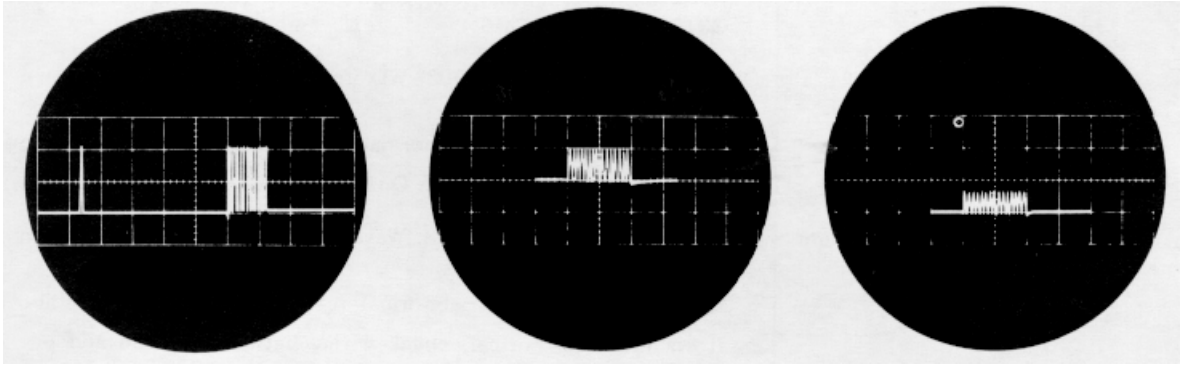
Component	Location (fig.)	Terminals	Dc resistance (ohms)
DL30901--	FO-4	1-2	200
K30801 --------	FO-4	2-7	500
PS31101 ------	3-6	A-C	140
PS31102---	3-6	A-C	140



A. PRETRIGGER
TESTPOINT: TP30903
SENSITIVITY: .1
SWEEP TIME: .5
HORIZONTAL DISPLAY: X1

B. CIRCULATING PULSE GATE
TESTPOINT: TP30904
SENSITIVITY: .2
SWEEP TIME: MILLISECONDS/CM .5
HORIZONTAL DISPLAY: X1

C. CIRCULATING PULSE
TESTPOINT: TP30804
SENSITIVITY: 10
SWEEP TIME: 5
HORIZONTAL DISPLAY: X100



D. DELAYED CIRCULATING PULSE AND IFF VIDEO
TESTPOINT: TP30805
SENSITIVITY: .2
SWEEP TIME: 20
HORIZONTAL DISPLAY: X1

E. IFF VIDEO INPUT (TO DELAY LINE)
TESTPOINT: TP30802
SENSITIVITY: .5
SWEEP TIME: 50
HORIZONTAL DISPLAY: X5

F. IFF VIDEO INPUT (TO PROCESSOR)
TESTPOINT: TP30803
SENSITIVITY: .2
SWEEP TIME: 50
HORIZONTAL DISPLAY: X5

NOTES:

1. WAVEFORMS TAKEN WITH OSCILLOSCOPE AN/USM-140B USING TIME DELAY GENERATOR MX-2962/USM
2. SWEEP MODE: PRESET
3. TRIGGER SOURCE: EXT AC
4. DELAY FUNCTION: AS REQUIRED
5. DELAYING SWEEP TIME/CM AS REQUIRED
6. HORIZONTAL DISPLAY: AS REQUIRED
7. SENSITIVITY: VOLTS/CM
8. SWEEP TIME: USEC/CM (UNLESS OTHERWISE INDICATED)

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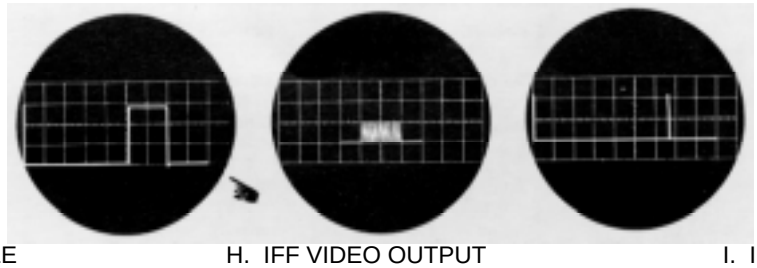
Figure 3-2 (1). Blanker, Interference MX-8795/TPX-41, waveforms (sheet 1 of 2).

(b) Delay line DL31101 (fig. 3-6).*

Terminals	Forward'	Meter scale (RX)	Reverse	Meter scale (RX)
3-1	0.1	1	0.1	1
3-2	infinity	100	infinity	100
3-4	250	100	42	10
3-5	infinity	100	infinity	100
3-6	6.2	1	300	100
3-7	0.1	1	0.1	1
3-8	infinity	100	infinity	100
3-9	0.1	1	0.1	1
3-10	infinity	100	infinity	100
3-11	0	1	0	1
3-12	250	100	42	10
3-13	infinity	100	infinity	100
3-14	6.2	1	300	100
3-15	0.1	1	0.1	1
3-16	infinity	100	infinity	100
3-17	0.1	1	0.1	1
3-18	infinity	100	infinity	100
3-19	0	1	0	1
3-20	250	100	42	10
3-21	infinity	100	infinity	i00
3-22	6.2	1	300	100
3-23	0.1	1	0.1	1
3-24	infinity	100	infinity	100

** Before attempting these measurements, remove ac power and the processor (chassis series No. 30800).*

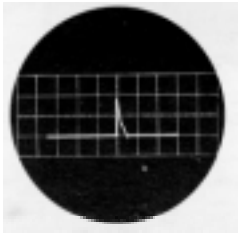
(5) Blanker, Interference MX-8795/TPX 41, dc resistance of diodes. The following charts list forward and reverse resistance of all diodes in the MX-8795 / TPX-41. Multimeter ME-26B / U or equivalent should be used to perform these tests. Included in each chart is a meter scale (RX1, RXI00, Rx1K, etc.) to be used for each particular measurement. All measurements are taken with all cables removed from the MX-8795/TPX-41.



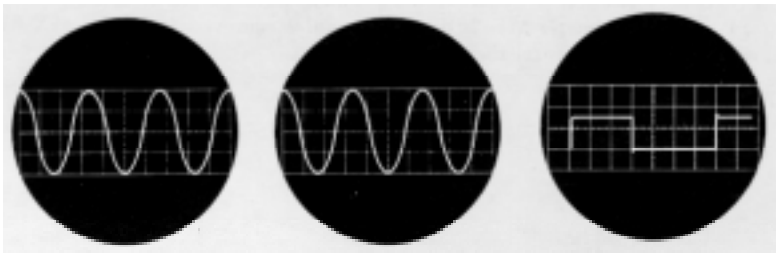
G. IFF OUTPUT ENABLE
TESTPOINT: TP30807
SENSITIVITY: .05
SWEEP TIME: MILLISECONDS/CM.5
HORIZONTAL DISPLAY: X1

H. IFF VIDEO OUTPUT
TESTPOINT: TP30806
SENSITIVITY: .5
SWEEP TIME: 50
HORIZONTAL DISPLAY: X5

I. IFF TRIGGER
TESTPOINT: 31003
SENSITIVITY: .5
SWEEPTIME: MILLISECONDS/CM .5
HORIZONTAL DISPLAY: X1



J. DELAYED TRIGGER
TEST POINT: TP30905
SENSITIVITY: .2
SWEEP TIME: 10
HORIZONTAL DISPLAY: X1



K. 1500 HZ RADAR SYNCH OUTPUT
TESTPOINT: CONNECTOR J31104
SENSITIVITY: .5
SWEEP TIME: MILLISECONDS/CM .2
HORIZONTAL DISPLAY: X1

L. 1500 HZ RADAR SYNCH
TESTPOINT: TP31004
SENSITIVITY: .5
SWEEP TIME: MILLISECONDS/CM .2
HORIZONTAL DISPLAY: X1

M. SQUARE WAVE
TESTPOINT: TP31002
SENSITIVITY: .5
SWEEP TIME: MILLISECONDS/CM .5
HORIZONTAL DISPLAY: X1

EL5895-479-35-TM-CI 1-21 (2)

Figure 3-2 (2) . Blanker. Interference MX-8795/ TPX-41, waveforms (sheet 2 of 2).

(a) Main chassis. *(b) Processor.*

Diode	Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Diode	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
CR31101	8.0	u	600	10	CR30801	280	100	6k	1k
CR31102	5.5	1	750	10	CR30802	280	100	3300	100
CR31103	1100	100	1100	100	CR30804	300	100	800k	10k
CR31104	5.5	1	1700	100	CR30805	450	100	240	100
CR31105	5.5	1	200	10					

(c) Trigger/gate generator

Diode	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
CR30901	1850	100	20k	1K
CR30902	300	100	7k	100
CR30903	300	100	10k	100
CR30904	300	100	26k	1K
CR30905	300	100	7k	100
CR30906	310	100	7k	100
CR30907	300	100	2.9k	100
CR30908	320	100	3k	100
CR30909	320	100	5k	100

(d) Synchronizer multiplier.

Diode	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
CR31001	45	10	24k	1K
CR31002	2k	100	20k	1K

(6) *Blanker, Interference MX-8795/TPX41. dc resistance of transistors.* The forward and reverse resistance of all transistors contained on the MX-8795 / TPX-41 are listed in the charts below. Multimeter ME-26 / U or equivalent should be used to perform these tests. Measurements are not made with respect to ground; they are measured across the transistor junctions listed. Forward and reverse values are given in ohms. All measurements are to be made only after ac power has been removed from the MX-8795/PTX-41, and the suspected circuit card has been removed.

(a) Processor

.

	Base to emitter				Base to Collector			
Transistor	Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
Q30801	1600	100	9.5k	1K	1200	100	30 mego	1M
Q30802	1350	100	7.5k	1K	1100	100	30 mego	1M
Q30803	1400	100	2.2k	100	1100	100	3.3k	100
Q30804	1500	100	6k	1K	1100	100	6k	1K
Q30805	1400	100	3k	100	1100	100	3k	100
Q30806	1500	100	10k	1K	1200	100	13k	1K
Q30807	1500	100	6.3k	1K	1100	100	30 mego	1M
Q30808	1550	100	13k	1K	1100	100	30 mego	1M
Q30809	1400	100	3k	100	1100	100	3k	100
Q30810	1600	100	6k	1K	1350	100	30 mego	1M
Q30811	1550	100	Ilk	1K	1100	100	30 mego	1M
Q30812	110	100	110	100	1300	100	30mego	1M
Q30813	1500	100	6.2k	1K	1100	100	30 mego	1M
Q30814	1650	100	10k	1K	1200	100	Ilk	1K
Q30815	1500	100	6k	1K	1050	100	6.2k	1K
Q30816	1600	100	3.6k	100	1300	100	5.8k	1K
Q30817	1500	100	200 Mego	IM	1100	100	200 mego	1M
Q30818	1450	100	400 Mego	1M	1100	100	400 mego	1M
Q30819	1400	100	3.5k	100	1100	100	30 mego	1M

(b) Trigger/gate generator.

Transistor	Base to emitter				Base to collector			
	Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
Q30901	1600	100	32k	1K	1150	100	190k	10K
Q30902	1500	100	140k	10K	1100	100	2k	100
Q30903	1500	100	14k	1K	1150	100	9k	1K
Q30904	1500	100	11k	1K	1100	100	14k	1K
Q30905	1500	100	11k	1K	1100	100	14k	1K
Q30906	1450	100	2.2k	100	1100	100	6.5k	1K
Q30907	1500	100	15k	1K	1100	100	11k	1K
Q30908	1200	100	2.5k	100	700	100	16k	1K
Q30909	1500	100	3.2k	100	1100	100	300 mego	1M
Q30910	1600	100	3.3k	100	1300	100	300 mego	1M
Q30911	1500	100	2.3k	100	1100	100	6.5k	1K
Q30912	1500	100	16k	1K	1100	100	11k	1K
Q30913	1550	100	28k	1K	1200	100	18k	1K
Q30914	1700	100	7k	1K	1300	100	11k	1K
Q30915	1500	100	3.6k	100	1050	100	4.5k	100
Q30916	940	100	960	100	1100	100	3k	100
Q30917	1500	100	16k	1K	1100	100	11k	1K
Q30918	1450	100	4.4k	100	1100	100	7k	1K

(c) Synchronizer multiplier.

Transistor	Base to emitter				Base to collector			
	Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
Q31001	64	100	11k	1K	55	100	33k	1K
Q31002	50	100	10k	1K	50	100	500 mego	1M
Q31003	50	100	6k	1K	48	100	24k	1K
Q31004	50	100	5k	1K	50	100	200k	1K
Q31005	65	100	8k	1K	55	100	15k	1K
Q31006	70	100	30k	1K	55	100	18k	1K
Q31007	60	100	100k	1K	55	100	100k	1K
Q31008	50	100	9k	1K	52	100	11k	1K
Q31009	50	100	13k	1K	48	100	3.4k	1K
Q31010	52	100	5k	1K	46	100	100k	1K

(7) *Blanker, Interference MX-8795/TPX41, voltage data.* The terminal voltages contained in the following charts ((a), (b), and (c) below) can be observed using Multimeter ME-26B/U. Before any voltage measurements are attempted, insulate the entire test probe, except for the extreme tip, with tape or sleeving. A momentary short circuit can damage a transistor in associated circuits. Characteristics of transistors may cause a large variation of the base and emitter voltage indications whenever they are replaced. This should not affect circuit operation. Observe that collector voltages remain stable. All connections of Interrogator Set AN/TPX-41 are normal with selected control settings and adjustments as indicated in paragraph 3-12a(l).

NOTE

For access to transistor terminals on plug-in circuit cards, use card extender as described in paragraph *3-12a(1)(e).* Before removing a subassembly from the connector or card extender, always insure that power is removed for protection of transistors.

(a) Processor.

Transistor	Voltage to ground		
	Emitter	Collector	Base
Q30801 (NPN)	−1.07	+6	−0.63
Q30802 (NPN)	−0.43	+3.0	+0.22
Q30803 (NPN)	0	+1.71	0
Q30804 (NPN)	0	+0.11	+0.67
Q30805 (NPN)	0	+3.2	+0.11
Q30806 (NPN)	0	+3.2	0
Q30807 (NPN)	0	+0.16	+0.72
Q30808 (NPN)	−1.36	+6	−0.68
Q30809 (NPN)	0	+3.4	+0.11
Q30810 (NPN)	0	+0.17	+0.68
Q38011 (NPN)	0	+5.9	0
Q30812 (PNP)	+5.9	0	+5.9
Q30813 (NPN)	0	+0.17	+0.72
Q30814 (NPN)	0	+1.7	0
Q30815 (NPN)	0	+0.16	+0.7
Q30816 (NPN)	+0.08	+0.16	+0.5
Q30817 (NPN)	0	+0.11	+0.58
Q30818 (NPN)	+0.1	+0.17	+0.64
Q30819 (NPN)	0	+6	+0.15

(b) Trigger/gate generator.

Transistor	Voltage to ground		
	Emitter	Collector	Base
Q30901 (NPN)	+0.32	+9.6	−0.04
Q30902 (NPN)	+9.4	+10	+9.6
Q30903 (NPN)	0	+10	+0.72
Q30904 (NPN)	0	+6	0
Q30905 (NPN)	0	+6	0
Q30906 (NPN)	0	+3.2	0
Q30907 (NPN)	0	+3.2	−0.05
Q30908 (NPN)	+0.21	+2.37	−0.1
Q30909 (NPN)	+0.14	+1.52	+0.55
Q30910 (NPN)	+0.14	+1.21	+0.55
Q30911 (NPN)	0	+2.78	0
Q30912 (NPN)	0	+2.78	+0.06
Q30913 (NPN)	+0.18	+2.67	−0.28
Q30914 (NPN)	0	+6.0	0
Q30915 (NPN)	0	+6.0	+0.17
Q30916 (NPN)	0	+0.19	+0.7
Q30917 (NPN)	0	+6.0	+0.18
Q30918 (NPN)	0	+6	0

(c) Synchronizer multiplier.

Transistor	Voltage to ground		
	Emitter	Collector	Base
Q31001 (NPN)	0	+9.0	0
Q31002 (NPN)	+14.0	0	+14.0
Q31003 (NPN)	−2.4	+8.6	−1.7
Q31004 (NPN)	−1.4	+14.0	+13.0
Q31005 (NPN)	0	+0.2	+4.2
Q31006 (NPN)	0	+2.8	+0.5
Q31007 (NPN)	−0.65	−0.1	+4.3
Q31008 (NPN)	−7.6	−1.8	−6.8
Q31009 (NPN)	−1.4	−8.2	−1.8
Q31010 (PNP)	−14.0	−1.5	−13.0

b Coder-Control KY-97C/TPX, Direct Support Troubleshooting. For information pertaining to the troubleshooting of Coder-Control KY-97C/TPX, refer to TM 11-5895-201-35.

c. Control, Remote Switching C-1271A/TPX-22, Direct Support Troubleshooting. Direct support troubleshooting of the C-1271A/TPX-22 consists of tracing troubles to the discrete component level. A prerequisite requires that the C-1271A/TPX-22 be properly installed in an operable AN/TPX-41 system. The instructions in (1) below cover preparational procedures that should be accomplished prior to troubleshooting the C-1271A/TPX-41. The Control, Remote Switching C-1271A/TPX-22 direct support troubleshooting chart, contained in (2) below, lists trouble symptoms, indicates the probable trouble for the symptom, and provides checks and corrective measures to remedy the problem. The resistance data contained in (3) below following the troubleshooting chart, provides supporting information to aid in identifying troubles. Locations of parts within the C-1271A/TPX-22 are shown in figure 3-7.

(1) *Control, Remote Switching C-1271A/TPX-22, preparation for troubleshooting.* To accomplish effective troubleshooting of the C-1271A/TPX-22, follow the preparational instructions given below.

(a) Remove C-1271A/TPX-22 from mounting bracket located on side of Cabinet, Electrical Equipment CY-2094/FPN-33 by removing four attaching screws, nuts, lockwashers, and flat washers.

(b) Place C-1271A/TPX-22 on suitable work area leaving external cables connected.

(c) Remove six screws that secure front panel of C-1271A/TPX-22 and carefully separate front panel from box assembly. This should expose all internal components of C-1271A/TPX-22 to facilitate troubleshooting.

(d) Make preliminary control settings and perform starting procedure as described in TM 11-5895-479-12

(2) *Control, Remote Switching C-1271A/ TPX-22, direct support troubleshooting chart.*

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
1	RT POWER indicator lamp I732 does not light	Check RT POWER indicator lamp socket. If socket is good check lamp socket wiring (fig. FO-5).
2	CHALLENGE indicator lamp I731 does not light	Check CHALLENGE indicator lamp socket. If socket is good check lamp socket wiring (fig. FO-5).
3	RECEIVER GAIN control R731 has no effect on video presentation or video breaks up when RECEIVER GAIN control is varied.	Check R731 (para 3-12c(3)).
4	No Interrogation when PUSH TO CHAL switch S733 is pressed.	Check PUSH TO CHAL switch S733 (para 3-12c(3)).
5	GTC action exists in one condition only, (LONG or SHORT) regardless of setting of GTC switch S734.	Check GTC switch S734 (para 3-12c(3)).
6	CHOP action remains either ON or OFF regardless of setting of CHOP switch S732.	Check CHOP switch S732 (para 3-12c(3)).
7	Interrogation in MODE 2 only, regardless of setting of MODE SELECTOR switch S731.	Check MODE SELECTOR switch S731 (para 3-12c(3)).
8	KY-97C/TPX and KY-593/TPX-44 do not operate in same mode.	Check MODE SELECTOR switch S731 (para 3-12c(3)).
9	Coded output of KY-97C/TPX does not correspond with selected mode of interrogation as established by setting of MODE SELECTOR switch S731.	Check MODE SELECTOR switch S731 (para 3-12c(3)).

(3) Control, Remote Switching C-1271A/ TPX-22, dc resistances. The following chart provides dc resistance and continuity information to aid in identifying defective components in the C-1271A/TPX-22. All resistance readings are to be taken with external cables removed from the unit, using Multimeter ME-26B/U.

Component	Switch position	Points of test	Resistance in ohms
MODE SELECTOR switch S731.....	1	Connector J731:	
		Pin G to B.....	0
		Pin G to H	Infinite
		Connector J732:	
		Pin B to A.....	0
		Pin B to C.....	Infinite
	2	Connector J731:	
		Pin G to B.....	Infinite
		Pin G to H	Infinite

Component	Switch position	Points of test	Resistance in ohms
		Connector J732:	
		Pin B to A	Infinite
		Pin B to C	Infinite
	3	Connector J731:	
		Pin G to B	Infinite
		Pin G to H	0
		Connector J732:	
		Pin B to A	Infinite
		Pin B to C	
CHOP switch S732	ON	Connector J731:	
		Pin G to A	0
	OFF	Connector J731:	
		Pin G to A	Infinite
PUSH TO CHAL switch S733	Pressed	Connector J731:	
		Pin G to C	0
	Released	Connector J731:	
		Pin G to C	Infinite
GTC switch S734	SHORT	Connector J731:	
		Pin G to F	0
	LONG	Connector J731:	
		Pin G to F	Infinite
RECEIVER GAIN poten-	:	Connector J731	
tiometer R731	Rotated from fully cw to fully ccw.	Pin J to D	Increases smooth-ly to 1000 +100
CHALLENGE indicator I731.....	:	Connector J731	
		Pin G to I	15
RT POWER indicator I732	:	Connector J731	
		Pin G to E	15

d. Modulator, Pulse MD-638/TPX-41, Direct Support Troubleshooting. Direct support troubleshooting of the MD-638/TPX-41 consists of tracing troubles to the discrete component level with the available test equipment. A prerequisite requires that the MD-638/TPX-41 be properly installed in an operable AN/TPX-41 system. The instructions in (1) below cover preparational procedures that should be accomplished prior to troubleshooting the MD-638/TPX/41. Parts location diagrams for the MD-638/TPX-41 are listed in (2) below. The Modulator, Pulse MD-638/TPX-41 direct support troubleshooting chart, contained in (3) below, lists trouble symptoms, indicates the probable trouble for the symptom, and provides checks and corrective measures to remedy the problem. The information contained in (4) through (7) below consists of pertinent resistance and voltage data that supports the troubleshooting chart and also references applicable figures for parts location purposes.

(1) *Modulator, Pulse MD-638/TPX-41, preparation for troubleshooting.* To accomplish effective troubleshooting of the MD-638/TPX-41, follow the preparational instructions given below.

(a) Remove MD-638/TPX-41 from wall of S-70/G Shelter by removing six attaching screws and place unit on suitable work area

.

(b) n MD-638/TPX-41, remove perforated dust cover by removing eight slotted panhead machine screws, eight flat washers, and eight lockwashers that secure perforated dust cover during normal operation.

(c) The MD-638/TPX-41 contains one plug-in circuit card; pulse generator processor (chassis series No. 1300). Troubleshooting of this circuit card necessitates use of locally fabricated card extender. To use card extender, remove ac power to MD-638/TPX-41, release two snap-lock fasteners on pulse generator processor, remove pulse generator processor and install card extender in its place. Install pulse generator processor in connector located on top of card extender.

CAUTION

For protection of transistors, before removing the pulse generator processor or the card extender, insure that power is removed.

(d) On Receiver-Transmitter, Radio RT-264D/UPX-6, install power attenuator Z501 and dummy load Z502 on ANTENNA connector J212.

(e) On Coder-Control KY-97C/TPX, place POWER switch (S407) to ON, CHALLENGE switch (S404) to ON, and LOCAL-REMOTE switch (S402) to REMOTE.

(f) On RT-264D/UPX-6, place POWER switch (S104) to ON.

(g) On Control, Remote Switching C-1271A/TPX-22, place MODE SELECTOR switch (S701) to position 2, RECEIVER GAIN control (R701) to 10, GTC switch (S703) to LONG, and CHOP switch (S702) to OFF.

(h) On Blanker, Interference MX-8795/TPX-41, place POWER switch (S31101) to ON, and PROCESSED VIDEO-RAW VIDEO switch (S31102) to RAW VIDEO.

(i) On Decoder, Video KY-593/TPX-44, place POWER switch (S201) to ON.

(j) On MD-638/TPX-41, place SLS switch (S1302) to ON.

(k) On Interconnecting Box J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON and ensure that SCAN switch S8601 is placed to OFF and IFF SCAN switch is placed to SAFE.

(2) *Modulator, Pulse MD-638/TPX-41, parts location illustrations.* Figures containing parts location information for the components of the MD-638/TPX-41 consist of the following:

(a) Modulator, Pulse MD-638/TPX-41 (chassis series No. 1200) (fig. 3-8).

(b) Pulse generator processor (chassis series No. 1300) (fig. FO-6).

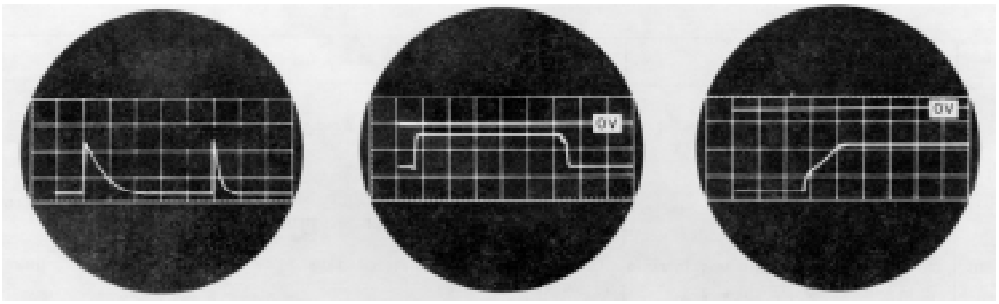
(3) Modulator, Pulse MD-638/TPX-41, direct support troubleshoooting chart.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
1	BIAS ON indicator lamp does not light and fuse F1301 does not blow.	Check for ac input power on rear of connector J1201 across pins A and B. a. If no ac input power is present, check for proper mating of connectors P1201 and J1201. b. If ac power is present, check POWER switch S1301, fuse holder XF1301, and lamp holder XDS1301. c. If indication in *b* above is normal, check relay K1301 (para 3-12d(4)). If the relay is good, make following checks: (1) Check for -30v at TP1302. *(a)* If voltage is normal, refer to (2) below. *(b)* If voltage is not present, check fuse F1303. If fuse is good, check +250v power supply circuits consisting of CR1203, CR1204, and CR1208 through CR1210 (para 3-12d(5)). (2) Check for +250v at TP1303. *(a)* If voltage is normal, refer to item 3.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
		(b) If voltage is not present, check fuse F1302. If fuse is good, check -30v power supply circuits consisting of CR1201, CR1202, and CR1205 through CR1207 (para 3-12d(5)).
2	BIAS ON indicator lamp does not light, fuse F1301 continues to blow.	Check transformer T1201 (para 3-12d(4)).
3	BIAS ON indicator lamp does not light and ac input circuits and power supply circuits (checked in items 1 and 2 above) are good.	Trouble may exist in RF cabling or interlock circuit. Make following checks to determine trouble source: *a.* Remove connector P1210 from MD-638/TPX-41 and measure resist ance between center conductor and outer conductor of P1210. Resistance should be less than 1000 ohms and greater than 70 ohms. If abnormal, disconnect connector P20003 from Pedestal, Antenna AB-1158/CPA-119 and check cables W9209 and W9407 for proper continuity. (1) If abnormal, one or both cables are defective. (2) If normal, trouble exists in antenna system. Refer to paragraph3-12f(3). b. If indication in a above is normal, check interlock circuits consisting of Q1313, Q1314, Q1315 (para 3-12c(6)) and CR1319 (para 3-12d(5)).
4	No isls action; no P2 pulse output at connector J1208 (C, fig. 3-1).	Observe waveform at testpoint TP1305. Waveform should be pulses as shown in G of fig. 3-3. *a.* If waveform is absent or abnormal, refer to item 5. *b.* If normal waveform is present, check wiring between connector J1203, pin V and J1208.
5	No P2 output waveform at TP1305 (G, fig. 3-2)	Observe waveform at emitter of Q1311. Waveform sho uld be pulse as shown in F, fig. 3-3. *a.* If waveform is absent or abnormal, refer to item 6. *b.* If waveform is normal, check following: (1) Check Q1312 (para *3-12d(6)).* (2) Check transformer T1301 (para 3-12d(4)). (3) Check diodes CR1313 through CR1318 (para 3-12d(5)).
6	No P2 stop pulse present at emitter of Q1311 (F, fig. 3-3)	Observe waveform at base of Q1309. Waveform should be ramp voltage as shown in E, fig. 3-3. *a.* If waveform is absent or abnormal, refer to item 7. *b.* If normal waveform is present, check Q1309, Q1310, and Q1311.
7	No P2 stop ramp present at base of Q1309 (E, fig. 3-3)	Observe waveform at collector of Q1312. Waveform should be start pulse as shown in D, fig. 3-3. a. If waveform is absent or abnormal, refer to item 8. b. If normal waveform is present, check Q1308 and Q1309 (para *3-12d(6)).*
8	No P2 and CP start pulse at collector of Q1309 (E, fig. 3-3)	Observe waveform at emitter of Q1305. Waveform should be ramp voltage as shown in C, fig. 3-3. a. If waveform is absent or abnormal, refer to item 14. *b.* If waveform is normal, check Q1306, Q1307 (para *3-12d(6))* and CR1307 through CR1311 (para 3-12d(5)).

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
9	No isls action; P2 pulse is present at connector J1208 (C, fig. 3-1)	Observe waveform at TP1306. Waveform should be control pulse as shown in J, fig. 3-3. a. If waveform is absent or abnormal, refer to item 10. *b.* If waveform is normal, check following connections: Z1201-2 to P1205, Z1201-1 to P1206, and P1207 to CP1201.
10	No control pulse output waveform at TP1306 (J, fig. 3-3)	Observe waveform at emitter of Q1321. Waveform should be cp stop pulse as shown in I, fig. 3-3. a. If waveform is absent or abnormal, refer to item 11. *b.* If waveform is normal, check CR1325 through CR1324 (para 3-12d(5)) and T1303 (para 3-12d(4)).
11	No cp stop pulse present at emitter of Q1321 (I, fig, 3-3)	Observe waveform at base of Q1319. Waveform should be cp stop ramp as shown in H, fig. 3-3. a. If waveform is absent or abnormal, refer to item 12. *b.* If waveform is normal, check Q1319 through Q1322 (para 3-12d(6)).
12	No cp stop ramp present at base of Q1319 (H, fig. 3-3)	Observe waveform at collector of Q1322. Waveform should be start pulse as shown in D, fig. 3-3. a. If waveform is absent or abnormal, refer to item 13. *b.* If waveform is normal, check Q1318, Q1319 (para 3-12d(6)) and CR1324 (para 3-12d(5)).
13	No P2 and cp start pulse at collector of Q1322 (D, fig. 3-3)	Observe waveform at emitter of Q1305. Waveform should be ramp voltage as shown in C, fig. 3-3. *a.* If waveform is absent or abnormal, refer to item 14. *b.* If waveform is normal, check Q1316, Q1317 (para *3-12d(6))* and CR1320 through CR1324 (para *3-12d(5)).*
14	No isls action; no P2 pulse or cp pulse outputs (observed at TP1305 and TP1306 respectively); no ramp voltage at emitter of Q1305 (C, fig. 3-3)	Observe waveform at collector of Q1303. Waveform should be isls gate as shown in B, fig. 3-3. *b.* If waveform is normal, check Q1304, Q1305 (para *3-12d(6))* and CR1364 through CR1306 (para 3-12d(5)).
15	No isls gate present at collector of Q1303	Observe waveform at TP1304. Waveform should be pulse pair as shown in A, fig. 3-3. a. If waveform is absent or abnormal, check switch S1302 and relay K1301 (para *3-12d(4)).* *b.* If waveform is normal, check Q1301, Q1302, and Q1303 (para 3-12d(6)).

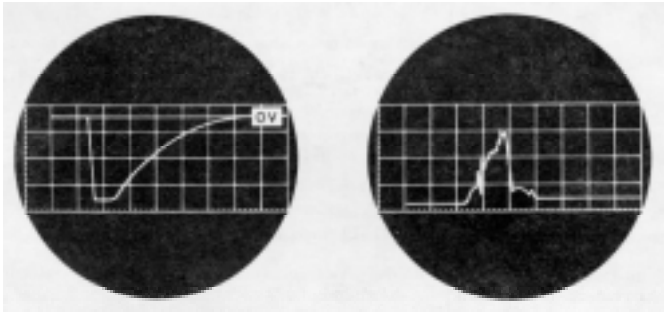
(4) Modulator, Pulse MD-638/TPX-41, de resistances of transformers, coils, and relays. The following chart lists the transformers, coils, and relay in the isls system, references a figure that shows the location of each, and gives the dc resistance of all windings when the MD-638/TPX-41 is disconnected from the AN/ TPX-41.



A CODED PAIR INPUT
TESTPOINT. TP1304
SENSITIVITY. 20
SWEEP TIME: I

B. SLS GATE
TESTPOINT 01303, COLLECTOR
SENSITIVITY: 20
SWEEP TIME 10

C. P2 DELAY RAMP
TESTPOINT Q1305, EMITTER
SENSITIVITY- 10
SWEEP TIME: 2



D. P2 AND CP START PULSE
TESTPOINT Q1312 AND 01322, COLLECTOR
SENSITIVITY: 10
SWEEP TIME 5

E. P2 STOP RAMP
TESTPOINT Q01309, BASE
SENSITIVITY. 5
SWEEP TIME: I

NOTES:

1. WAVEFORMS TAKEN WITH OSCILLOSCOPE AN/USM-140B USING TIME DELAY GENERATOR MX-2962/USM.
2. SWEEP MODE PRESET
3. TRIGGER SOURCE: EXT AC
4. DELAY FUNCTION' AS REQUIRED
5. DELAYING SWEEP TIME/CM AS REQUIRED
6. HORIZONTAL DISPLAY AS REQUIRED
7. SENSITIVITY VOLTS/CM
8. SWEEP TIME USEC/CM

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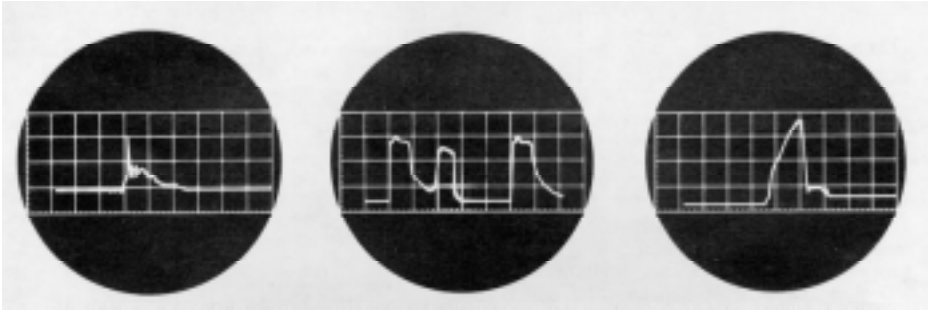
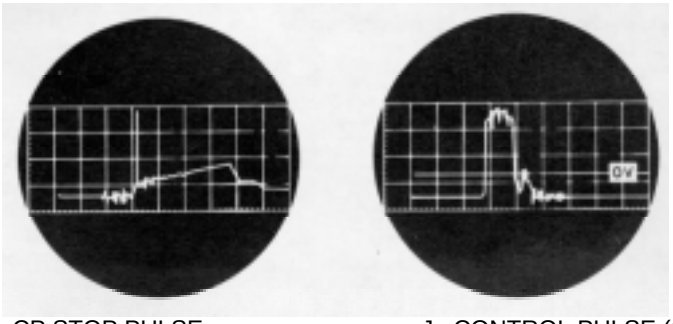
Figure 3-3 (1) . Modulator, Pulse MD-638/TPX-41, waveforms (sheet 1 of 2).



F. P2 STOP PULSE
TESTPOINT: Q1311, EMITTER
SENSITIVITY: 5
SWEEP TIME: I

G. P2 MOD (OUT)
TESTPOINT: TP1305
SENSITIVITY: 100
SWEEP TIME: I

H. CP STOP RAMP
TESTPOINT. Q01319, BASE
SENSITIVITY 5
SWEEP TIME: I



I. CP STOP PULSE
TESTPOINT: 01321, EMITTER
SENSITIVITY: 5
SWEEP TIME: I

J. CONTROL PULSE (OUT)
TESTPOINT TP1306
SENSITIVITY: 20
SWEEP TIME. I

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Figure 3-3 (2) . Modulator, Pulse MD-638/TPX-41, waveforms (sheet 2 of 2).

Transformer, coil, or relay	Location (fig.)	Terminals	Dc resistance (ohms)
T1201	3--8	1-2	4.5
		3-4	165
		4-5	170
		6-7	1.8
		7-8	1.9
L1201	3-8	1-2	115
K1301	FO-12	4-8	630
T1301	FO-12	1-4	4.2
		3-6	1.6
T1302	FO-12	1-4	3.9
		3-6	1.6
T1303	FO-12	1-2	10
		3-4	0.35

(5) *Modulator, Pulse MD-638/TPX-41, dc resistances of diodes.* The following charts list forward and reverse resistance of all diodes in the MD-638/TPX-41. Multimeter ME-26B/U or equivalent should be used to perform tests. Included in each chart is a meter scale (RX1, RX100, RX1K, etc) to be used for each particular measurement. All measurements are taken with all cables removed from the unit, and the pulse generator processor removed from the MD-638/TPX-41.

NOTE

RX1 meter scale on ME-26B/U should be used only when checking forward resistance of CR1201 through CR1210.

(a) Main chassis.

Diode	Meter scale Forward	(RX)	Meter scale Reverse	(RX)
CR1201	5.0	1	100k	10K
CR1202	5.0	1	100k	10K
CR1203	5.5	1	10k	1K
CR1204	5.5	1	10k	1K
CR1205	4.8	1	550k	10K
CR1206	4.5	1	500k	10K
CR1207	4.7	1	550k	10K
CR1208	5.5	1	100k	1K
CR1209	5.0	1	100k	1K
CR1210	5 5	1	100k	1K

(b) Pulse generator processor subassembly.

Diode	Meter scale Forward	(RX)	Meter scale Reverse	(RX)
CR1301	270	100	600	100
CR1303	300	100	30k	1K
CR1304	300	100	220k	10K
CR1305	1400	100	Inf.	
CR1306	1350	100	Inf.	
CR1307	10	100	1350	100
CR1308	310	100	25k	1K
CR1309	320	100	33k	1K
CR1310	1300	100	3800	100
CR1311	300	100	15k	1K
CR1312	310	100	15k	1K
CR1313	300	100	15k	1K
CR1315	300	100	15k	1K
CR1317	1150	100	26k	1K
CR1318	1150	100	26k	1K
CR1319	1800	100	800M	1M
CR1320	20	100	1500	100
CR1321	320	100	24k	1K
CR1322	300	100	33k	1K
CR1323	310	100	16k	1K
CR1324	300	100	16k	1K
CR1325	0	100	0	100
CR1327	300	100	16k	1K
CR1329	1150	100	26k	1K

NOTE

The diodes listed in the chart below consist of silicon-controlled switches that are contained in the pulse generator processor. To check these diodes, insure that power is removed from the MD-638/TPX-41, and remove the pulse generator processor before any measurements are attempted. Unsolder at least two leads before connecting the ME-26B/U as indicated in the chart below.

(c) Silicon-controlled switch generators.

Diode	Gate-cathode Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Gate-anode Forward	Meter scale (RX)	Reverse	Meter scale (RX)
CR1314	100	100	100	100	70 mego	1 mego	500 mego	1 mego
CR1316	0	100	0	100	80 mego	1 mego	500 mego	1 mego
CR1326	100	100	100	100	70 mego	1 mego	500	1 mego
CR1328	0	100	0	100	70 mego	1 mego	500	1 mego

(6) *Modulator, Pulse MD-638/TPX--61, dc resistances of transistors.* The forward resistance and reverse resistance of all transistors contained in the MD-638/TPX-41 are listed in the chart below. Multimeter ME-26B/U or equivalent should be used to perform these tests. Measurements are not made with, respect to ground; they are measured across the transistor junctions listed. Forward and reverse values are given in ohms. All measurements are to be made only after ac power has been removed from the MD-638/TPX-41 and the pulse generator processor subassembly has been removed.

	Base to emitter				Base to collector			
Transistor	Forward	Meter scale (RX)	Reverse	Meter scale (RX)	Forward	Meter scale (RX)	Reverse	Meter scale (RX)
Q1301	1400	100	22k	1K	1300	100	38k	1K
Q1302	1350	100	9k	1K	1200	100	22k	1K
Q1303	1400	100	68k	10K	1300	100	56k	10K
Q1304	270	100	15k	1K	260	100	380k	10K
Q1305	1300	100	350k	10K	1200	100	170k	10K
Q1306	360	100	26k	1K	1200	100	65k	1K
Q1307	1400	100	55k	10K	1250	100	40k	1K
Q1308	1400	100	30k	1K	1300	100	7.5k	1K
Q1309	1350	100	17k	1K	1250	100	18k	1K
Q1310	1350	100	9k	1K	1500	100	11k	1K
Q1311	1400	100	26k	1K	1250	100	3.8k	100
Q1312	1400	100	24k	1K	1300	100	19k	1K
Q1313	1400	100	Inf.	----------	1300	100	Inf.	
Q1314	280	100	40k	1K	270	100	600k	10K
Q1315	1200	100	140k	10K	270	100	600k	10K
Q1316	360	100	25k	1K	1200	100	56k	10K
Q1317	1400	100	55k	10K	1300	100	40k	1K
Q1318	1350	100	35k	1K	1250	100	9.5k	1K
Q1319	1400	100	1650	1K	1300	100	16k	1K
Q1320	1400	100	9k	1K	1300	100	11k	1K
Q1321	1300	100	25k	1K	1200	100	3.8k	1K
Q1322	1400	100	23k	1K	1300	100	18k	1K

(7) Modulator, Pulse MD-638/TPX-41, voltage data. The terminal voltages contained in the following charts *((a),* (b), and *(c)* below) can be observed using Multimeter ME-26B/U. Before any voltage measurements are attempted, insulate the entire test probe, except for the extreme tip, with tape or sleeving. A momentary short circuit can damage a transistor in associated circuits. The characteristics of transistors may cause a large variation of the emitter and base voltage indications whenever they are replaced. This should not affect circuit operation. Observe that collector voltages remain stable. All measurements are taken with ANTENNA connector i212 on Receiver Transmitter, Radio RT-264D/UPX-6 terminated with power attenuator Z501 and dummy load Z502. All other connections of Interrogator Set AN/TPX-41 are normal with selected control settings as indicated in paragraph 3-12d(1).

NOTE

For access to transistor terminals on the pulse generator processor, use card extender as described in paragraph *3-12d(1)(c).* Before removing the pulse generator processor from its connector or from the card extender, insure that power is removed for protection of transistors.

(a) Transistor terminal voltages.

	Voltage to ground		
Transistor	**Emitter**	**Collector**	**Base**
Q1301 (NPN)	-29.5	0	-29.5
Q1302 (NPN)	-29.5	0	-29.5
Q1303 (NPN)	-29.0	-29.0	-28.5
Q1304 (NPN)	-11.8	-28.8	-11.9
Q1305 (NPN)	-29.3	0	-28.8
Q1306 (NPN)	-29.5	0	-29.5
Q1307 (NPN)	-29.3	-29.1	-28.6
Q1308 (NPN)	-29.0	0	-28.8
Q1309 (NPN)	-20.6	-4.85	-29.0
Q1310 (NPN)	-20.6	-20.4	-20.0
Q1311 (NPN)	-21.0	0	-20.4
Q1312 (NPN)	-29.5	-29.5	-28.7
Q1313 (NPN)a	-29.5	-29.5	-28.7
Q1313 (NPN)b	-29.8	0	-29.4
Q1313 (NPN)C	-29.8	0	-30.0

Transistor	Voltage to ground		
	Emitter	Collector	Base
Q1314 (PNP)a	-17.5	-17.5	-17.8
Q1314 (PNP)b	-27.8	-27.8	-28.0
Q1314 (PNP)C	-0.08	-28.5	0
Q1315 (NPN)a	-18.2	-17.8	-17.5
Q1315 (NPN)b	-28.5	-28.0	-27.8
Q1315 (NPN)C	-29.1	0	-28.5
Q1316 (NPN)	-29.5	0	-29.5
Q1317 (NPN)	-29.3	-29.2	-28.6
Q1318 (NPN)	-29.5	0	-29.0
Q1319 (NPN)	-21.2	-4.9	-29.5
Q1320 (NPN)	-21.2	-19.2	-20.5
Q1321 (NPN)	-19.5	0	-19.2
Q1322 (NPN)	-29.5	-0.03	-29.1

[a] Normal load on CP1201.
[B] CP1201 open circuit.
[C] CP1201 short circuit.

(b) Silicon-controlled switch generator terminal voltages.

Silicon-controlled switch generator	Voltage to ground		
	Cathode	Gate	Anode
CR1314	0	0	+250
CR1316	+0.16	+0.16	+250
CR1326	0	0	+250
CR1328	0	0	+250

(c) Power supply voltage checks.

Junction -	Voltage to ground
CR1201, CR1202, L1201----------	+310
L1201, C1201, R1201----------	+300
R1201, CR1205, R1202, C1202----	+250
CR1205, CR1206----------	+200
CR1206, CR1207 ----------	+103
CR1203, CR1204, C1203, R1203--	-56.5
R1203, CR1208, R1204, C1204---	-29.9
CR1208, CR1209 ----------	-19.6
CR1209, CR1210 ----------	-9.9

e. Receiver-Transmitter, Radio RT-264D/ UPX-6. Direct Support Troubleshooting. For information pertaining to the troubleshooting of Receiver-Transmitter, Radio RT-264D/UPX-6, refer to TM 11-5895-245-35.

f. *Antenna Group AN/GPA-119, Direct Support Troubleshooting.* Direct support troubleshooting of the AN/GPA-119 consists of tracing troubles to the discrete component level with available test equipment. A prerequisite requires that the AN/GPA-119 be properly installed in an operable AN/TPX-41 system. The instructions in (1) below cover preparational procedures that should be accomplished prior to troubleshooting the AN/GPA-119. Parts location diagrams for the AN/GPA-119 are listed in (2) below. The Antenna Group AN/GPA-119, direct support troubleshooting chart, contained in (3) below, lists trouble symptoms, indicates the probable trouble for the " / symptom, and provides checks and corrective measures to remedy the problem. The dc resistance and continuity data contained in (4) below provides supporting information to aid in identifying defective parts.

(1) *Antenna Group AN/GPA-119, preparation for troubleshooting.* To accomplish effective troubleshooting of the AN/GPA-119, follow the preparational instructions given below.

(a) When properly installed, Antenna Group AN/GPA-119 is accessible for troubleshooting without extensive disassembly. For access to components located within the RF switch enclosure, remove 12 screws, lockwashers, and flat washers that secure the RF switch chassis to the enclosure and remove the RF switch chassis.

(b) On Coder-Control KY-97C/TPX, place POWER switch (S407) to ON, CHALLENGE , switch (S404) to ON, and LOCAL-REMOTE switch (S402) to REMOTE.

(c) On Modulator, Pulse MD-638/TPX-41, place POWER switch (S1301) to ON, and SLS switch (S1302) to ON.

(d) On Receiver-Transmitter, Radio RT-264D/TPX-6, place POWER switch (S104) to ON.

(e) On Control, Remote Switching C-1271A/TPX-22, place MODE SELECTOR switch (S701) to position 2, RECEIVER GAIN control (R701) to 10, GTC switch (S703) to LONG, and CHOP switch (S702) to OFF.

(f) On Control, Remote Switching C-7014/TPX-44, place BEACON ASSIST switch (S40306) to OFF, EMER-OFF switch (S40304) to OFF, and BRACKET-OFF switch (S40305) to BRACKET.

(g) On Blanker, Interference MX-8795/TPX-41, place POWER switch

(S31101) to ON, and PROCESSED VIDEO-RAW VIDEO switch (S31102) to RAW VIDEO.

(h) On Decoder, Video KY-593/TPX-44, place POWER switch (S201) to ON.

(i) On Interconnecting Box J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON, SCAN switch S8601 to ON, and IFF SCAN switch S8602 to OPERATE.

(2) *Antenna Group AN/GPA-119, parts location illustrations.* Figures containing parts location information for the components of Antenna Group AN/GPA-119 consist of the follow ing:

(a) Pedestal, Antenna AB-1158/GPA119 (fig. 5-1).

(b) Antenna AS-1796/GPA-119 (fig. 3-11).

(c) RF switch S1001 (fig. 3-12).

WARNING

When working near Antenna AN/GPA119, insure that IFF SCAN switch S8602 on Interconnecting Box J-2945/TPX-41 is placed to SAFE. Antenna rotation may endanger personnel.

(3) Antenna Group AN/GPA-119, direct support troubleshooting chart.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
1	Antenna AS-1796/GPA-119 rotates slower than 15 rpm	Low ac input voltage. Check ac input voltage. *a.* Remove side panel from Interconnecting Box J-2945/TPX-41 and check for 117 vac between terminals 6 and 9 of TB8601. *b.* If abnormal, check voltage output of ac power generator to insure proper voltage is being generated. *c.* If normal, check for 117 vac across pins H and G of connector P20004. *d.* If indication in c above is abnormal, check cables W9406 and W9207. Defective antenna drive motor B20002. Check antenna dr ive motor B20002. *a.* Measure dc resistance of motor windings (para 3-12f(4)). *b.* If abnormal, replace antenna drive motor B20002. *c.* If normal, remove motor and check that main drive shaft rotates freely. *d.* If shaft does not rotate freely, replace motor.
2	IFF replies do not appear at the same azimuth of associated radar targets	Antenna synchro alignment incorrect. Perform Antenna Group AN/GPA-119, synchro alignment as instructed in para 3-23.
3	No isls replies appear on associated ppi indicators	On Modulator, Pulse MD-638/TPX-41, place ISLS switch S1302 to OFF. On MD-638/TPX-41, measure dc voltage at CP testpoint TP1303. Normal indication is +250v. *a.* If abnormal, check MD-638/TPX-41 (para 3-12d(3)). *b.* If normal, check interconnecting cabling. *c.* If abnormal, replace defective cable. If normal, on Antenna AS-1796/GPA-119, remove RF switch S1001 and connector P1101. Check for continuity between center conductor and shell on diplexer Zl101 connector Z1-1. Normal indication is infinity. *a.* If abnormal, replace RF switch S1001. *b.* If normal, remove connector P1102, check for continuity between center conductor and shell on diplexer Zl101 connector Z1-2. Normal indication is infinity.

Item No.	Trouble symptom	Probable trouble; checks; and corrective measures
		c. If abnormal, replace RF switch S1001. *d.* If normal, remove connectors P1103 and P1104 and measure the resistance from center conductor of connector P1101 to center conductor of connector P1103. Normal indication is 270 ohms. e. If abnormal, replace RF switch S1001. f. If normal, measure the resistance from center conductor of connector P1101 to center conductor of connector P1104. Normal indication is 470 ohms. g. If abnormal, replace RF switch S1001. *h.* If normal, measure for continuity between center conductor of connector P1101 and ground (red lead of multimeter to ground). Normal reading is infinity. *i.* If abnormal, replace RF switch S1001. j. If normal, perform antenna radiation test (para 4-11). k. If abnormal, replace Antenna AS-1796/GPA-119.
4	Intermittent replies	Check all cable connections between Antenna AS-1796/GPA-119 and associated equipment. If normal, on Pedestal, Antenna AB-1158/GPA-119, remove connectors J20001 and CP21001 from rotary joint E20001 and measure for continuity across center conductor of rotary joint. Normal indication is zero. a. If abnormal, replace rotary joint E20001. *b.* If normal, measure for continuity between center conductor and shell of rotary joint E20001. Normal indication is infinity. c. If abnormal, replace rotary joint E20001.
5	Antenna AS-1796/GPA-119 radiation pattern weak in intensity and power.	Poor cable connections, defective RF switch S1001, defective rotary joint E20001. Check cable connections. a. If normal, check RF switch S1001 (item 3). *b.* If normal, check rotary joint (item 4).
6	Pedestal Antenna AB-1158/GPA-119 is noisy during rotation.	Insufficient bearing lubrication or defective antenna drive motor B40103. Remove antenna drive motor B20002 and inspect bearings for excessive wear and sufficient lubrication.

(4) *Antenna Group AN/GPA119, dc resistances.* The following chart provides dc resistance and continuity information to aid in identifying defective components in Antenna Group AN/GPA119. All resistance readings are taken with external cables removed from the AB1158/GPA119, using Multimeter ME26B/U.

Component	Points of test	Dc resistance (ohms)
Synchro transmitter B20001	Connector J20004:	
	Pin E to D	100
	Pin A to B.....	94
	Pin B to C	94
	Pin C to A	94

Component	Points of test	DC resistance (ohms)
Antenna drive motor B20002	Connector P20001:	
	Pin A to D	1.3
	Pin B to C	6
	Pin A to B.....	infinite
Relay Relay K20001	Connector J20004-H to Connector J20001-A	0
Rotary joint	Center conductor of connector J20003 to center conductor connector CP21001.	
	Center conductor of connector J20003 to outer shell	Infinite

g. Decoder, Video KY-593/TPX-44, Direct Support Troubleshooting. For information pertaining to the troubleshooting of Decoder, Video KY-593/TPX-44, refer to TM 11-5840-309-35.

h. Control, Remote Switching C-7014/TPX-44, Direct Support Troubleshooting. For information pertaining to the troubleshooting of Control, Remote Switching C-7014/TPX-44, refer to TM 11-5840-309-35.

i. Simulator, Radar Signal SM-472/TPX-44, Direct Support Troubleshooting. For information pertaining to the troubleshooting of Simulator, Radar Signal SM-472/TPX-44, refer to TM 11-5840-326-35.

j. Interconnecting Box J-2945/TPX-41, Direct Support Troubleshooting. Direct support troubleshooting of the J-2945/TPX-41 consists of tracing troubles to the discrete component level. A prerequisite requires that the J-2945/TPX-41 be properly installed in an operable AN/TPX-41 system. The instructions in (1) below cover preparational procedures that should be accomplished prior to troubleshooting the J-2945/TPX-41. The Interconnecting Box J-2945/TPX-41 direct support troubleshooting chart, contained in (2) below, lists trouble symptoms, indicates the probable trouble for the symptom, and provides checks and corrective measures to remedy the problem. The resistance data contained in (3) below provides supporting information to aid in identifying troubles. Locations of parts within the J-2945/TPX-41 are shown in figure 3-13.

(1) *Interconnecting Box J-2945/TPX-41, preparation for troubleshooting.* To accomplish effective troubleshooting of the J-2945/TPX-41, follow the preparational instructions given below.

(a) Remove J-2945/TPX-41 from side of IFF equipment rack by removing four attaching screws, flat washers, lockwashers, and nuts.

(b) Place J-2945/TPX-41 on suitable work area leaving external cables connected.

(c) Remove eight screws and flat washers that secure side panel of J-2945/TPX-41 and remove side panel. This should expose all internal components of J-2945/TPX-41 to facilitate troubleshooting.

(d) Make preliminary control settings and perform starting procedure as described in TM 11-5895-479-12.

(2) *Interconnecting Box J--2945/TPX--41, direct support troubleshooting chart.*

Item No.	Trouble symptom	Probable trouble, checks, and corrective measures
1	Pedestal, Antenna AB-1158/GPA-119 receives no ac antenna drive voltage and components of Interrogator group located at receiver-transmitter site receive no ac power inputs	Poor connection at connector J8603, IFF POWER circuit breaker CB8601 defective. a. Check for proper mating of connectors J8603 and P8603. *b.* Check circuit breaker CB8601 (para 3-12j(3)). *c.* If *a* and *b* above are normal, check power source.

Item No.	Trouble symptom	Probable trouble, checks, and corrective measures
2	Pedestal, Antenna AB-1158/GPA-299 receives no ac antenna drive voltage. Components of interrogator group located at receiver-transmitter site receive normal ac power inputs.	Check antenna drive voltage output by measuring across pins H and J on rear side of connector J8601. Normal indication is 117 vac. *a.* If normal, trouble exists in cabling between J-2945/TPX-41 and Pedestal, Antenna AB1158/GPA119. *b.* If abnormal, check relay K8601 (para 3-12j(3)). *c.* If relay K8601 is good, check switches S8601 and S8602 (para3-12j(3)). *d.* If switches S8601 and S8602 are good, check circuit breaker CB8601 (para 3-12j(3)).
3	Components of interrogator group located at receiver-transmitter site receive no ac power inputs. Pedestal, Antenna AB-1158/GPA-119 Receives normal ac antenna drive voltage	Check for 117 vac between following points to determine if proper ac voltage outputs are present: *a.* Check between terminals 5 and 7 of terminal board TB8601. *b.* Check between terminals 4 and 9 of terminal board TB8601. *c.* Check between terminals 4 and 8 of terminal board TB8601. *d.* If any of all checks performed in a, *b,* and c above are normal, check TB8601 wiring per fig. FO-8. *e.* If all checks performed in *a, b,* and c above are abnormal, check circuit breaker CB8601 (para 3-12j(3)).

(3) Interconnecting Box J-2945/TPX-41, dc -TPX-41. *resistances.* The following chart provides dc resistance and continuity information to aid in identifying defective components in the J-2945/. All resistance readings are taken with external cables removed from the unit, using Multimeter ME-26B/U.

Component	Switch position	Points of test	Dc resistance (ohms)
IFF POWER circuit breaker CB8601	OFF	J8603-A to TB8601-5	Infinite
		J8603-A to TB8601-6	Infinite
	ON	J8603-A to TB8601-5	0
		J8603-A to TB8601-6	0
Relay K8601	.....	K8601-X1 to K8601-X2	170
SCAN switch S8601.....	OFF	J8601-C to J8601-G	Infinite
	ON	J8601-C to J8601-G	0
IFF SCAN switch S8602	OFF	J8601-G to K8601-X2	Infinite
	ON	J8601-G to K8601-X2	0

Section III. ADJUSTMENT AND ALIGNMENT PROCEDURES

3-13. General

This section covers direct support adjustment and alignment procedures required to assure optimum performance of Interrogator Set AN/TPX41. To accomplish the procedures contained within this section, it is required that the major component undergoing adjustment be properly installed in an operable AN/TPX41 system. Major components of the AN/TPX41 are listed in *a* through j below with references to paragraphs covering adjustment and alignment procedures.

a. Blanker Interference MX8795/TPX41 (para, 3-14 through 3-16).

b. Coder-Control KY-97C/TPX (para 3-17).
c. Control. Remote Switching C-1271A1 TPX22 (para 3-18).
d. Modulator, Pulse MD-638/PTX-41 (para 3-19 through 3-21).
e. Receiver-Transmitter, Radio RT264D / UPX-6 (para 3-22).
f. Antenna Group AN/GPA-119 (para 3-23).
g. Decoder, Video KY-593/TPX-44 (para 324).
h. Control. Remote Switching C-7014/TPX44 (para 3-25).
i. Simulator. Radar Signal SM-472/TPX-41 (para 3-26).
j. Interconnecting Box J-2945 / TPX-41 (para 3-27i).

3-14. Blanker, Interference MX-8795/TPX41, Positive 15-Volt Power Supply Adjustment

a. Test Equipment Required. Multimeter ME-26B / U.

b. Equipment Conditions.

(1) On MX-8795 / TPX-41, POWER switch (S31101) placed to ON.

(2) On Interconnecting Box J-2945/TPX41, IFF POWER circuit breaker CB8601 placed to ON.

c. Procedure. To adjust the + 15-volt output on PS31101, proceed as follows:

(1) Connect Multimeter ME-26B/U between PWR SUP COM testpoint TP3110 and +15V testpoint TP31102.

NOTE

Before adjusting + 15V ADJ, loosen adjustment locknut. After adjustment locknut finger-tight and verify that voltage indication does not change.

(2) On front panel of MX-8745/TPX-41, adjust +15V ADJ (R31101) for a +15-volt indication on ME-26B / U.

(3) Move ME-26B / U test lead and observe that voltage present at: ± 1 OV testpoint TP31104 is 10'+ I volts, ±6V testpoint TP 31106 is 6i+0.5 volts, and at +3.3V testpoint TP31108 is 3.3 ±0.25 volts.

3-15. Blanker, Interference MX-8795/TPX41, Negative 15-Volt Power Supply Adjustment

a. Test Equipment Required. Multimeter ME26B / U.

b. Equipment Conditions;.

(1) On MX-8795 / TPX-41, POWER switch S31101) placed to ON.

(2) On Interconnecting Box J-2945/TPXTM 11-5895-479-35 41. IFF POWER circuit breaker CB8601 placed to ON.

c. Procedure. To adjust the -15-volt output of PS31102. proceed as follows: (1) Connect Multimeter ME-26B/U between PWR SUP COM testpoint TP31101 and 15V testpoint TP31103.

NOTE

Before adjusting-15V ADJ, LOOSEN ADJUSTMENT LOCKNUT. After adjustment is completed. tighten adjustment locknut finger-tight and verify that voltage indication does not change.

(2) On front panel of MX-8745/TPX-41, adjust -15V ADJ (R31102) for -15-volt indication on ME-26B/ U.

(3) Move ME-26B / U test lead and observe that voltage present at -6V testpoint TP31107 is -6 ±0.5 volts and -10V testpoint TP31105 is -10 ±1 volts.

3-16. Blanker, Interference MX8795 / TPX-41, Timing Adjustment

a. Test Equipment Required. Oscilloscope AN/USM-140B (para 3-10), including MX2962 / USM subassembly.

b. Equipment Conditions.

(1) On MX-8795/TPX-41, release four captive screws on front panel and slide chassis forward from dust cover to expose testpoints on circuit cards.

(2) On MX-8795/TPX-41, place POWER switch (S31101) to ON.

(3) On Interconnecting Box J-2945/TPX41, place IFF POWER circuit breaker CB8601 to ON.

c. Procedure. To adjust timing pulses and gates in the MX-8795/TPX-41 for proper time relationships, proceed as follows:

(1) On AN/USM-140B, place TRIGGER SOURCE to EXT DC and connect CHANNEL A INPUT to PRE TRIG testpoint TP30903 on trigger/gate generator subassembly. On MX8795 / TPX-41, install adapter UG-274B / U on DISPLAY TRIGGER connector J31106 and connect one side of adapter to TRIGGER SOURCE input on AN / USM-140B.

(1.1) On MX-4795 / TPX-41, set PRF SEL switch S3 to position 2.

(2) On MX-8795 / TPX-41, adjust PW ADJ control R30907 until pretrigger pulse width (at 50percent points) is 0.4 μsec (fig. 3-2).

(3) On processor subassembly, connect AN/USM-140B to IFF ENABLE testpoint TP30807.

(4) On trigger/gate generator subassembly, adjust IFF GATE control R30920 until 2450 μsec negative pulse (fig. 32) is observed in (3) above.

(5) On trigger/gate generator subassembly, connect AN / USM140B to CP GATE testpoint TP30904.

(6) Adjust CP GATE control R30936 until 2550 sec positive gate (fig. 32) is observed in (4) above.

(7) On AN/ USM140B, move CHANNEL A INPUT to DLYD TRIG testpoint TP30905 on trigger/ gate generator subassembly.

(8) On trigger / gate generator subassembly, observe that DELAY ADJ control R30942 will adjust trigger delay between 70 and 110 μsec from start of sweep. Final adjustment should be completed during system alignment to attain range separation of 1/2 mile between IFF video and radar video on associated radar ppi indicator.

NOTE

If no operational adjustment is required, adjust R30942 for a delay of 90 μsec.

(9) On AN / USM140B, move Channel A INPUT to DELAY GATE testpoint TP31002 on synchronizer-multiplier subassembly.

(10) Verify that a square wave similar to that shown in M, figure 32 is present. Final adjustment of DELAY ADJ R31017 should be made during system alignment.

(11) On AN/ USM140B, install adapter UG274B/U on CHANNEL A INPUT con336 Change 1 nector. Connect one side of adapter to 1500 CPS testpoint TP31004 on synchronizer-multiplier subassembly and connect other side of adapter to INPUT on AN / USM207.

(12) On AN/USM207, place power switch to TRACK, FUNCTION switch to FREQ, GATE TIME control to 101, and observe readout display. Readout should be 1492 to 1508 Hz.

(13) On synchronizer-multiplier subassembly, adjust FREQ control R31024 for maximum amplitude of 1500Hz sine wave displayed on AN / USM140B while insuring that frequency remains within limits specified in (12) above. If clipping occurs, decrease sine wave amplitude using LEVEL control R31037, and continue adjustment of FREQ control R31024 for maximum amplitude of sine wave.

(14) On synchronizer-multiplier subassembly, adjust LEVEL control R3 1037 for small amount of clipping of 1500Hz sine wave. While observing 1500Hz sine wave, adjust BAL control R31039 for symmetrical clipping of sine wave.

(15) After adjustment of BAL control R31039, readjust LEVEL control R31037 for maximum amplitude of sine wave with no clipping.

Sine wave amplitude should be 20 volts peak-to-peak minimum.

(16) Turn off and disconnect all test equipment and restore MX8795/TPX41 to service.

3-17. Coder Control KY97C/TPX, Adjustment and Alignment Procedures

For information regarding the alignment and adjustment of Coder Control KY97C/TPX, refer to TM 11589520135.

3-18. Control, Remote Switching C1271A/ TPX22, Adjustment and Alignment Procedures

Control, Remote Switching C1271A/TPX22 requires no internal adjustment. All adjustments are accomplished through the use of the operating controls located on the front panel. Instructions for setting these controls to comply with operational requirements are given in TM 11589547912.

NOTE

Adjustment procedures for Modulator, Pulse MD638/TPX41, given in paragraphs 319, 320, and 321 are interacting. These adjustments should be performed in the sequence given.

3-19. Modulator, Pulse MD638/TPX41, P2 Pulse Timing Adjustment

a. Test Equipment Required.

(1) Oscilloscope AN/USM140B.

(2) Time Delay Generator MX2962/USM.

(3) Test Set, Radar AN/UPM6B.

b. Equipment Conditions.

(1) Remove MD638/TPX41 from wall of S70/G Shelter by removing six attaching screws and place unit on suitable work area.

(2) On MD638/TPX41, remove perforated dust cover by removing eight attaching screws, flat washers, and lockwashers that secure perforated dust cover during normal operation.

(3) The MD638/TPX41 contains one plugging circuit card; pulse generator processor (chassis series No. 1300). Access to components on this circuit card necessitates use of locally fabricated card extender. To use card extender, remove TM 11589547935 ac power to MD638/TPX41, release two snaplock fasteners on pulse generator processor, remove pulse generator processor and install card extender in its place. Install pulse generator processor in connector located on top of card extender.

CAUTION

For protection of transistors, before removing the pulse generator processor or the card extender, insure that power is removed.

(4) On Receiver Transmitter, Radio RT264D/UPX6, install power attenuator Z501 and dummy load Z502 on ANTENNA connector J212.

(5) On Coder Control KY97C/TPX, place POWER switch (S407) to ON, CHALLENGE switch (S404) to ON, and LOCALREMOTE switch (S402) to REMOTE.

(6) On RT264D/UPX6, place POWER switch (S104) to ON.

(7) On Control, Remote Switching C1271A/TPX22, place MODE SELECTOR switch (S701) to position 2, RECEIVER GAIN control (R701) to 10, GTC switch (S703) to LONG, and CHOP switch (S702) to OFF.

(8) On Blanker, Interference MX8795/TPX41, place POWER switch (S31101) to ON, and PROCESSED VIDEORAW VIDEO switch (S31102) to RAW VIDEO.

(9) On Decoder, Video KY593/TPX44, place POWER switch (S201) to ON.

(10) On MD638/TPX41, place SLS switch (S1302) to ON.

(11) On Interconnecting Box J2945/TPX41, place IFF POWER circuit breaker CB8601 to ON, insure that SCAN switch S8601 is placed to OFF, and IFF SCAN switch is placed to SAFE.

c. Procedure. To adjust for proper timing of the P2 pulse, proceed as follows:

(1) On Receiver-Transmitter, Radio RT-264D/UPX-6, temporarily disconnect connector P213 from RF PROBE MID BAND ATTEN connector J213. Connect cable W703 supplied with Test Set, Radar AN/UPM-6B between J213 and RF IN connector on AN/UPM-6B.

(2) On Oscilloscope AN/USM-140B, connect CHANNEL A INPUT to CP testpoint TP1306 on MD-638/TPX-41.

(3) On AN/USM-140B, using cable CG-409E/U (part of AN/USM-140B) connect CHANNEL B INPUT to connector UG-274G/U installed on VIDEO OUT connector of AN/UPM6B. Connect Dummy Load, Electrical DA-232/U to open terminal of UG-274B/U.

(4) On AN/USM-140B, using cable CG-409E/U, connect TRIGGER SOURCE INPUT to second UG-274B/U installed on CODED PAIR IN connector J1202. Insure that cable assembly W32107 is installed on other receptacle of UG274B/U.

(5) On Coder-Control KY-97C/TPX, place LOCAL-REMOTE switch S402 to LOCAL, MODE SELECTOR switch S403 to 1, and CHALLENGE switch S404 to ON.

(6) On Modulator, Pulse MD-638/TPX-41, insure that SLS switch S1302 is placed to ON.

(7) On AN/USM-140B, at CHANNEL B, adjust controls to display transmitted pulse train of normal MODE 1 pulse pair from coding system with P2 pulse interposed between them.

(8) On MD-638/TPX-41, adjust P2 DELAY ADJ control R1315 until half-amplitude points (50 percent) on leading edges of pulses P1 and P2 are 1.9 , usec apart.

(9) When this adjustment is satisfactory, complete adjustments described in paragraphs 3-20 and 3-21 below.

3-20. Modulator, Pulse MD-638/TPX-41, P2 Pulse Width Adjustment

a. Test Equipment Required.

(1) Oscilloscope AN/USM-140B.

(2) Time Delay Generator MX-2962/USM.

(3) Test Set, Radar AN/UPM-6B.

b. Equipment Condition. Same as specified in paragraph 3-19b.

c. Procedure. To adjust for proper pulse width of the P2 pulse, proceed as follows:

(1) On Receiver-Transmitter, Radio RT-264D/UPX-6, temporarily disconnect connector P213 from RF PROBE MID BAND ATTEN connector J213. Connect cable W703 supplied with Test Set, Radar AN/UPM-6B between J213 and RF IN connector on AN/UPM-6B.

(2) On Oscilloscope AN/USM-140B, connect CHANNEL A INPUT to CP testpoint TP1306 on MD-638/TPX-41.

(3) On AN/USM-140B, using cable CG-409E/U (part of AN/USM-140B), connect CHANNEL B INPUT to connector UG-274B/U installed on VIDEO OUT connector of AN/UPM6B. Connect Dummy Load, Electrical DA-232/U to open terminal of UG-274B/U.

(4) On AN/USM-140B, using cable CG-409E/U, connect TRIGGER SOURCE INPUT to second UG-274B/U installed on CODED PAIR IN connector J1202. Insure that cable assembly W9002 is installed on other receptacle of UG274B/U.

(5) On Coder-Control KY-97C/TPX, place LOCAL-REMOTE switch (S402) to LOCAL, MODE SELECTOR switch (S403) to 1, and CHALLENGE switch (S404) to ON.

(6) On Modulator, Pulse MD-638/TPX-41, ensure that SLS switch (S1302) is placed to ON.

(7) On AN/USM-140B, at CHANNEL B, adjust controls to display transmitted pulse train of normal MODE 1 pulse pair from coding system with P2 pulse interposed between them.

(8) On MD638/TPX41, adjust P2 PULSE WIDTH ADJ control R1321 until half-amplitude point (50 percent) is 0.7 μsec wide. If trailing edge of P2 pulse overlaps P3 pulse, reduce P2 pulse width until trailing edge of P2 pulse has time to reach baseline.

(9) When adjustment of P2 PULSE WIDTH ADJ control R1321 is normal, proceed to paragraph 3--21 and complete isls system adjustments.

3-21. Modulator, Pulse MD-638/TPX-41, Control Pulse Delay Adjustment

a. Test Equipment Required.

(1) Oscilloscope AN/USM-140B.

(2) Time Delay Generator MX-2962/USM.

(3) Test Set, Radar AN/UPM-6B.

b. Equipment Conditions. Same as specified in paragraph 3-19b.

c. Procedure. To adjust control pulse for the proper delay, proceed as follows:

(1) On Receiver-Transmitter, Radio RT-264D/UPX-6, temporarily disconnect connector P213 from RF PROBE MID BAND ATTEN connector J213. Connect cable W703 supplied with Test Set, Radar AN/UPM-6B between J213 and RF IN connector on AN/UPM-6B.

(2) On Oscilloscope AN/USM-140B, connect CHANNEL A INPUT to CP testpoint TP1306 on MD-638/TPX-41.

(3) On AN/USM-140B, using cable CG-409E/U (part of AN/USM-140B), connect CHANNEL B INPUT to connector UG-274B/U installed on VIDEO OUT connector of AN/UPM6B. Connect Dummy Load, Electrical DA-232/U to open terminal of UG-274B/U.

(4) On AN/USM-140B, using cable CG-409E/U, connect TRIGGER SOURCE INPUT to second UG-274B/U installed on CODED PAIR IN connector J1202. Insure that cable assembly W9002 is installed on other receptacle of UG-274B/U.

(5) On Coder-Control KY-97C/TPX, place LOCAL-REMOTE switch (S402) to LOCAL, MODE SELECTOR switch (S403) to 1, and CHALLENGE switch (S404) to ON.

(6) On Modulator, Pulse MD-638/TPX-41, ensure that SLS switch (S1302) is placed to ON.

(7) On AN/USM-140B, at CHANNEL B, adjust controls to display transmitted pulse train of normal MODE 1 pulse pair from coding system with P2 pulse interposed between them.

(8) On AN/USM-140B, observe CHANNEL B INPUT during adjustment of HORIZONTAL POSITION control. For reference, locate half-amplitude point (50 percent) on trailing edge of P2 pulse at a vertical grid line.

(9) On MD-638/TPX-41, rotate CP DELAY ADJ control R1343 as required, and observe AN/USM-140B, at CHANNEL A INPUT that trailing edge of control pulse is coincident with vertical grid line referenced in (8) above.

(10) On KY-593/TPX-44, place CHALLENGE switch S404 to OFF. On AN/USM-140B, remove all input cables from test circuit and store both UG-274B/U and DA-232/U.

(11) On AN/UPM-6B, remove cable W703 connected between RF IN connector and RF PROBE MID BAND ATTEN connector J213 on RT-264D/UPX-6. On RT-264D/UPX-6, replace connector P213 on RF PROBE MID BAND ATTEN connector J213, and restore MD-638/TPX-41 to service.

3-22. Receiver-Transmitter, Radio RT-264D/ UPX-6, Adjustment and Alignment Procedures

For information regarding the alignment and adjustment of Receiver-Transmitter, Radio RT-264D/UPX-6, refer to TM 11-5895-245-35.

3-23. Antenna Group AN/GPS-119, Synchro Alignment

a. Test Equipment. Boresite telescope.

b. Equipment Conditions. Interrogator Set AN/TPX-41 and Radar Set AN/FPN-40 in normal operation.

c. Procedure. Instructions for orienting Antenna Group AN/GPA-119 and aligning the antenna synchro are given in (1) and (2) below.

NOTE

Orientation and synchro alignment of radar Antenna Group OA-2666/FPN-40 must be accomplished prior to orientation of IFF Antenna Group AN/GPA-119.

(1) *Antenna positioning.* Prior to any electrical alignment in the IFF antenna synchro system, the IFF and radar antennas must be positioned to point in the same direction. This is easily accomplished by establishing an azimuth reference point and physically positioning both antennas to point directly at this reference point. Instructions for establishing an azimuth reference point and positioning the radar and IFF antennas are given in (a) through (m) below.

(a) On SB-1116/FPN-40, place SCAN ON-OFF switch to OFF.

(b) On J-2945/TPX-41, place SCAN ON-OFF switch to OFF.

(c) Mount boresite telescope on radar azimuth Antenna AS-1079/FPN-40.

NOTE

For the purposes of the following steps, an azimuth reference point may be an easily identifiable, fixed geographical feature of the surrounding area that is located at least 1 mile from the radar antenna.

(d) Site through boresite telescope and physically rotate radar azimuth Antenna AS1079/FPN-40 until suitable azimuth reference point is encountered.

(e) Carefully position radar azimuth Antenna AS-1079/FPN-40 so that vertical crosshair of boresite telescope bisects azimuth reference point.

(f) Taking care not to move antenna, remove boresite telescope from radar azimuth Antenna AS-1079/FPN-40.

(g) Install boresight telescope on telescope mount located on side of Pedestal, Antenna AB1158/GPA-119 support casting.

(h) Loosen six screws that secure Pedestal, Antenna AB-1158/GPA-119 to mounting fixture just enough so that pedestal may be rotated.

(i) Site through boresight telescope and position Pedestal, Antenna AB-1158/GPA-119 so that telescope vertical crosshair bisects azimuth reference point established in (*e)* above.

(j) Tighten six pedestal mounting screws (loosened in *(h)* above) and site through boresight telescope to verify that Pedestal, Antenna AB1158/GPA-119 has not shifted position.

(k) Remove boresight telescope from Pedestal, Antenna AB-1158/GPA-119.

(l) At top of Pedestal, Antenna AB1158/GPA-119, locate two reference marks: one on rotating section of pedestal and one on stationary section of pedestal adjacent to rotating section.

(m) Position Antenna AS-1796/GPA-119 so marks identified in (1) above are aligned.

NOTE

Take care to prevent movement of the IFF and radar antennas.

(2) *IFF sweep orientation.* Perform following *(a)* through *(k)* below to align the IFF synchro and orient the IFF sweep.

(a) On SN-386/FPN-40, place IFF ONOFF switch to ON and RANGE NAUTICAL MILES switch to SEARCH 200.

(b) Inside SN-386/FPN-40 on chassis deck just behind RANGE NAUTICAL MILES switch, adjust VERT IFF ADJ and HORIZ IFF ADJ controls to center origin of 200-mile IFF sweep.

(c) Place RANGE NAUTICAL MILES switch to SEARCH 5. Inside SN-386/FPN-40, adjust VERT IFF OFF CENTERING and HORIZ IFF OFF CENTERING controls to center origin of 5-mile sweep.

(d) Repeat *(b)* and *(c)* above until sweep origins remain centered when RANGE NAUTICAL MILES switch is placed alternately to 5and 200-mile position.

(e) Establish communication between indicator and Antenna Group AN/GPA-119, and have one man remain at indicator to observe sweep presentations.

(*f*) At Pedestal, Antenna AB-1158/ GPA-119, remove cover from synchro B20001 and manually rotate synchro until IFF sweep is superimposed on radar sweep at indicator. Reinstall cover on synchro B20001.

(g) On SB-1116/FPN-40, place SCAN ON-OFF switch to ON.

(h) On J-2945/TPX-41, place SCAN ON-OFF switch to ON and insure SCAN switch is placed to OPERATE.

(i) At radar indicator, select responding aircraft target that is moving directly inbound or outbound in relation to site.

(j) IFF response (arc) should be centered directly behind radar return.

(k) If IFF response is not centered directly behind radar return, readjust IFF synchro to attain requirements of (j) above.

3-24. Decoder, Video KY-593/TPX-44, Adjustment and Alignment Procedures

For information regarding the alignment and adjustment of Decoder, Video KY-593/TPX-44, refer to TM 11-5840-309-35.

3-25. Control, Remote Switching C-7014/ TPX-44, Adjustment and Alignment Procedures

Control, Remote Switching C-7014/TPX-44 requires no internal adjustment. All adjustments are accomplished through the use of the operating controls located on the front panel. Instructions for setting these controls to comply with operational requirements are given in TM 11-5895-479-12.

3-26. Simulator, Radar Signal SM-472/ TPX-41, Adjustment and Alignment Procedures

For information regarding the alignment and adjustment of Simulator, Radar Signal SM-472/TPX-41, refer to TM 11-5840-326-35.

3-27. Interconnecting Box J-2945/TPX-41, Adjustment and Alignment Procedures

Interconnecting Box J-2945/TPX-41 requires no adjustment. The switches located on the front panel of the unit control application of ac system power and antenna drive voltage. Functional operation of these switches is described in TM 11-5895-479-12.

Section IV. REPAIR PROCEDURES

3-28. General

This section contains instructions for performing various repair operations on components of Interrogator Set AN/TPX-41. The specific repair operations covered in this section are listed in a through d below with references to paragraphs that provide pertinent instructions for each type of repair operation.

a. Electric component repair (para 3-29).

b. Mechanical parts repair (para 3-30).

c. Coaxial cable repair (para 3-31).

d. Multiconductor cable repair (para 3-32).

3-29. Electronic Component Repair

Most malfunctions that occur in the major components of the AN/TPX-41 are due to the failure of discrete electronic parts. These parts generally are not economically repairable. For this reason, repair of the major components in the AN/TPX41 is usually accomplished by replacement of defective electronic parts. Detailed instructions covering replacement of electronic parts are given in a through b below.

a. Before a part is unsoldered, note the position of the leads. If a part such as the power transformer or a switch has a number of connections, tag each of the leads to insure proper connections when replacing the part. Be careful not to damage

other leads by pulling or pushing them away. During soldering and unsoldering operations, dissipate excessive heat by holding the component lead with a pair of pliers. This is particularly important when the part concerned is a transistor or crystal diode.

b. It is very important to make well-soldered joints. A carelessly soldered joint may create a new trouble and is one of the most difficult troubles to locate. Be careful not to allow drops of solder to fall into the equipment as they may cause short circuits.

c. When replacing a part in the RF or IF circuit, place it in exactly the same position as the original part. A part having the same electrical value but different physical size may cause trouble in high frequency circuits. In such circuits, use the same type capacitor for replacement and the same length lead because of the self-resonant frequencies of different brands of capacitors. When replacing parts in high frequency circuits, give particular attention to proper grounding; use the same ground as in the original wiring. Failure to observe these precautions when replacing parts in high frequency circuits may result in decreased gain or possibly in unwanted oscillations.

d. In transistorized assemblies, such as the MX-8795/TPX-41 and MD-638/TPX-41, use pencil-type soldering iron TL-606A/U with a 25-watt maximum capacity. If TL-606A/U must be used with alternating current, use isolating transformer FSN 5950-356-1779 between the iron and the line. Do not use a soldering gun; damaging voltages can be induced in circuit components.

e. When soldering transistor leads, use type 60/40 solder FSN 3432-269-9610 quickly; wherever wiring permits, use a heat sink (such as long-nosed pliers) between the soldered joint and 3-42 the transistor. Do not immediately clip the leads of replacement transistors or diodes; connect the new component across the suspected part and observe whether condition returns to normal. If so, clip the leads to the proper length and solder tham permanently in place. For further information on soldering and unsoldering techniques, refer to TB SIG 222.

f. Whenever a part is replaced, make any necessary adjustments and check the performance of the equipment to be sure that the original trouble is remedied and no new trouble has developed in the equipment as a result of the repair.

3-30. Mechanical Parts Repair

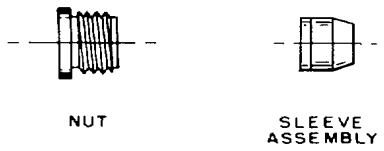
When the specific part requiring repair is removed, close examination will usually determine how repair can be accomplished most effectively. In general, few mechanical parts are economically repairable. Worn or damaged parts usually should be replaced by new parts. In many cases, improper operation of mechanical parts can be corrected by simple readjustments to relieve undue pressure (or to produce more pressure), or to create better alignment between fixed or moving parts. The need for adjustments of this nature may not be apparent until a thorough investigation is made. Always check for possible correcting adjustments before attempting to alter the part mechanically.

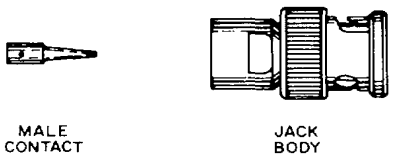
3-31. Coaxial Cable Repair

Follow the detailed instructions in figure 3-4 when fabricating or repairing coaxial cables.

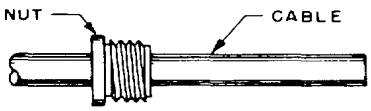
3-32. Multiconductor Cable Repair

Follow the detailed instructions in figure 3-5 when fabricating or repairing Multiconductor cables.



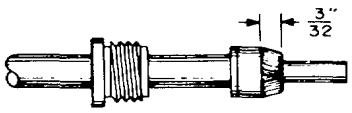


OUTLINE

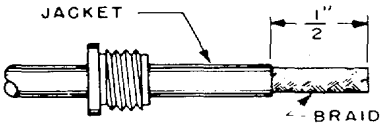


1. CUT OFF SHARP.

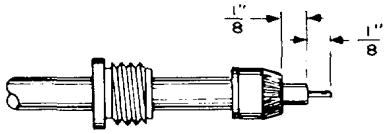
OUTLINE



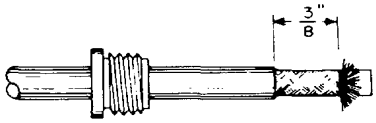
6. WITH SLEEVE IN PLACE, COMB OUT BRAID, FOLD BACK SMOOTH AS SHOWN, AND TRIM TO $\frac{3}{32}$ INCH FROM END.



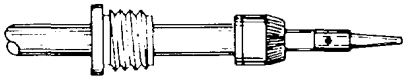
2. CUT OFF JACKET $\frac{1}{2}$ INCH FROM END. BE CAREFUL NOT TO NICK BRAID.



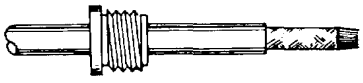
7. CUT INNER DIELECTRIC $\frac{1}{8}$ INCH FROM BRAID. BE CAREFUL NOT TO NICK INNER CONDUCTOR. CUT OFF INNER CONDUCTOR $\frac{1}{8}$ INCH FROM END OF DIELECTRIC.



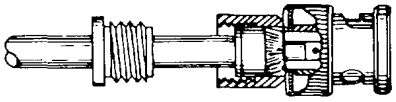
3. CUT OFF INNER INSULATION AND WIRE UNDER BRAID $\frac{3}{8}$ INCH FROM END OF JACKET.



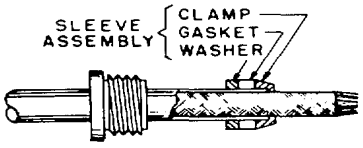
8 TIN INSIDE HOLE OF MALE CONTACT, TIN CENTER CONDUCTOR OF CABLE, SLIP MALE CONTACT IN PLACE AND SOLDER, REMOVE EXCESS SOLDER. BE SURE CABLE DIELECTRIC IS NOT HEATED EXCESSIVELY AND SWOLLEN SO AS TO PREVENT DIELECTRIC ENTERING BODY.



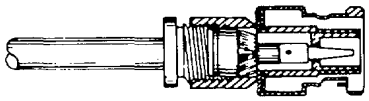
4. TAPER BRAID.



9. PUSH INTO BODY AS FAR AS IT WILL GO, THEN SLIDE NUT INTO BODY AND SCREW INTO PLACE, WITH WRENCH, UNTIL MODERATELY TIGHT. HOLD CABLE AND SHELL RIGIDLY AND ROTATE NUT.



5. SLIDE SLEEVE OVER TAPERED BRAID TO FIT TIGHT AGAINST JACKET. BE SURE INNER SHOULDER OF SLEEVE FITS SQUARELY AGAINST END OF CABLE JACKET.



FINAL ASSEMBLY SHOWN IN CROSS SECTION

EL5895-479-35-TM-23

Figure 3-4. Coaxial cable repair.

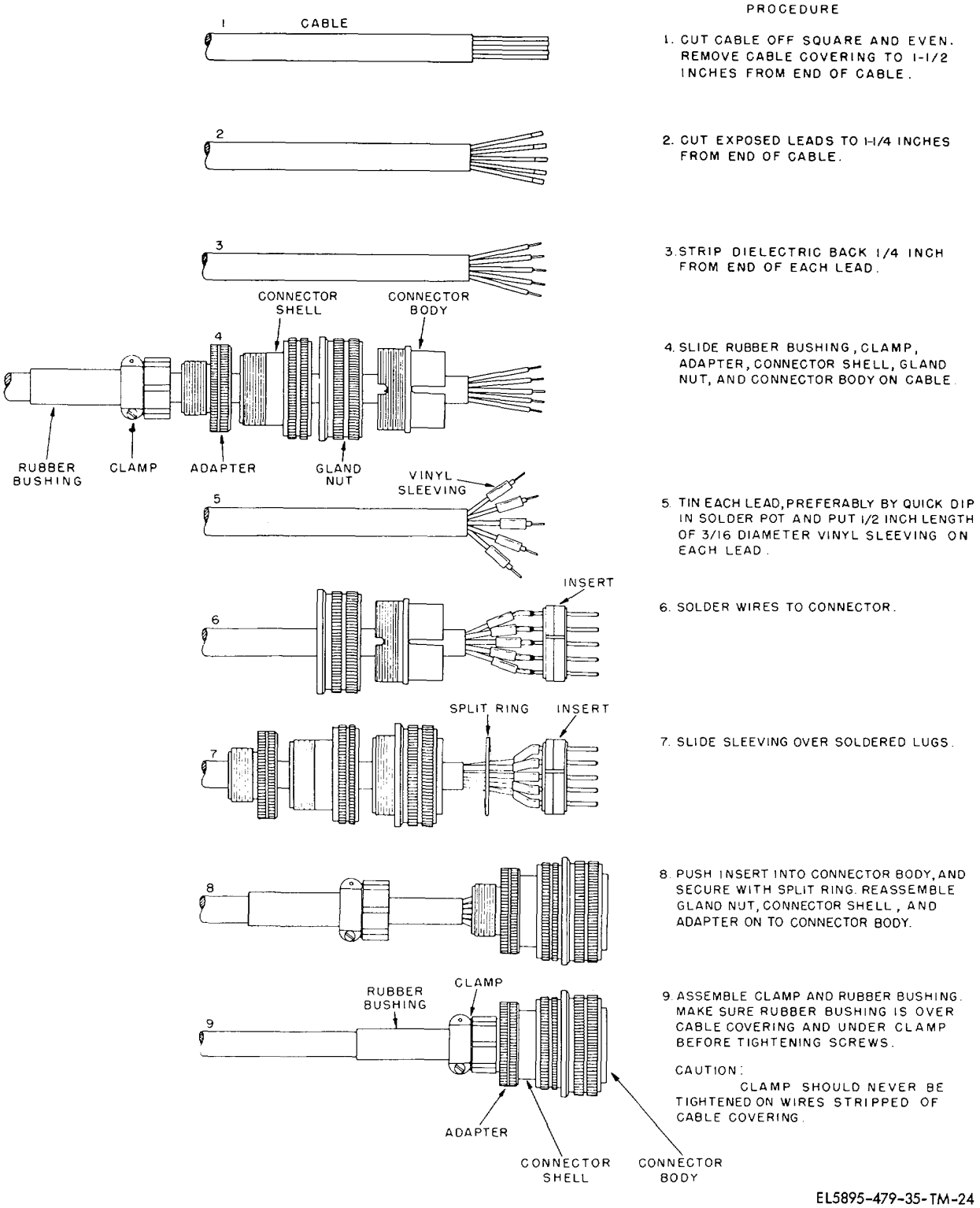


Figure 3-5. Multiconductor cable repair.

Section V. REMOVAL AND REPLACEMENT; DISASSEMBLY AND REASSEMBLY

3-33. General

This section provides detailed instructions for disassembly, reassembly, removal and replacement operations that can be performed Dy the direct support repairman. These instructions consist of step-by-step procedures keyed to accompanying illustrations that portray the units, assemblies, and parts of a major component in an exploded view. Before disassembling a major component, study the applicable exploded view and note the relationships between the various parts and subassemblies. During disassembly, give particular attention to the assemblage of complex mechanical assemblies. This will provide for ease of disassembly and serve as an aid during reassembly. Major components of the AN / TPX-41 are listed in a through I below with references to the paragraphs covering each.

a. Blanker, Interference MX-8795/TPX-41 (para 3-34)
b. Coder-Control KY-97C/TPX (para 3-35)
c. Control, Remote Switching C-1271A/TPX22 (para 3-36)
d. Modulator, Pulse MD-638/TPX-41 (para 3-37)
e. Receiver-Transmitter, Radio RT264D / UPX-6 (para 3-38)
f. Antenna Group AN/GPA-119 (para 3-39)
g. Pedestal, Antenna AB-1158 / GPA-119 (para 3-40)
h. Antenna AS-1796/GPA-119 (para 3-41 and 3-42)
i. Decoder, Video KY-593/TPX-44 (para 343)
j. Control, Remote Switching C-7014/ TPX-44 (para 3-44)
k. Simulator, Radar Signal SM-472/TPX-44 (para 3-45)
l. Interconnecting Box J-2945 / TPX-41 (para 3-46)
3-

3-34. Blanker, Interference MX-8795/TPX41, Disassembly and Assembly (fig. 3-6).

a. Disassembly. To disassemble interference Blanker MX-8795 / TPX-41, proceed as follows:

(1) Remove front panel (1), processor (2), trigger / gate generator (3), and synchronizer-multiplier (4).

NOTE
Refer to steps (25) through (37) for complete disassembly of front panel.

(2) Remove four screws (5), lockwashers (6), and flat washers (7).

(3) Tag and unsolder wires to board assembly (8).

(4) Unsolder and remove capacitors C31101 (9), C31102 (10), C13303 (11), C31104 (12), and C31105 (13).

(5) Unsolder and remove resistors R31103 (14), R31104 (15), R31105 (16), R31106 (17), R31107 (18), R31108 (19), and R31109 (20).

(6) Unsolder and remove semiconductors CR31102 (21), CR31103 (22), CR31104 (23), CR31101 (24), and CR31105 (25).

Key to fig. 3-6:

1 Front panel
2 Processor
3 Trigger / gate generator
4 Synchronizer-multiplier
5 Screw (4)
6 Lockwasher (4)
7 Flat washer (4)
8 Board assembly
9 Capacitor C31101
10 Capacitor C31102
11 Capacitor C31103
12 Capacitor C31104
13 Capacitor C31105
14 Resistor R31103
15 Resistor R31104
16 Resistor R31105
17 Resistor R31106
18 Resistor R31107
19 Resistor R31108
20 Resistor R31109
21 Semiconductor CR31102
22 Semiconductor CR31103
23 Semiconductor CR31104
24 Semiconductor CR31101
25 Semiconductor CR31105
26 Screw (41
27 Screw 12)
28 Flat washer (21
29 Screw (2)
30 Flat washer (2)
31 Bracket
31A Delay line DL31101
31B Screw (2)
31C Flat washer (2)
31D Bracket
32 Screw (12)
33 Lockwasher (121
34 Flat washer (12)
35 Power supply PS31101
35A Power supply PS31102
35B Standoff (121
36 Nut (41
37 Lockwasher (4)
37A Flat washer (4)
37B Filter FL31101
37C Switch S31103
38 Nut 16)
39 Screw (6)
40 Lockwasher (6)
41 Flat washer (6)
42 Connector J31109
43 Connector J31108
44 Connector J31107
45 Nut
46 Lockwasher
47 Terminal (2)
48 Screw
49 Nut (6)
50 Flat washer (6)
51 Screw (61
52 Receptacle (2)
53 Nut (5)
54 Lockwasher (5)
55 Connector J31102
56 Seal 15)
57 Connector J31104
58 Conn3ctor J31105
59 Connector J31106
60 Connector J31103
61 Nut (41
62 Screw 14)
63 Lockwasher (41
64 Flat washer (41
65 Connector J31101
66 Grommet
67 Nut (6i
68 Screw (6)
69 Flat Washer (61
70 Screw (4)
71 Lockwasher 14)
72 Flat washer (4l
73 Handle (2)
74 Nut (2)
75 Lockwasher (2)
76 Key washer (2)
77 Switch S31101
78 Switch S31102
79 Fuse cap
80 Gasket
81 Fuse F31101
82 Nut
83 Lockwasher
84 Fuse holder XF31101
85 Gasket
86 Fuse holder XF31102 (F31102)
87 Lamp cap
88 Lamp DS31101
89 Nut
90 Lockwasher
91 Lampholder XDS31101
92 Lampholder XDS31102 IDS31102)
93 Nut (8)
94 Lockwasher (8)
95 Testpoint TP31101
96 Testpoint TP31102
97 Testpoint TP'31103
98 Testpoint TP31104
99 Testpoint TP31105
100 Testpoint TP31106
101 Testpoint TP31107
102 Testpoint TP31108
103 Locknut (2)
104 Nut (2)
105 Lockwasher (2)
106 Resistor R31101
107 Resistor R31102
108 Ring (4)
109 Stud (4)
110 Nut (4)
111 Flat washer (4)
112 Screw (4)
113 Flat washer (4)
114 Identification plate
115 Nut (6)
116 Screw (6)
117 Lockwasher (6)
118 Flat washer (6)
119 Clamp (6)

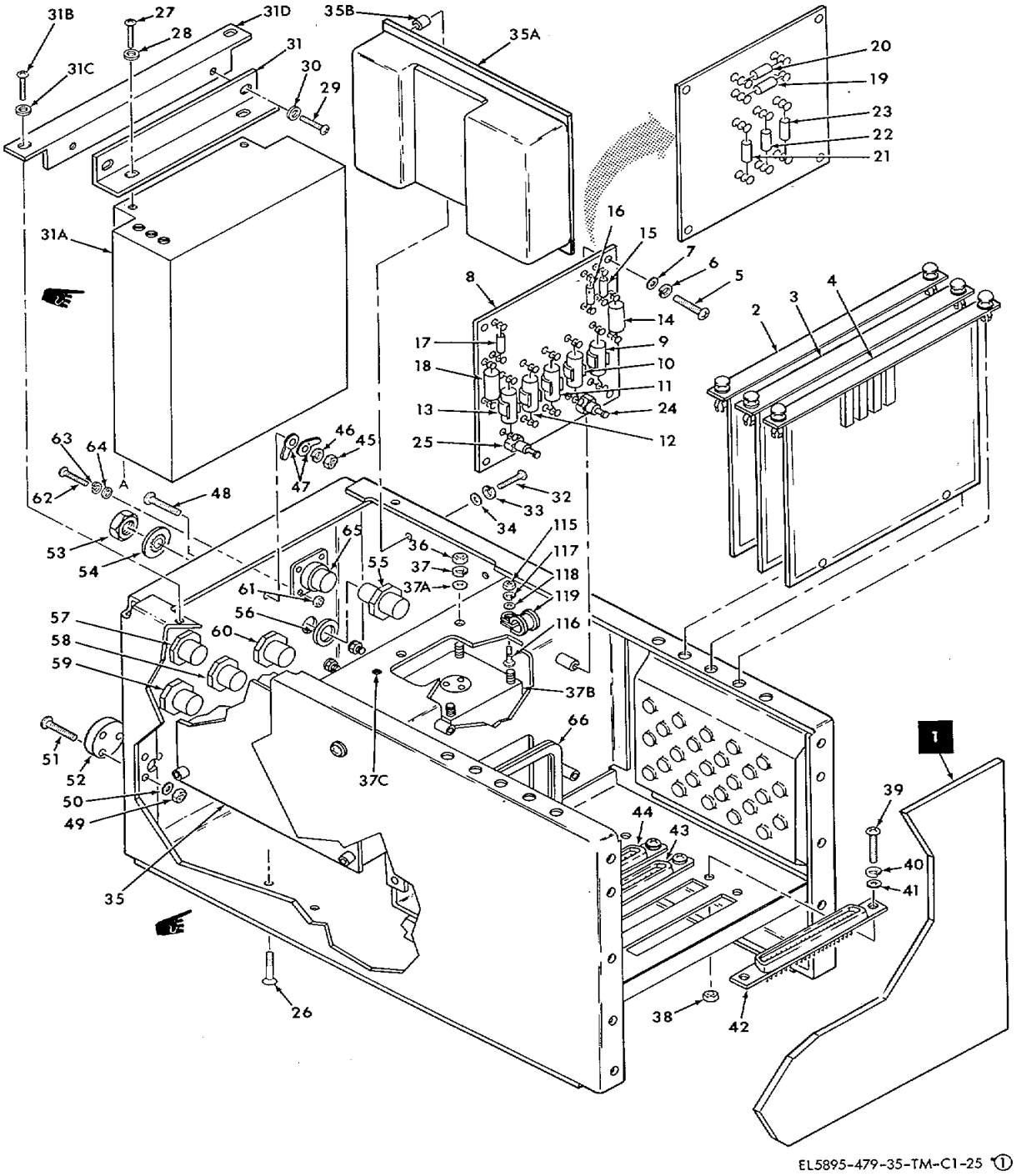


Figure 3-6 (1) . Blanker, Interference MX-8795 / TPX41, disassembly and parts location (sheet 1 of 2).

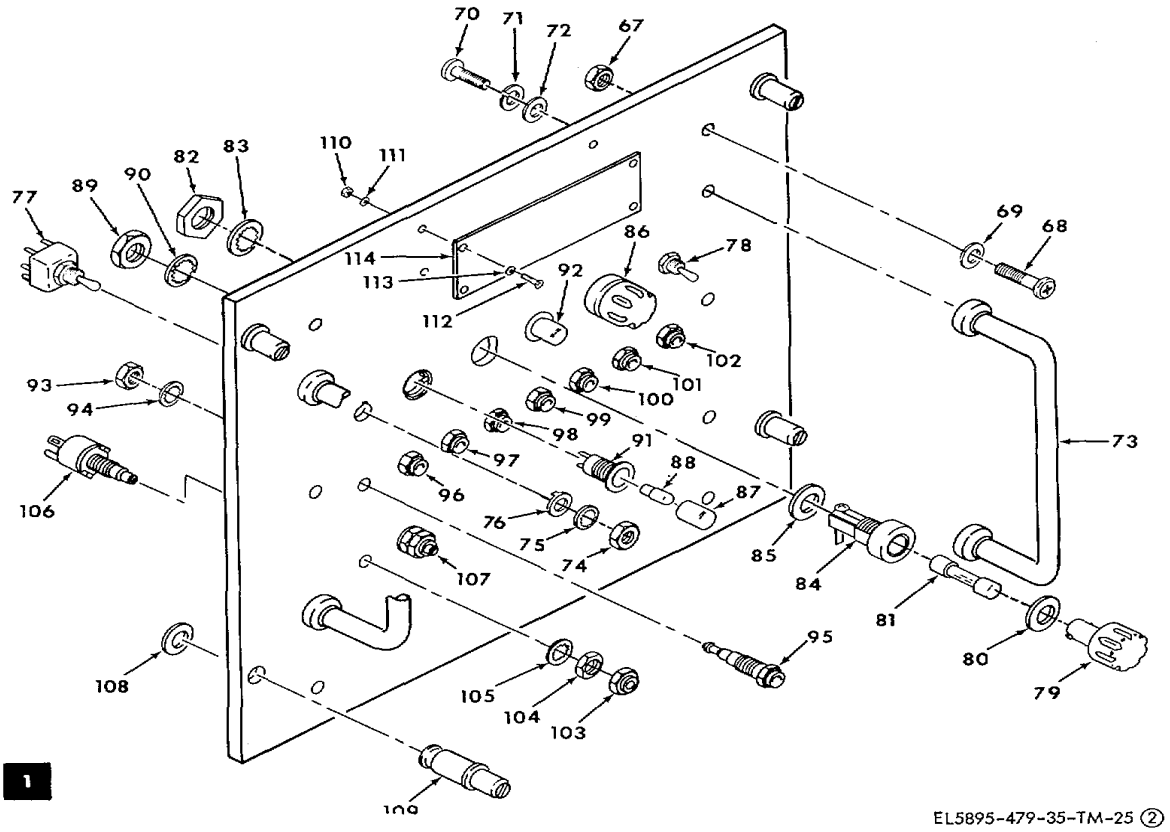


Figure 3-6 (2) Blanker. Interference MX-8795 / TPX-41, disassembly and parts location (sheet 2 of 2).

(7) Remove four screws (26) from underside Df chassis.

(8) Remove two screws (27) and two flat washers (28).

(9) Remove two screws (29), two flat washers (30), and bracket (31).

(10) Lift delay line DL31101 (31A) from chassis, place on flat work surface, and tag and disconnect all wires.

(11) Remove two screws (31B), two flat washers (31C), and bracket (31D).

(12) Remove 12 screws (32), lockwasher (33), and flat washers (34).

(13) Tag and unsolder wires to power supplies PS31101 (35) and PS21102 (35A).

(13.1) Remove power supplies PS31101 (35) and PS31102 (35A) and 12 standoffs (35B).

(13.21 Remove four nuts (36) lockwashers (37), flat washer (37A), and filter FL31101 (37B).

(13.3) Tag and unsolder wires to switch S31103 (37C) and remove switch.

(14) Remove six nuts (38), screws (39), lockwashers (40), and flat washers (41).

(15) Tag and unsolder wires to connectors J31109 (42), J31108 (43), and J31107 (44).

(16) Remove nut (45), lockwasher (46), two terminals (47), and screw (48).

(17) Tag and unsolder wires to two terminals.

(18) Remove six nuts (49), flat washers (50), screws (51), and two receptacles (52).

(19) Remove nut (53), lockwasher (54), connector 'J31102 (55), and seal (56).

(20) Repeat (19) above to remove connectors J31104 (57), J31105 (58), J31106 (59), and J31103 (60).

(21) Tag and unsolder wires to connectors J31102, J31104, J31105, J31106, and J31103.

(22) Remove four nuts (61), screws (62), lockwashers (63), flat washers (64), and connector J31101 (65).

(23) Tag and unsolder wires to connector J31101.

(24) Remove grommet (66).

(25) Remove six nuts (67), screws (68), and flat washers (69).

(26) Remove four screws (70), lockwashers (71), flat washers (72), and two handles (73).

NOTE

Tag and unsolder wires to electrical parts on front panel.

(27) Remove two nuts (74), lockwashers (75), key washers (76), and switches S31101 (77) and S31102 (78).

(28) Remove fuse cap (79), gasket (80), fuse F31101 (81), nut (82), lockwasher (83), fuse holder XF31101 (84), and gasket (85).

(29) Repeat (28) above to disassemble fuse holder XF31102 (86) for fuse F31102.

(30) Remove lamp cap (87), lamp DS31101 (88). nut (89), lockwasher (90), and lampholder XDS31101 (91).

(31) Repeat (30) above to disassemble lampholder XDS31102 (92) for lamp DS31102.

(32) Remove nut (93), lockwasher (94), and testpoint jack TP31101 (95).

(33) Repeat (32) above for testpoint jacks TP31102 (96), TP31103 (97), TP31104 (98), TP31105 (99), TP31106 (100), TP31107 (101), and TP31108 (102).

(34) Remove locknut (103), nut (104), lockwasher (105), and resistor R31101 (106).

(35) Repeat (34) above to remove resistor R31102 (107).

(36) Remove four rings (108) and studs (109).

(37) Remove four nuts (110), flat washers (111), screws (112), flat washers (113), and identification plate (114).

(38) Remove six clamps (119) by removing six screws (116), nuts (115), lockwashers (117), and flat washers (118).

b. Assembly. To assemble Blanker, Interference, MX8795/TPX41, proceed as follows:

(1) Attach identification plate (114) to front panel(1) using four nuts (110), flat washers (111), screws (112), and flat washers (113).

(2) Install four rings (108) and studs (109).

(3) Install resistors R31101 (106) and R31102 (107 using locknuts (103), nuts (104), and lockwashers (105).

(4) Install testpoint jack TP31101 (95) using nut (93) and lockwasher (94).

(5) Repeat step (4) to install testpoint jacks TP31102 (96), TP31103 (97), TP31104 (98), TP31105 (99), TP31106 (100), TP31107 (101), and TP31108 (102).

(6) Install lampholder XDS31101 (91) using lockwasher (90), nut (89), lamp DS31101 (88), and lamp cap (87).

(7) Repeat step (6) to install lamp DS31102 and lampholder XDS31102 (92).

(8) Install fuse holder XF31101 (84) using gasket (85), lockwasher (83), nut (82), fuse F31101 (81, gasket (80), and fuse cap (79).

(9) Repeat step (8) to install fuse F31102 and fuse holder XF31102 (86).

(10) Install switches S31101 (77) and S31102 (78) using two nuts (74), lockwashers (75), and key washers (76).

NOTE

Use Blanker, Interference MX8795 / TPX41 wiring diagram as guide (fig. FO4) and solder wires to electrical parts on front panel and chassis.

(11) Install front panel (1) on chassis using six nuts (67), screws (68), and flat washers (69).

(12) Install two handles (73) on front panel using four screws (70), lockwashers (71), and flat washers (72).

(13) Install grommet (66).

(14) Install connector J31101 (65) using four nuts (61, . screws (62), lockwashers (63), and flat washers (64).

(15) Install connectors J31102 (55), J31104 (57). J31105 (58), J31106 (59), and J31103 (60) using five nuts (53), lockwashers (54), and seals (56).

(16) Install two receptacles (52) using six nuts (49), flat washers (50), and screws (51).

(17) Install two terminals (47) using nut (45), lockwasher (46), and screw (48).

(18) Install connectors J31109 (42), J31108 (43), and J3 1107 (44) using six screws (30), lockwashers (40), flat washers (41), and nuts (38).

(19) Install switch S31103 (37C) and solder leads to appropriate points of connection using figure FO4 as a guide.

(20) Install filter FL31101 (37B) using four flat washers (37A), lockwashers (37), and nuts (36).

(21) Install power supplies PS31101 (35) and PS31102 (35A) and 12 standoffs (35B) using 12 flat washers (34), lockwashers (33), and screws (32). Solder wires to power supplies using figure FO4 as a guide.

(21.1) Install bracket (31D) using two flat washers (31C) and screws (31B).

(21.2) Solder wires to delay line DL31101 (31A), using figure FO4 as a guide, and position delay line in chassis.

(21.3) Install bracket (31) using two flat washers (30), screws (29), flat washers (28), and screws (27).

(21.4) Install four screws (26) from underside of chassis.

(22) Install semiconductors CR31102 (21),

CR31103 i22). CR31104 (23). CR31101 (24)., and CR31105 1251 on board assembly (q).

(23) Install resistors R31103 (14). R31104 115). R31105 (16). R31106 (17). R31107 (181). R31108 119) (20) on board assembly.

(24) Install capacitors C31101 (9). C31102 10). C31103 (11). C31104 i12). and C31105 113) on board assembly.

(25) Install board assembly on chassis using four screws (5). lockwashers (6). and flat washers ().

(26) Install processor (2). trigger/ gate generator (3). and synchronizer-multiplier (4).

(27) Install six clamps (119), . screws (116), flat washers (118). lockwashers (11 7). and nuts (115).

3-35. Coder Control KY97C / TPX, Disassembly and Assembly

For information covering the disassembly and assembly of Coder Control KY97C / TPX, refer to TM 11589520135.

3-36. Control, Remote Switching C, .121A / TPX22, Disassembly and Assembly (fig. 37)

a. Disassembly. To disassemble Control, Remote Switching C127 1A / TPX22, proceed as follow s:

(1) Remove six screws (1 on front panel (2).

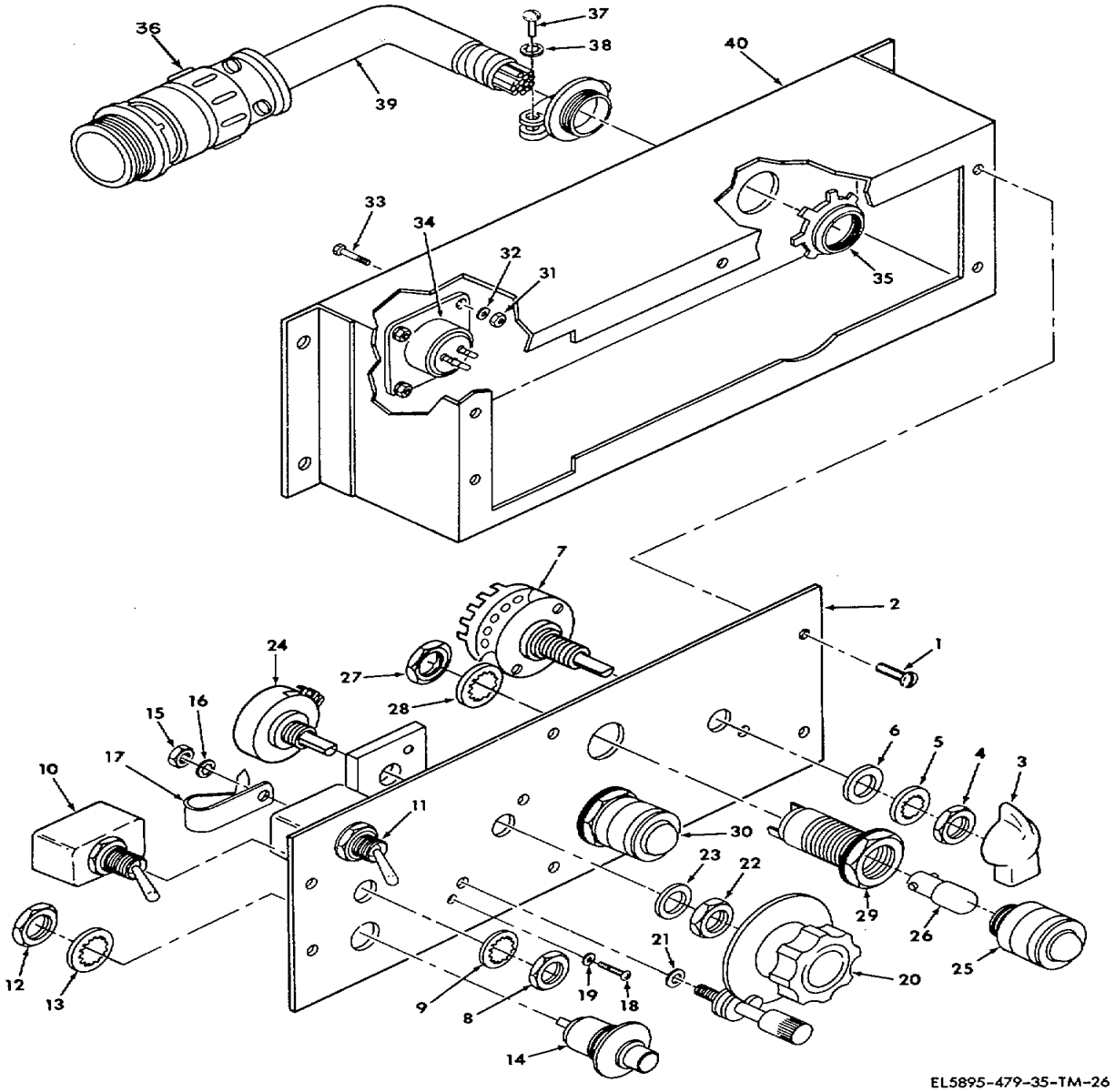
(2) Tag and unsolder wires to switches, lampholders. and resistor on front panel.

(3) Remove knob (3), nut (4), lockwasher (5). flat washer (6). and switch S731 (i).

(4) Remove nut (8)1. lockwasher (9). and switch S732 (10). Use same procedure to remove switch S734 (11).

(5) Remove nut (12). lockwasher (13), and switch S733 (14).

(6) Remove nut (15). lockwasher (16). and clip (17i).



1	Screw (6)	11	Switch S734	21	Flat washer	31	Nut (4)
2	Front panel	12	Nut	22	Nut	32	Washer (4)
3	Knob	13	Lockwasher	23	Flat washer	33	Screw (4)
4	Nut	14	Switch S733	24	Resistor R731	34	Connector J732
5	Lockwasher	15	Nut	25	Cover	35	Ring
6	Flat washer	16	Lockwasher	26	Lamp	36	Connector J731
7	Switch S731	17	Clip	27	Nut	37	Screw (2)
8	Nut	18	Screw	28	Lockwasher	38	Lockwasher (2)
9	Lockwasher	19	Flat washer	29	Lampholder I732	39	Cable assembly
10	Switch S732	20	Knob assembly	30	Lampholder I731	40	Chassis

Figure 3-7. Control, Remote Switching C--1271A/TPX-22, disassembly and parts location.

(7) Remove screw (18), flat washer (19), knob assembly (20), and flat washer (21).

(8) Remove nut (22), flat washer (23), and variable resistor R731 (24).

(9) Remove cover (25), lamp (26), nut (27), lockwasher (28), and lampholder 1732 (29). Use same procedure to remove lampholder 1731 (30).

(10) Remove four nuts (31), washers (32), screws (33), and connector J732 (34).

(11) Tag and unsolder wires on connector J732.

(12) Remove ring (35) and connector J731 (36) from chassis.

(13) Remove two screws (37), lockwashers (38), cable assembly (39) from chassis (40).

b. Assembly. To assembly Control, Remote Switching C-1271A/TPX-22, proceed as follows:

(1) Attach cable assembly (39) to chassis (40) using connector J731 (36) and ring (35).

(2) Install two screws (37) and lockwashers (38) on cable assembly.

(3) Attach connector J732 (34) to chassis using four nuts (31), washers (32), and screws (33).

(4) Attach lampholder I732 (29) to front panel (2) using nut (27) and lockwasher (28).

(5) Install lamp (26) and cover (25) on lampholder I732 (29). Use same procedure to install lampholder 1731 (30).

(6) Install variable resistor R731 (24) using nut (22) and flat washer (23).

(7) Install knob assembly (20) with flat washer (21) and secure with screw (18) and flat washer (19).

(8) Install clip (17) using nut (15) and lockwasher (16).

(9) Install switch S733 (14) using nut (12) and lockwasher (13).

(10) Install switch S732 (10) using nut (8) and lockwasher (9). Use same procedure to install switch S734 (11).

(11) Install switch S731 (7) using nut (4), lockwasher (5), and flat washer (6).

(12) Attach knob (3) to switch S731 (7).

(13) Using Control, Remote Switching C-1271A/TPX-22, wiring diagram as guide (fig.FO-5), solder wires to switches, lampholders, connector, and resistor.

(14) Attach front panel to chassis using six screws (1).

3-37. Modulator, Pulse MD-638/ TPX-41, Disassembly and Assembly (fig. 3-8)

a. Disassembly. To disassemble Modulator, Pulse MD-638/TPX-41, proceed as follows:

(1) Remove pulse generator processor (1).

(2) Remove eight screws (2), lockwashers (3), flat washers (4), and dust cover (5).

(3) Remove four nuts (6), lockwashers (7), flat washers (8) and screws (9).

(4) Tag and unsolder wires to reactor L1201 (14).

(5) Remove four nuts (10), lockwashers (11), flat washers (12), bracket (13), and reactor L1201 (14).

(6) Tag and unsolder wires to transformer T1201.

(7) Remove four nuts (15), lockwashers (16), flat washers (17), and transformer T1201 (18).

(8) Remove six nuts (19), lockwashers (20), flat washers (21), screws (22), and flat washers (23).

(9) Unsolder and remove capacitors C1201 (24), C1203 (25), C1202 (26), C1204 (27), and resistors R1202 (28), and R1204 (29).

(10) Unsolder and remove diodes CR1201 (30), CR1202 (31), CR1203 (32), and CR1204 (33).

(11) Tag and unsolder wires to component board (34).

(12) Remove two nuts (35), lockwashers (36), one terminal (37), two flat washers (38), screws (39), and connector J1203 (40).

(13) Tag and unsolder wires to connector J1203.

(14) Remove connector CP1201 (41) and washer (42).

(15) Remove four nuts (43), lockwashers (44), flat washers (45), screws (46), and two clamps (47).

(16) Remove screw (48), lockwasher (49), flat washer (50), and clamp (51).

(17) Remove nut (52), screw (53), and clamp (54).

(18) Disconnect remaining coax connector at Z1201-2 and remove diplexer Z1201 and cable assembly (55).

NOTE

Refer to (35) through (47) below for complete disassembly of diplexer Z1201 and cable assembly.

(19) Remove two rubber pads (56).

(20) Tag and unsolder wires to connector J1201.

(21) Remove four nuts (57), lockwashers (58), flat washers (59), screws (60), and connector J1201 (61).

(22) Tag and unsolder wires to connectors J1202, J1209, and J1208.

(23) Remove three nuts (62), lockwashers (63), and connectors J1202 (64), J1209 (65), and J1208 (66).

(24) Tag and unsolder wires to resistor R1201.

(25) Remove two nuts (67), lockwashers (68), flat washers (69), screws (70), and resistor R1201 (71).

(26) Tag and unsolder wires to resistor R1203.

(27) Remove two nuts (72), lockwashers (73), flat washers (74), screws (75), and resistor R1203 (76).

(28) Remove nut (77), lockwasher (78), solder lug terminal (79), flat washer (80), and screw (81).

(29) Tag and unsolder wire(s) to terminal.

(30) Remove post (82), flat washer (83), screw (84), lockwasher (85), and flat washer (86).

(31) Tag and unsolder wires to semiconductors CR1205 (87), CR1206 (88), CR1207 (89), CR1208 (90), CR1209 (91), and CR1210 (92).

NOTE

Detailed exploded views of semiconductors and mounting kits are shown in figure 3-8 (2) .

(32) Remove nut (93), lockwasher (94), flat washer (95), solder lug (96), flat washer (97), two mica washers (98 and 99), semiconductor (100), two mica washers (101 and 102), and insert (103). Step is for removal of semiconductors CR1205 and CR1208 from pulse modulator chassis (122).

(33) Remove nut (104), lockwasher (105), flat washer (106), two mica washers (107 and 108), semiconductor (109), two mica washers (110 and 111), flat washer (112), solder lug (113), and insert (114). Step is for removal of semiconductors CR1206 and CR1209 from pulse modulator chassis (122).

(34) Remove nut (115), lockwasher (116), flat washer (117), semiconductor (118), flat washer (119), solder lug (120), and insert (121). Step is for removal of semiconductors CR1207 and CR1210 from pulse modulator chassis (122).

NOTE

The following steps describe detailed disassembly of diplexer Z1201 and cable assembly (fig. 3-82).

(35) Remove connectors P1207 (123), P1206 (124), and cable assembly (125).

(36) Remove four screws (126), lockwashers (127), flat washers (128), and connector (129).

(37) Remove two nuts (130), lockwashers (131), flat washers (132), screws (133), and clamps (134).

(38) Remove connector Z1201-2 (135).

(39) Remove four screws (136), lockwashers (137), flat washers (138), and connector P1205 (139).

(40) Remove low-pass filter (140).

(41) Remove four screws (141), lockwashers (142), flat washers (143), and connector (144).

(42) Remove connector (145).

(43) Remove four screws (146), lockwashers (147), flat washers (148), and connector (149).

(44) Remove high-pass filter (150).

(45) Remove four screws (151), lockwashers (152), flat washers (153), and connector (154).

(46) Remove four screws (155), lockwashers (156), flat washers (157), and diplexer-T cover (158).

(47) Remove diplexer-T (159).

b. Assembly. To assemble pulse modulator MD-638/TPX-41, proceed as follows:

(1) Install diplexer-T cover (158) on diplexer-T (159) using four screws (155), lockwashers (156), and flat washers (157).

(2) Install connector (154) using four screws (151), lockwashers (152), and flat washers (153).

(3) Install connector (145) to diplexer connector (154).

(4) Install connector (149) on high-pass filter (150) using four screws (146), lockwashers (147), and flat washers (148).

(5) Install connector (144) on other end of high-pass filter using four screws (141), lockwashers (142), and flat washers (143).

(6) Connect high-pass filter connector (149) to right-angle connector (145).

(7) Install connector P1205 (139) on lowpass filter (140) using four screws (136), lockwashers (137), and flat washers (138).

(8) Connect low-pass filter to diplexer-T (159) using two clamps (134), nuts (130), lockwashers (131), flat washers (132), and screws (133).

(9) Connect connector Z1201-2 (135) to connector P1205.

(10) Connect connector (129) to diplexer-T (159) using four screws (126), lockwasher (127), and flat washers (128).

(11) Install connectors P1207 (123) and P1206 (124) on cable assembly (125).

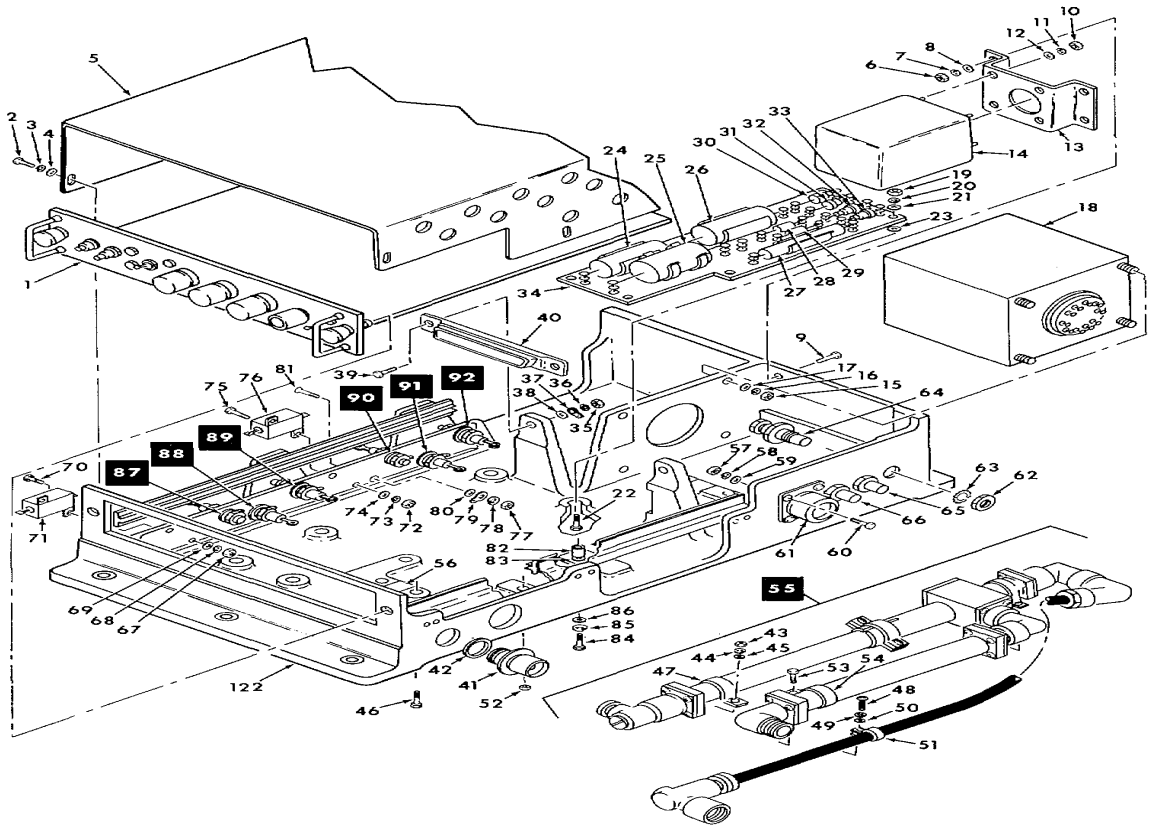
(12) Connect connector P1206 to right-angle connector (129).

(13) Install semiconductors CR1205 (87) and CR1208 (90) on pulse modulator chassis (122) using nut (93), lockwasher (94), flat washer (95), solder lug (96), flat washer (97), two mica washers (98 and 99), semiconductor (100), two mica washers (101 and 102), and insert (103).

NOTE

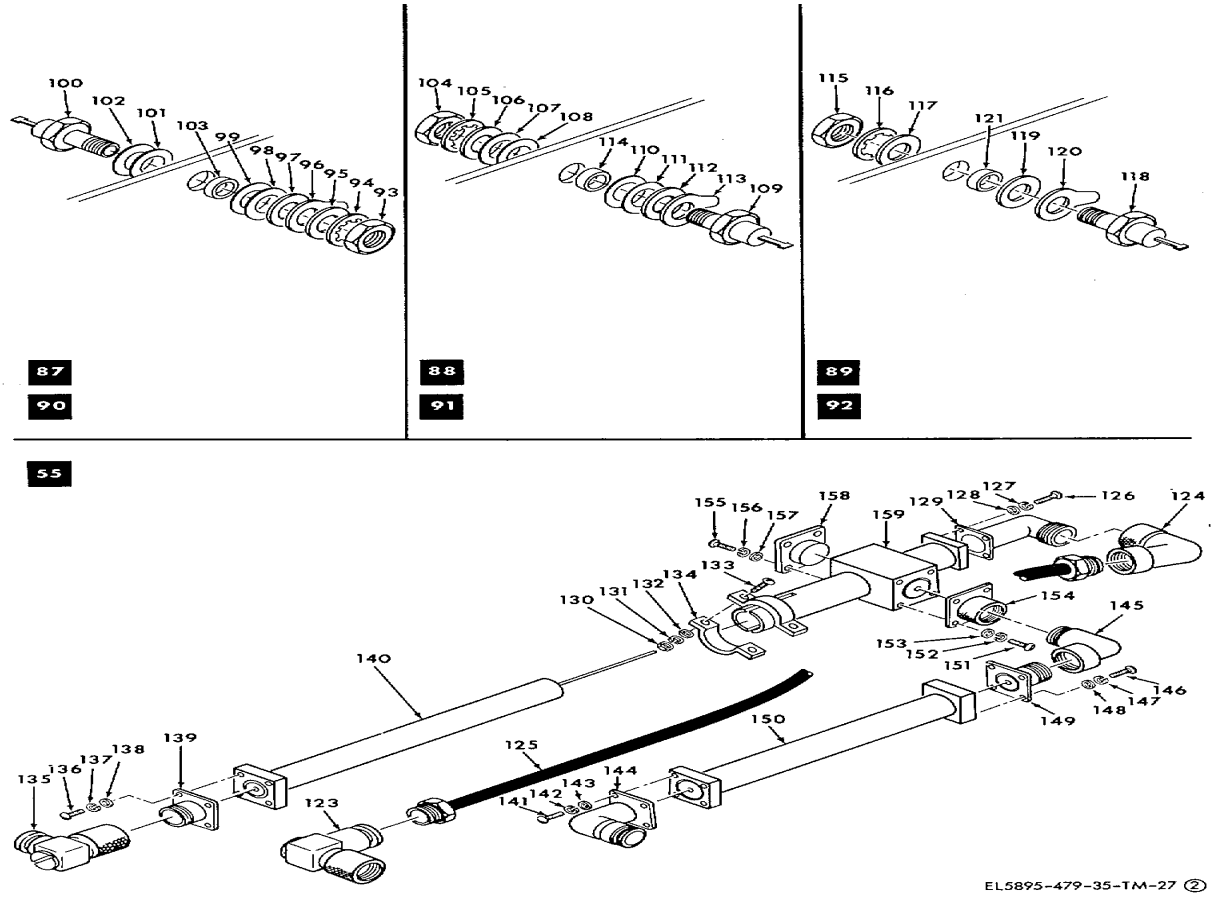
Detailed exploded view of semiconductors and mounting kits are shown in figure 3-82.

(14) Install semiconductors CR1206 (88) and CR1209 (91) on pulse modulator chassis (122) using nut (104), lockwasher (105), flat washer



1	Pulse generator processor	25	Capacitor C1203	49	Lockwasher	72	Nut (2)
2	Screw (8)	26	Capacitor C1202	50	Flat washer	73	Lockwasher (2)
3	Lockwasher (8)	27	Capacitor C1204	51	Clamp	74	Flat washer (2)
4	Flat washer (8)	28	Resistor R1202	52	Nut	75	Screw (2)
5	Dust cover	29	Resistor R1204	53	Screw	76	Resistor R1203
6	Nut (4)	30	Diode CR1201	54	Clamp	77	Nut
7	Lockwasher (4)	31	Diode CR1202	55	Diplexer Z1201 and cable assy	78	Lockwasher
8	Flat washer (4)	32	Diode CR1203			79	Terminal
9	crew (4)	33	Diode CR1204	56	Rubber pad (2)	80	Flat washer
10	Nut (4)	34	Component board	57	Nut (2)	81	Screw
11	Lockwasher (4)	35	Nut (2)	58	Lockwasher (4)	82	Post
12	Flat washer (4)	36	Lockwasher (2)	59	Flat washer (4)	83	Flat washer
13	Bracket	37	Terminal	60	Screw (4)	84	Screw
14	Reactor L1201	38	Flat washer (2)	61	Connector J1201	85	Lockwasher
15	Nut (4)	39	Screw (2)	62	Nut (3)	86	Flat washer
16	Lockwasher (4)	40	Connector J1203	63	Lockwasher (3)	87	Semiconductor CR1205
17	Flat washer (4)	41	Connector CP1201	64	Connector J1202	88	Semiconductor CR1206
18	Transformer T1201	42	Washer	65	Connector J1209	89	Semiconductor CR1207
19	Nuts (6)	43	Nut (4)	66	Connector J1208	90	Semiconductor CR1208
20	Lockwasher (6)	44	Lockwasher (4)	67	Nut (2)	91	Semiconductor CR1209
21	Flat washer (6)	45	Flat washer (4)	68	Lockwasher (2)	92	Semiconductor CR1210
22	Screw (6)	46	Screw (4)	69	Flat washer (2)		
23	Flat washer (6)	47	Clamp (2)	70	Screw (2)		
24	Capacitor C1201	48	Screw	71	Resistor R1201		

Figure 3-8 (1). Modulator, Pulse MD-638/TPX-41, disassembly and parts location (sheet 1 of 2).



93	Nut	110	Mica washer	127	Lockwasher (4)	144	Connector
94	Lockwasher	111	Mica washer	128	Flat washer (4)	145	Connector
95	Flat washer	112	Flat washer	129	Connector	146	Screw (4)
96	Lug	113	Lug	130	Nut(2)	147	Lockwasher (4)
97	Flat washer	114	Insert	131	Lockwasher (2)	148	Flat washer (4)
98	Mica washer	115	Nut	132	Flat washer (2)	149	Connector
99	Mica washer	116	Lockwasher	133	Screw (2)	150	High-pass filter
100	Semiconductor	117	Flat washer	134	Clamp (2)	151	Screw (4)
101	Mica washer	118	Semiconductor	135	Connector Z1201-2	152	Lockwasher (4)
102	Mica washer	119	Flat washer	136	Screw (4)	153	Flat washer (4)
103	Insert	120	Lug	137	Lockwasher (4)	154	Connector
104	Nut	121	Insert	138	Flat washer (4)	155	Screw (4)
105	Lockwasher	122	Pulse modulator chassis	139	Connector P1205	156	Lockwasher (4)
106	Flat washer	123	Connector P1207	140	Low-pass filter	157	Flat washer (4)
107	Mica washer	124	Connector P1206	141	Screw (4)	158	Tee cover
108	Mica washer	125	Cable assembly	142	Lockwasher (4)	159	Diplexer-T
109	Semiconductor	126	Screw (4)	143	Flat washer (4)		

Figure 3-8 (2). Modulator, Pulse MD-638/TPX-41, disassembly and parts location (sheet 2 of 2)

(106), two mica washers (107 and 108), semiconductors (109), two mica washers (110 and 111), flat washer (112), solder lug (113), and insert (114).

(15) Install semiconductors CR1207 (89) and CR1210 (92) on pulse modulator chassis (122) using nut (115), lockwasher (116), flat washer (117), semiconductor (118), flat washer (119), solder lug (120), and insert (121).

(16) Install post (82) using flat washer (83), screw (84), lockwasher (85), and flat washer (86).

(17) Install solder lug terminal (79) using nut (77), lockwasher (78), flat washer (80), and screw (81).

(18) Install resistor R1203 (76) using two nuts (72), lockwashers (73), flat washers (74), and screws (75).

(19) Install resistor R1201 (71) using two nuts (67), lockwashers (68), flat washers (69), and screws (70).

(20) Install connectors J1202 (64), J1209 (65), and J1208 (66) using three nuts (62) and lockwashers (63).

(21) Install connector J1201 (61) using four nuts (57), lockwashers (58), flat washers (59), and screws (60).

(22) Install two rubber pads (56) on pulse modulator chassis (122).

(23) Install diplexer Z1201 and cable assembly (55) on pulse modulator chassis using nut (52), screw (53), and clamp (54).

(24) Install clamp (51) on diplexer cable assembly using screw (48), lockwasher (49), and flat washer (50).

(25) Install two clamps (47) using four nuts (43), lockwashers (44), flat washers (45), and screws (46).

(26) Install connector CP1201 (41) using washer (42). Connector CP1201 mates with connector P1207.

(27) Using Modulator, Pulse MD-638/TPX41, wiring diagram as guide (fig. FO-6), solder wires to connector J1203.

(28) Install connector J1203 (40) using two nuts (35), lockwashers (36), flat washers (38), screws (39), and solder lug terminal (37).

NOTE

Assemble component board using Modulator, Pulse MD-638/TPX-41, wiring diagram as guide (fig. FO-6) for soldering wires to component board. Use figure 3-8 as guide for placement of parts.

(29) Attach and solder diodes CR1201 (30), CR1202 (31), CR1203 (32), and CR1204 (33) to component board (34).

(30) Attach and solder capacitors C1201 (24), C1203 (25), C1202 (26), C1204 (27), resistors R1202 (28), and R1204 (29) to component board.

(31) Install component board on pulse modulator chassis using six nuts (19), lockwashers (20), flat washers (21), screws (22), and flat washers (23).

(32) Connect and solder wires to component board.

(33) Using Modulator, Pulse MD-638/TPX41, wiring diagram as guide (fig. FO-6), solder wires to two resistors, six semi-conductors, and terminal mounted on left-hand side of pulse modulator chasses.

(34) Connect and solder wires to connectors J1201, J1202, J1209, J1208, and P1207.

(35) Install transformer T1201 (18) using four nuts (15), lockwashers (16), and flat washers (17).

(36) Connect and solder wires to transformer T1201 using Modulator, Pulse MD-638/TPX-41, wiring diagram as guide (fig. FO-6).

(37) Attach bracket (13) to reactor L1201 (14) using four nuts (10), lockwashers (11), and flat washers (12).

(38) Connect and solder wires to reactor L1201 using schematic of pulse modulator as guide (fig. FO-12).

(39) Install reactor L1201 (14) and bracket (13) using four nuts (6), lockwashers (7), flat washers (8), and screws (9).

(40) Install dust cover (5) using eight screws (2), lockwashers (3), and flat washers (4).

(41) Install pulse modulator processor (1).

3-38. Receiver-Transmitter, Radio RT-264D/ UPX-6, Disassembly and Assembly

For information covering the disassembly and assembly of Receiver-Transmitter, Radio RT-264D/UPX, refer to TM 11-5895-245-35.

3-39. Antenna Group AN/GPA-119, Disassembly and Assembly (fig. 3-9) a. Disassembly.

To disassemble Antenna Group AN/GPA-119, proceed as follows:

(1) Disconnect connector P21002 (1) from connector J21002.

(2) Disconnect connector P21001 (2) from adapter CP21001 and remove cable assembly W21001 (3).

(3) Remove four screws (4), lockwashers (5), flat washers (6), and two guide pins (7).

(4) Remove adapter CP21001 (8) from pedestal rotary joint.

(5) Remove antenna (9).

(6) Remove four screws (10), lockwashers (11), and flat washers (12).

(7) Remove adapter (13) from pedestal (14).

(8) Remove screw and nut (15), cover (16), and clamps (17) on cable assembly W21001. Use same procedure to remove dust cap (18).

b. Assembly. To assemble antenna group AN/ GPA-119, proceed as follows:

(1) Attach clamp (17), cover (16), screw and nut (15) to cable assembly W21001 (3). Install dust cap (18) using same procedure.

(2) Install adapter (13) on pedestal (14) using four screws (10), lockwashers (11), and flat washers (12).

(3) Install adapter CP21001 (8) on pedestal rotary joint.

(4) Install antenna (9) on adapter (12) using four screws (4), lockwashers (5), flat washers (6), and two guide pins (7).

(5) Install cable assembly W21001 (3) connecting connector P21001 (2) to adapter CP21001 and connector P21002 (1) to connector J21002.

3-40. Pedestal, Antenna AB-1158/GPA, Removal and Replacement of Synchro and Drive Motor (fig. 3-10)

a. Removal. To remove synchro and drive motor, proceed as follows: (1) Remove four screws (1), lockwashers (2), and flat washers (3).

(2) Remove synchro cover (4), gasket (5), and four pieces of packing (6).

(3) Release four clamps (7).

(4) Tag and disconnect five terminals (8).

(5) Remove clamp (9) and gear (10) from synchro B2001 (11).

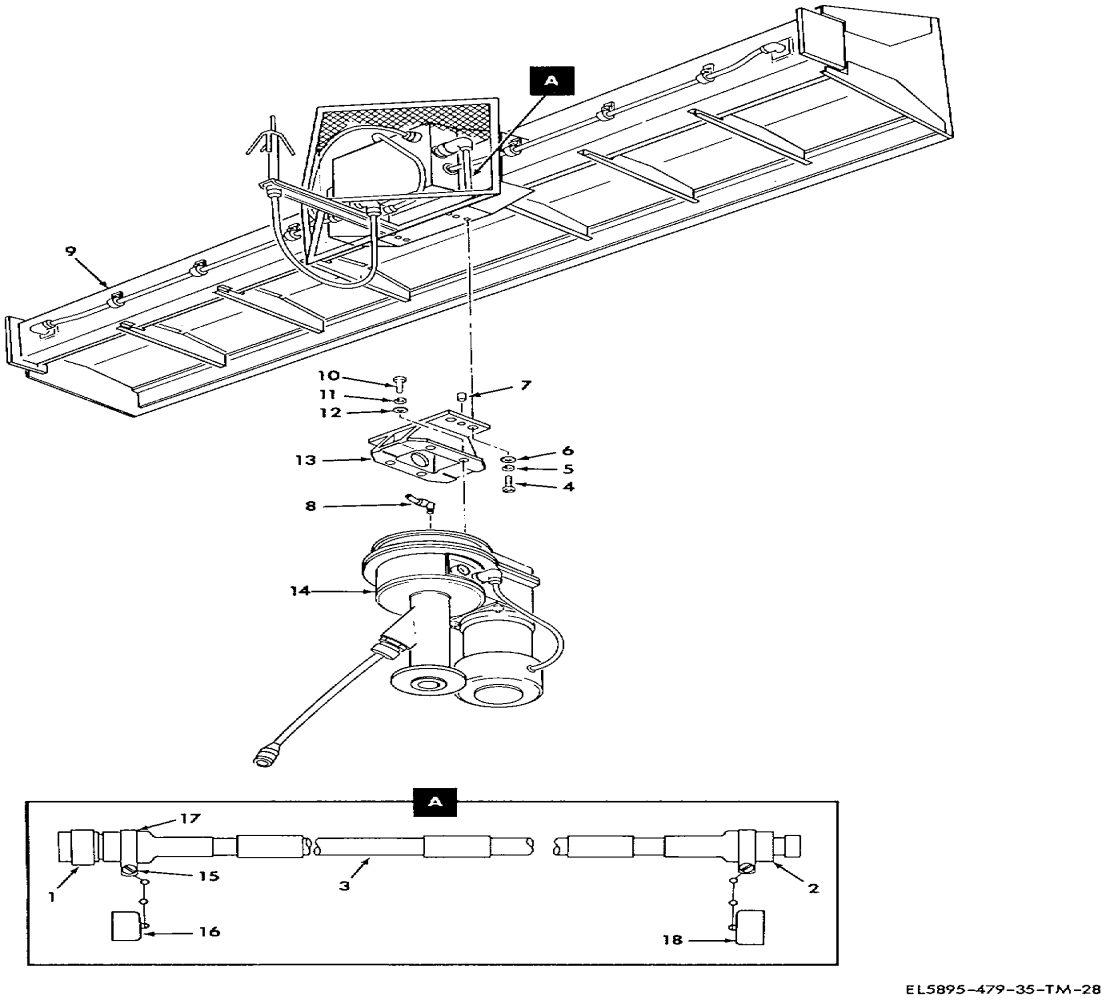
(6) Disconnect connector P20001 (12) from J20001.

(7) Remove four screws (13), lockwashers (14), and flat washers (15).

(8) Remove six screws (16) and washers (17).

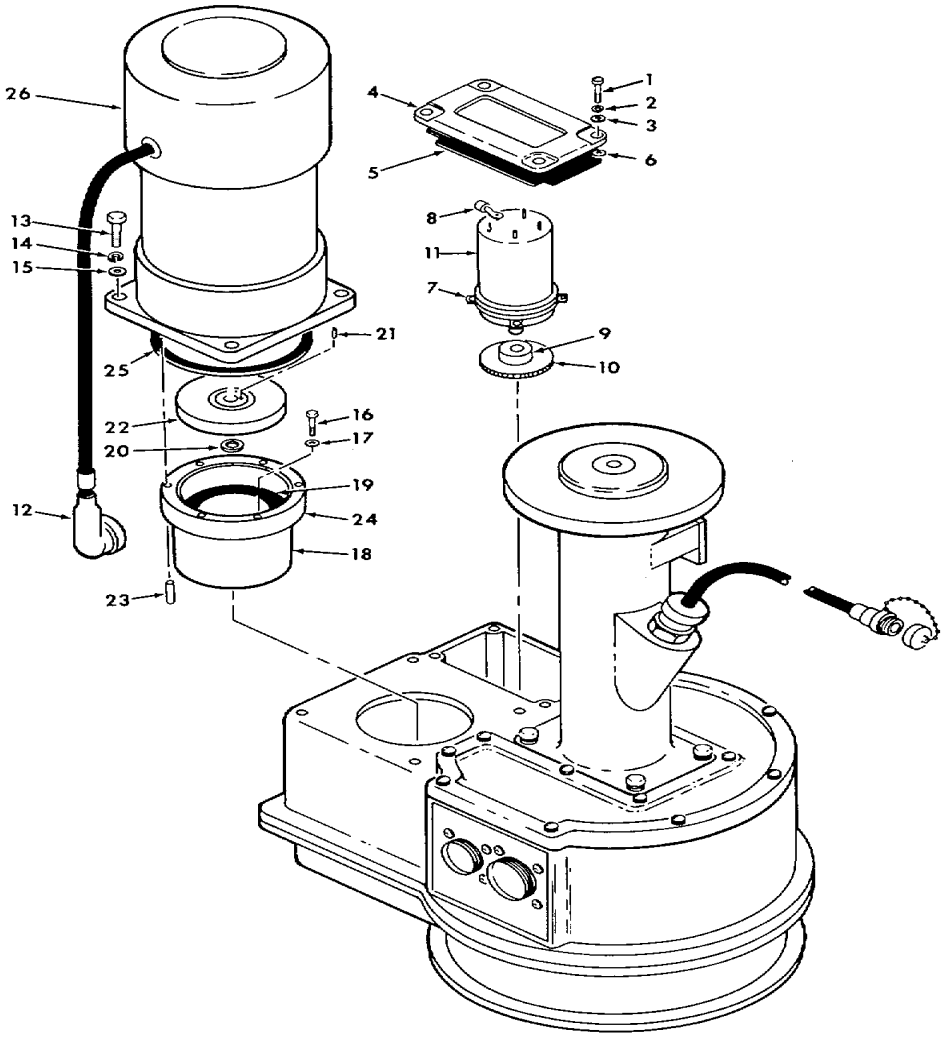
(9) Remove harmonic drive flexspline (18) and grease cartridge (19).

(10) Remove retainer ring (20), key (21), and harmonic drive wave generator (22).



1	Connector P21002	10	Screw (4)
2	Connector P21001	11	Lockwasher (4)
3	Cable assembly W21001	12	Flat washer (4)
4	Screw (4)	13	Adapter
5	Lockwasher (4)	14	Pedestal
6	Flat washer (4)	15	Screw and nut (2)
7	Pin (2)	16	Cover
8	Adapter CP21001	17	Clamp (2)
9	Antenna	18	Dust cap

Figure 3-9. Antenna Group AN/GPA-119, disassembly and parts location.



EL5895-479-35-TM-29

1	Screw (4)	14	Lockwasher (4)
2	Lockwasher (4)	15	Flat washer (4)
3	Flat washer (4)	16	Screw (6)
4	Synchro cover	17	Washer (6)
5	Gasket	18	Flexspline
6	Packing (4)	19	Grease cartridge
7	Clamp (4)	20	Ring
8	Terminal (S)	21	Key
9	Clamp	22	Wave generator
10	Gear	23	Pin
11	Synchro B20001	24	Circular spline
12	Connector P20001	25	Packing
13	Screw (4)	26	Drive motor B20002

Figure 3-10. Pedestal, Antenna AB-1158/GPA-119, removal and replacement of synchro and drive motor.

(11) Remove six pins (23) and harmonic drive circular spline (24).

(12) Remove packing (25) from drive motor B20002 (26).

b. Replacement. Replace synchro and drive motor as follows:

(1) Install packing (25) on drive motor B20002 (26).

(2) Position harmonic drive circular spline (24) on drive motor B20002 and secure with six pins (23).

(3) Position harmonic drive wave generator (22) on drive motor shaft and secure in place with key (21) and retainer ring (20).

(4) Position grease cartridge (19) inside harmonic drive flexspline (18) and secure to pinion shaft in drive housing using six screws (16), and washers (17). Torque six screws (16) to 180 +10 pound-inches.

(5) Attach drive motor B20002 to drive housing using four screws (13), lockwashers (14), and flat washers (15).

(6) Connect connector P20001 (12) to connector J20001 on drive housing.

(7) Position clamp (9) and gear (10) on synchro B20001 (11) shaft. Secure in place using clamp.

(8) Using Pedestal, Antenna AB-1158/ GPA-119, wiring diagram as guide (fig. FO-7), connect five terminals (8) to synchro B20001.

(9) Position synchro B20001 in drive housing and secure using four clamps (7).

(10) Position four pieces of packing (6) between gasket (5) and synchro cover (4).

(11) Secure synchro cover (4) and gasket (5) to drive housing using four screws (1), lockwashers (2), and flat washers (3).

3-41. Antenna AS-1796/GPA-119, Disassembly and Assembly (fig. 3-11)

a. Disassembly. To disassemble Antenna AS1796/GPA-119, proceed as follows:

(1) Disconnect connector P1009 (1) and connector P1010 (2) and remove cable assembly W1003 (3).

(2) Remove four nuts (4), lockwashers (5), flat washers (6), flat washers (7), screws (8), and dipole antenna E1002 (9).

(3) On base of dipole antenna E1002, remove four screws (10), lockwashers (11), flat washers (12), and connector E1002-IN (13).

(4) Disconnect connector P1011 (14) of cable assembly W1006 (15).

(5) Disconnect connector P1007 (16) of cable assembly W1005 (17).

(6) Remove four screws (18), lockwashers (19), flat washers (20), and backfill reflector (21).

(7) Disconnect connectors P1003 (22) and P1001 (23).

(8) Remove six screws (24), lockwashers (25), flat washers (26), and clamps (27) to detach cable assemblies W1001-1 (28) and W1001-2 (29) from IFF antenna.

(9) Remove 18 nuts (30), lockwashers (31), flat washers (32) and screws (33).

(10) Remove antenna mount (34) from IFF antenna E1001 (35).

(11) Disconnect connector P1013 (36) and remove cable assembly W1006.

(12) Remove 12 screws (37), lockwashers (38), and flat washers (39) on RF switch assembly (40).

(13) Remove RF switch assembly by disconnecting connector P1005 (41) of cable assembly W1004 (42).

NOTE

For complete disassembly and assembly of RF switch chassis, refer to paragraph 3-42.

(14) Disconnect connectors P1002 (43), P1006 (44), and P1004 (45).

(15) Remove four screws (46), lockwashers (47), flat washers (48), and hybrid-T HY1001 (49).

(16) Remove four nuts (50), flat washers (51), screws (52), lockwashers (53), and flat washers (54).

(17) Remove split cover (55), grommet (56), split cover (57), and gasket (58). Pull connector P1004 end of cable assembly W1001-2 through cable entry opening.

NOTE

Repeat (16) and (17) above to remove cable assemblies W1001-1 and W1005.

(18) Remove four nuts (59), lockwashers (60), flat washers (61), screws (62), and coupler DC1001 (63).

(19) Remove four screws (64), lockwashers (65), and flat washers (66), on connector E1001-A (67). Repeat step to disassembly connector E10001-B at other end of IFF antenna.

(20) Remove seven screws (68), lockwashers (69), flat washers (70), and end plate (71). Repeat step to remove plate at opposite end of IFF antenna.

(21) Unsolder waveguide probe (72) at connector E1001-A.

(22) Remove connector E1001-A from IFF antenna E1001 (35).

NOTE

Repeat (21) and (22) above to remove connector E1001-B at other end of IFF antenna.

(23) Remove two waveguide probes using suitable potting compound solvent and soldering tool.

b. Assembly. To assemble Antenna AS1796/GPA-119, proceed as follows:

(1) Install two waveguide probes (72) in IFF antenna E1001. Use solder per MIL-S-6872. Coat plating boundaries 1/4 inch wide on waveguide probes and IFF antenna with sealant per MIL-S-8516.

(2) Install connector E1001-A (67) using four screws (64), lockwashers (65), and flat washers (66). Seal exterior edges, cavities, and hardware with sealing compound per MILS-8802.

(3) Solder waveguide probe to connector E1001-A (67), and apply sealant.

NOTE

Repeat (2) and (3) above to install connector E1001-B at other end of IFF antenna.

(4) Attach end plate (71) to IFF antenna using seven screws (68), lockwashers (69), and flat washers (70). Repeat procedure at opposite end of antenna.

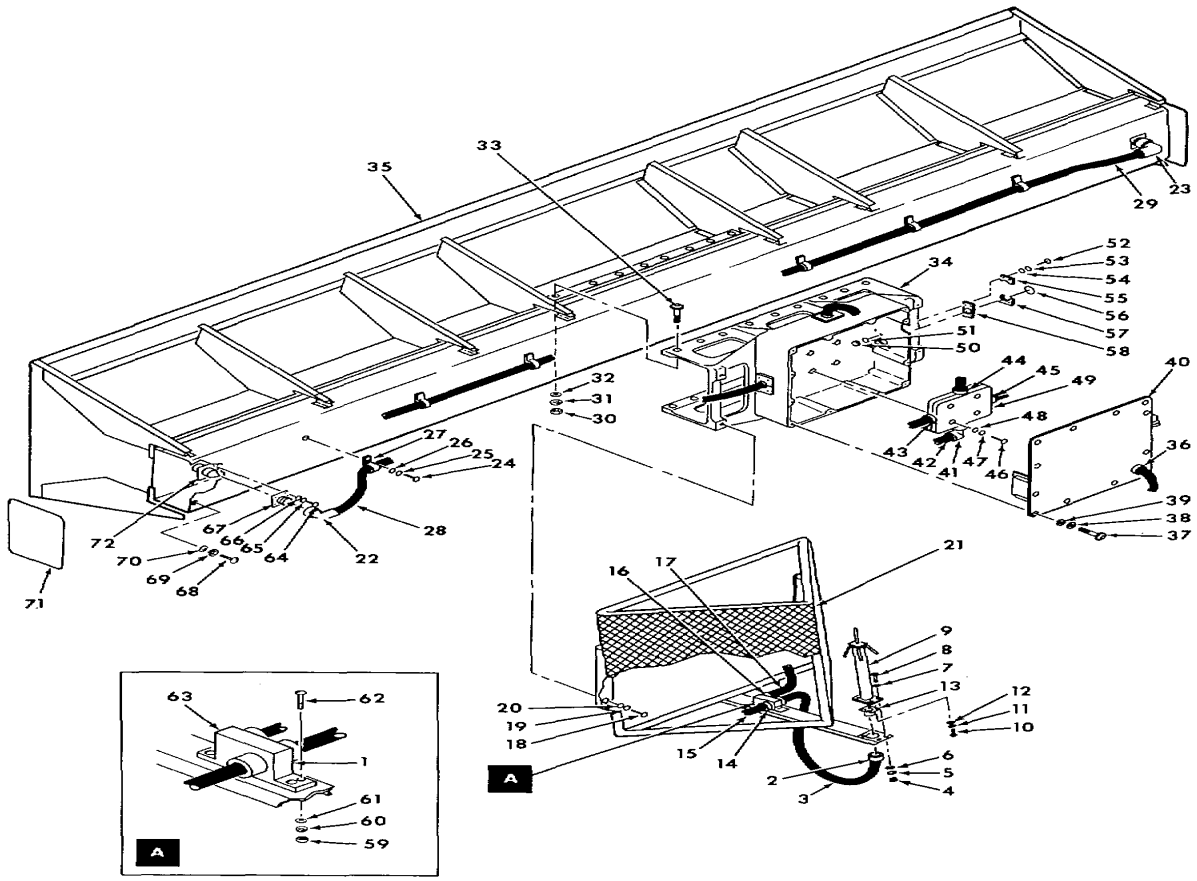
(5) Install coupler DC1001 (63) on backfill reflector (21) using four nuts (59), lockwashers (60), flat washers (61), and screws (62).

(6) Place a gasket (58) on each cable entry opening and pull connectors P1002 (43), P1006 (44), and P1004 (45) through openings.

NOTE

Determine length of cable required within antenna mount (34) by temporarily mounting hybrid-T HY1001 (49) and connecting P1002 to arm 3, P1006 to arm 4, and P1004 to arm 2. Disconnect connectors and remove hybrid-T HY1001 (49).

(7) Secure cable assemblies W1001-1 (28), W1001-2 (29), and W1005 (17) to antenna mount (34) using split cover (57), grommet (56), split cover (55), four flat washers (54), lockwashers (53), screws (52), flat washers (51), and nuts (50).



1	Connector P1009	25	Lockwasher (6)	49	Hybrid-T HY1001
2	Connector P1010	26	Flat washer (6)	50	Nut (4)
3	Cable assembly W1003	27	Clamp (6)	51	Flat washer (4)
4	Nut (4)	28	Cable assembly W1001-1	52	Screw (4)
5	Lockwasher (4)	29	Cable assembly W1001-2	53	Lockwasher (4)
6	Flat washer (4)	30	Nut (18)	54	Flat washer (4)
7	Flat washer (4)	31	Lockwasher (18)	55	Split cover (3)
8	Screw (4)	32	Flat washer (18)	56	Grommet (3)
9	Dipole antenna E1002	33	Screw (18)	57	Split cover (3)
10	Screw (4)	34	Antenna mount	58	Gasket (3)
11	Lockwasher (4)	35	IFF antenna E1001	59	Nut (4)
12	Flat washer (4)	36	Connector P1013	60	Lockwasher (4)
13	Connector E1002-IN	37	Screw (12)	61	Flat washer (4)
14	Connector P1011	38	Lockwasher (12)	62	Screw (4)
15	Cable assembly W1006	39	Flat washer (12)	63	Coupler DC1001
16	Connector P1007	40	RF switch assembly	64	Screw (4)
17	Cable assembly W1005	41	Connector P1005	65	Lockwasher (4)
18	Screw (4)	42	Cable assembly W1004	66	Flat washer (4)
19	Lockwasher	43	Connector P1002	67	Connector E1001-A
20	Flat washer (4)	44	Connector P1006	68	Screw (7)
21	Reflector	45	Connector P1004	69	Lockwasher (7)
22	Connector P1003	46	Screw (4)	70	Flat washer (7)
23	Connector P1001	47	Lockwasher (4)	71	End plate (2)
24	Screw (6)	48	Flat washer (4)	72	Waveguide probe (2)

Figure 3-11. Antenna AS--1796/GPA-119, disassembly and parts location.

(8) Connect following connectors to hybridTHY1001 (49): P1002 (43) of cable assembly W1001-1 (28) to arm 3.

P1006 (44) of cable assembly W1005 (17) to arm 4.

P1004 (45) of cable assembly W1001-2 (29) to arm 2.

P1005 (41) of cable assembly W1004 (42) to arm 1.

(9) Mount hybrid-T HY1001 on antenna mount using four screws (46), lockwashers (47), and flat washers (48).

(10) Mount RF switch assembly (40) on antenna mount using 12 screws (37), lockwashers (38), and flat washers (39).

(11) Attach antenna mount (34) to IFF antenna E1001 (35) using 18 screws (33), flat washers (32), lockwashers (31), and nuts (30).

(12) Attach cable assemblies W1001-1 (28) and W1001-2 (29) to IFF antenna E1001 using six clamps (27), screws (24), lockwashers (25), and flat washers (26).

(13) Connect connector P1003 (22) to connector E1001-A.

(14) Connect connector P1001 (23) to connector E1001-B at other end of IFF antenna E1001.

(15) Attach backfill reflector (21) to antenna mount using four screws (18), lockwashers (19), and flat washers (20).

(16) Solder center conductor of dipole antenna E1002 (9) to connector E1002-IN per MIL-S-6872 using SN60 solder.

(17) Secure connector E1002-IN (13) to base of dipole antenna E1002 using epoxy adhesive bonding, four screws (10), lockwashers (11), and flat washers (12).

(18) Mount dipole antenna E1002 (9) on backfill reflector bracket using four screws (8), flat TM 11-5895-479-35 washers (7), nuts (4), lockwashers (5), and flat washers (6).

(19) Install cable assembly W1003 (3) connecting connector P1009 (1) to connector 1C of coupler DC1001 and connector P1010 (2) to connector E1002-IN (13).

(20) Install cable assembly W1006 (15) connecting connector P1011 (14) to connector 1A of coupler DC1001 and connector P1013 (36) to RF switch assembly (40).

(21) Connect connector P1007 (16) to connector 1D of coupler DC1001.

3-42. Antenna AS-1796/GPA-119, Switch Assembly, Disassembly and Assembly (fig. 3-12)

a. Disassembly. To disassemble the RF switch assembly, proceed as follows:

NOTE

Refer to paragraph 3-41a(12) and (13) for removal of RF switch chassis from antenna AS-1796/GPA-119.

(1) Remove two screws (1), lockwashers (2), and flat washers (3).

(2) Remove four nuts (4), lockwashers (5), flat washers (6), screws (7), and two posts (8).

NOTE

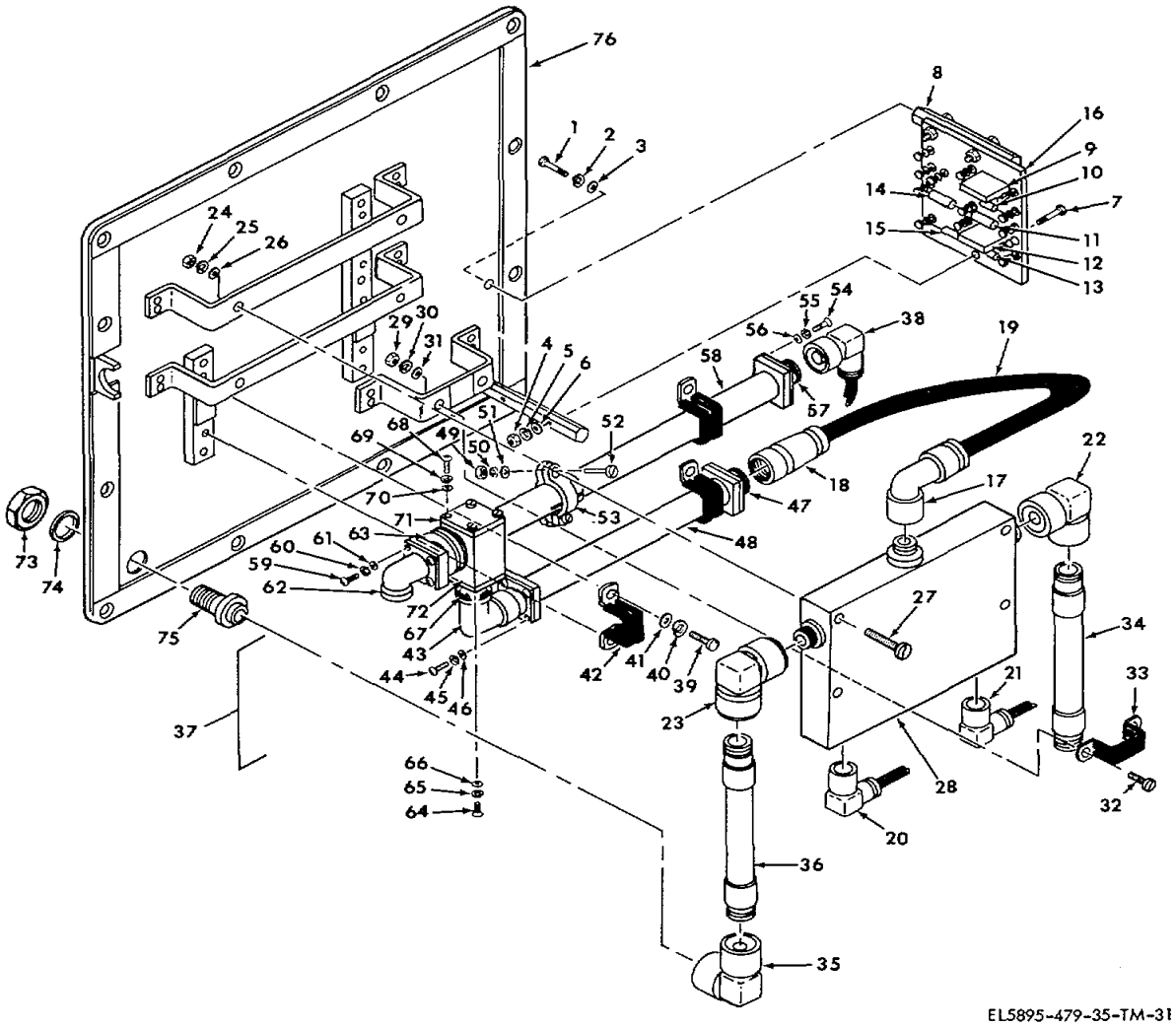
Tag and unsolder wires to component board.

(3) Unsolder and remove capacitor C1102 (9), resistor R1103 (10), resistor Rl101 (11), capacitor Cl101 (12), resistor R1104 (13), resistor R1102 (14), and capacitor C1103 (15) on component board (16).

(4) Disconnect connectors P1105 (17) and P1102 (18) to remove cable assembly Wl101 (19).

(5) Disconnect connectors P1104 (20) and P1103 (21).

(6) Disconnect adapters CPl101 (22) and CP1102 (23).



1	Screw (2)	20	Connector P1104	39	Screw (6)	58	Low-pass filter
2	Lockwasher (2)	21	Connector P1103	40	Lockwasher (6)	59	Screw (4)
3	Flat washer (2)	22	Adapter CP1101	41	Flat washer (6)	60	Lockwasher (4)
4	Nut (4)	23	Adapter CP1102	42	Clamp (3)	61	Flat washer (4)
5	Lockwasher (4)	24	Nut (4)	43	Connector	62	Connector
6	Flat washer (4)	25	Lockwasher (4)	44	Screw (8)	63	Grommet
7	Screw (4)	26	Flat washer (4)	45	Lockwasher (8)	64	Screw (4)
8	Post (2)	27	Screw (4)	46	Flat washer (8)	65	Lockwasher (4)
9	Capacitor C1102	28	RF switch S1101	47	Connector (2)	66	Flat washer (4)
10	Resistor R1103	29	Nut (2)	48	High-pass filter	67	Connector
11	Resistor Rl101	30	Lockwasher (2)	49	Nut (2)	68	Screw (4)
12	Capacitor Cl101	31	Flat washer (2)	50	Lockwasher (2)	69	Lockwasher (4)
13	Resistor R1104	32	Screw (2)	51	Flat washer (2)	70	Flat washer (4)
14	Resistor R1102	33	Clamp	52	Screw (2)	71	Cover
15	Capacitor C1103	34	RF filter FL1101	53	Clamp (2)	72	Diplexer-T
16	Component board	35	Adapter CP1103	54	Screw (4)	73	Nut
17	Connector P1105	36	RF filter FL1102	55	Lockwasher (4)	74	Flat washer
18	Connector P1102	37	Diplexer assembly	56	Flat washer (4)	75	Adapter CP1104
19	Cable assembly Wl101	38	Connector P1101	57	Connector	76	RF switch chassis

Figure 3-12. Antenna AS-1 796/GPA-119, RF switch assembly, disassembly and parts location.

(7) Remove four nuts (24), lockwashers (25), flat washers (26), screws (27), and RF switch S1101 (28**).**

(8) Remove two nuts (29), lockwashers (30), flat washers (31), screws (32), clamp (33), and RF filter FLl101 (34).

(9) Disconnect adapter CP1103 (35) and remove RF filter FL1102 (36).

(10) Remove the diplexer assembly (37) disconnecting connector P1101 (38) and removing six screws (39), lockwashers (40), flat washers (41), and three clamps (42).

(11) Disconnect connector (43) and remove eight screws (44), lockwashers (45), flat washers (46) and two connectors (47) from high-pass filter (48).

(12) Remove two nuts (49), lockwashers (50), flat washers (51), screws (52), and clamps (53).

(13) Remove four screws (54), lockwashers (55), flat washers (56), and connector (57) on low-pass filter (58).

(14) Remove four screws (59), lockwashers (60), flat washers (61), and connector (62).

(15) Remove grommet (63), four screws (64), lockwashers (65), flat washers (66), and connector (67).

(16) Remove four screws (68), lockwashers (69), flat washers (70), and cover (71) on diplexer-T (72).

(17) Remove nut (73), flat washer (74), and adapter CP1104 (75) on RF switch chassis (76).

b. Assembly. To assemble the RF switch assembly, proceed as follows:

(1) Attach adapter CP1104 (75) to RF switch chassis (76) using nut (73) and flat washer (74).

(2) Install cover (71) on diplexer-T (72) using four screws (68), lockwashers (69), and flat washers (70).

(3) Install connector (67) on diplexer-T using four screws (64), lockwashers (65), and flat washers (66).

(4) Install connector (62) on diplexer-T using four screws (59), lockwashers (60), and flat washers (61).

(5) Install connector (57) on low-pass filter (58) using four screws (54), lockwashers (55), and flat washers (56).

(6) Clamp low-pass filter to diplexer-T using two clamps (53), screws (52), flat washers (51), lockwashers (50), and nuts (49).

(7) Install two connectors (47) on high-pass filter (48) using eight screws (44), lockwashers (45), and flat washers (46).

(8) Connect connector (43) to diplexer-T connector (67) and high-pass filter.

(9) Install grommet (63) between connector (62) and diplexer-T.

(10) Mount diplexer assembly (37) on RF switch chassis (76) using three clamps (42), six screws (39), lockwashers (40), and flat washers (41).

(11) Connect connector P1101 (38) to lowpass filter connector (57).

(12) Mount RF switch S1101 (28) on RF switch chassis using four nuts (24), lockwashers (25), flat washers (26), and screws (27).

(13) Install cable assembly WI101 (19) connecting connector P1102 (18) to high-pass filter connector (47) and connector P1105 (17) to RF switch input.

(14) Connect adapter CPl101 (22) to RF switch Sl101 (28) and RF filter FLl101.

(15) Attach RF filter FLl101 (34) to RF switch chassis using two nuts (29), lockwashers (30), flat washers (31), screws (32), and clamp (33).

(16) Connect adapter CP1103 (35) to adapter CP1104 and RF filter FL1102 (36)

(17) Connect adapter CP1102 (23) to other end of RF filter FL1102 and RF switch output.

(18) Connect connectors P1104 (20) and P1103 (21) to RF switch assembly.

NOTE

Using Antenna AS-1796/GPA-119, schematic diagram as guide (fig. FO-19), solder parts and wires to component board. Use RF switch assembly, exploded view (fig. 3-12) as guide for parts placement on component board.

(19) Attach and solder capacitor C1102 (9), resistor R1103 (10), resistor Rl101 (11), capacitor Cl101 (12), resistor R1104 (13), resistor R1102 (14), and capacitor C1103 (15) to component board (16).

(20) Attach two posts (8) to component board using four nuts (4), lockwashers (5), flat washers (6), and screws (7).

(21) Install component board on RF switch assembly using two screws (1), lockwashers (2), and flat washers (3).

NOTE

Refer to paragraph 3-41b(10) for installing RF switch assembly on antenna AS1796/GPA-119.

3-43. Decoder, Video KY-593/TPX-44 Disassembly and Assembly

For information covering disassembly and assembly of Decoder, Video KY-593/TPX-44, refer to TM 11-5840-309-35.

3-44. Control, Remote Switching C-7014/ TPX-44, Disassembly and Assembly

For information covering disassembly and assembly of Control, Remote Switching C-7014/TPX-44, refer to TM 11-5840-309-35.

3-45. Simulator, Radar Signal SM-472/ TPX-44, Disassembly and Assembly

For information covering the disassembly and assembly of Simulator, Radar Signal 3-66 SM-472/TPX-44, refer to TM 11-5840-32635.

3-46. Interconnecting Box J-2945/ TPX-41, Disassembly and Assembly (fig. 3-13)

a. Disassembly. To disassemble Interconnecting Box J-2945/TPX-41, proceed as follows:

(1) Remove eight screws (1), flat washers (2), and box cover (3).

NOTE

Tag and unsolder wires to switches, relays circuit breaker, and chassis ground terminal.

(2) Remove nut (4), switch S8601 (5), washer (6), and lockwasher (7).

(3) Remove nut (8), switch guard (9), switch S8602 (10), washer (11), and lockwasher (12).

(4) Remove four screws (13), lockwashers (14), flat washers (15), and circuit breaker CB8601 (16).

(5) Remove four nuts (17), lockwashers (18), flat washers (19), screws (20), and connector J8601 (21).

(6) Remove four nuts (22), lockwashers (23), flat washers (24), screws (25), and connector J8602 (26).

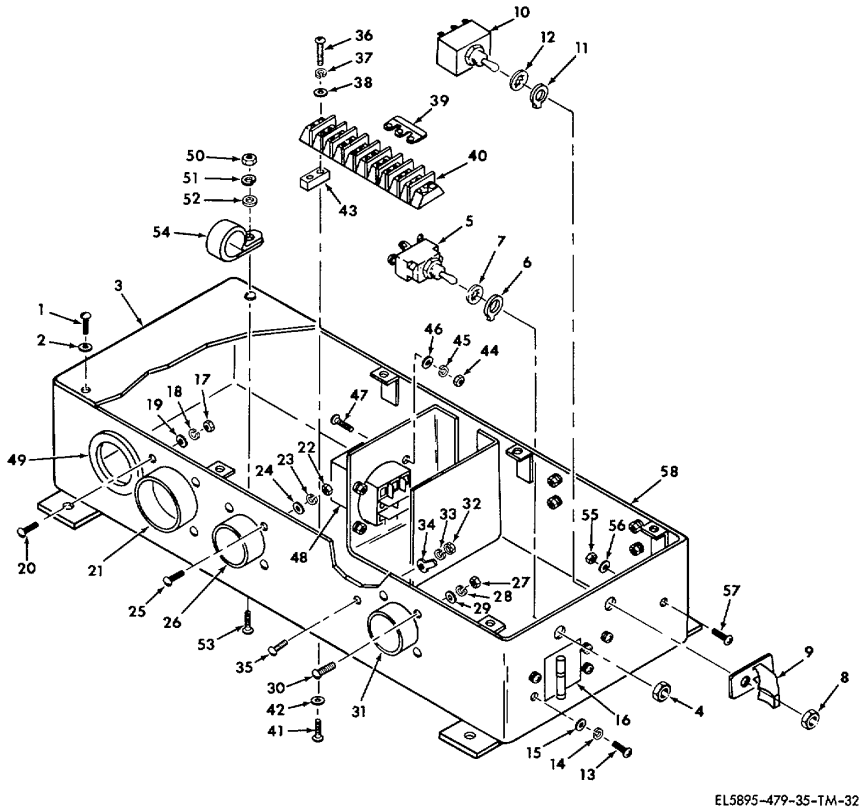
(7) Remove four nuts (27), lockwashers (28), flat washers (29), screws (30), and connector J8603 (31).

(8) Remove nut (32), lockwasher (33), terminal (34), and screw (35).

(9) Remove four screws (36), lockwashers (37), and flat washers (38).

(10) Tag and disconnect wires and bus bar (39) on terminal board TB8601 (40).

(11) Remove terminal board TB8601 (40), four screws (41) flat washers (42), and two spacers (43).



1 Screw (8)
2 Flat washer (8)
3 Cover
4 Nut
5 Switch S8601
6 Washer
7 Lockwasher
8 Nut
9 Switch guard
10 Switch S8602
11 Washer
12 Lockwasher
13 Screw (4)
14 Lockwasher (4)
15 Flat washer (4)
16 Circuit breaker CB8601
17 Nut (4)
18 Lockwasher (4)
19 Flat washer (4)
20 Screw (4)
21 Connector J8601
22 Nut (4)
23 Lockwasher (4)
24 Flat washer (4)
25 Screw (4)
26 Connector J8602
27 Nut (4)
28 Lockwasher (4)
29 Flat washer (4)
30 Screw (4)
31 Connector J8603
32 Nut
33 Lockwasher
34 Terminal
35 Screw
36 Screw (4)
37 Lockwasher (4)
38 Flat washer (4)
39 Bus bar
40 Terminal board TB8601
41 Screw (4)
42 Flat washer (4)
43 Spacer (2)
44 Nut (4)
45 Lockwasher (4)
46 Flat washer (4)
47 Screw (4)
48 Relay K8601
49 Grommet
50 Nut
51 Lockwasher
52 Flat washer
53 Screw
54 Clamp
55 Nut (2)
56 Flat washer (2)
57 Screw (2)
58 Chassis

Figure 3-13. Interconnecting Box J-2945/TPX-41, disassembly and parts location.

(12) Remove four nuts (44), lockwashers (45), flat washers (46), screws (47), and relay K8601 (48).

(13) Remove grommet (49).

(14) Remove nut (50), lockwasher (51), flat washer (52), screw (53), and clamp (54).

(15) Remove two nuts (55), flat washers (56), and screws (57) on chassis (58).

b. Assembly. To assemble Interconnecting Box J-2945/TPX-41, proceed as follows:

(1) Install two screws (57), flat washers (56), and nuts (55) on chassis (58).

(2) Attach clamp (54) to chassis using nut (50), lockwashers (51), flat washer (52), and screw (53).

(3) Install grommet (49) on chassis.

(4) Using Interconnecting Box J-2945/TPX-41, wiring diagram as guide (fig. FO-8), solder wires to relay K8601.

(5) Attach relay K8601 (48) to chassis bracket using four nuts (44), lockwashers (45), flat washers (46), and screws (47).

(6) Install two spacers (43) using four screws (41) and flat washers (42).

(7) Position terminal board TB8601 (40) on two spacers (43) and secure using four screws (36), lockwashers (37), and flat washers (38).

(8) Using Interconnecting Box J-2945/TPX-41, wiring diagram as guide (fig. FO-8), attach wires and bus bar (39) to terminal board TB8601.

(9) Using Interconnecting Box J-2945/TPX-41, wiring diagram as guide (fig. FO-8), solder wire(s) to terminal (34).

(10) Attach terminal to chassis using nut (32), lockwasher (33), and screw (35).

(11) Using Interconnecting Box J-2945/ TPX-41, wiring diagram as guide (fig. FO-8), solder wires to connector J8603.

(12) Install connector J8603 (31) using four nuts (27), lockwashers (28), flat washers (29), and screws (30).

(13) Using Interconnecting Box J-2945/ TPX-41, wiring diagram as guide (fig. FO-8), solder wires to connector J8602.

(14) Install connector J8602 (26) using four nuts (22), lockwashers (23), flat washers (24), and screws (25).

(15) Using Interconnecting Box J-2945/ TPX-41, wiring diagram as guide (fig. FO-8), solder wires to connector J8601.

(16) Install connector J8601 (21) using four nuts (17), lockwashers (18), flat washers (19), and screws (20).

(17) Install circuit breaker CB8601 (16) using four screws (13), lockwashers (14), and flat washers (15).

(18) Using Interconnecting Box J-2945/ TPX-41 wiring diagram as guide (fig. FO-8), solder wires to circuit breaker CB8601.

(19) Install switch S8602 (10) and switch guard (9), using nut (8), washer (11), and lockwasher (12).

(20) Using Interconnecting Box J-2945/ TPX-41 wiring diagram as guide (fig. FO-8), solder wires to switch S8602.

(21) Attach box cover (3) to chassis using eight screws (1)and flat washers (2).

CHAPTER 4

DIRECT SUPPORT TESTING

4-1. General

This chapter covers direct support testing of the major components that comprise Interrogator Set AN/TPX-41. These tests should be used to evaluate equipment performance after completion of repair and adjustment operations. To accomplish tests requiring voltage or signal measurement, it is required that the component under test be properly installed in an operable AN/ TPX-41 system. Each test in this chapter is preceded by a list of test equipment and materials required to perform the test, equipment conditions that are a prerequisite to accomplishing the test, references to test connection diagrams as applicable, and any special instructions required to perform the test. Instructions for connecting and operating the test equipment required for each test are contained in the respective test procedures. Perform the tests in the order presented and follow the procedural steps in each test in the order given.

4-2. Direct Support Test Procedures

Paragraphs 4-2 through 4-10 cover direct support test procedures for major components of Interrogator Set AN/TPX-41. The major components of the AN/TPX-41 are listed in *a* through j below with references to the paragraphs covering direct support testing of each.

a. Blanker, Interference MX-8745/TPX-41 (paras 4-3 through 4-5).

b. Coder-Control KY-97C/TPX (para 4-6).

c. Control, Remote Switching C-1271A/TPX22((para 4-7

d. Modulator, Pulse MD-638/TPX-41 (para 4-8 and 4-9).

e. Receiver-Transmitter, Radio RT-264D/ UPX-6 (para 4-10).

f. Antenna Group AN/GPA-119 (para 4-11).

g. Decoder, Video KY-593/TPX-44 (para 4-12).

h. Control, Remote Switching C-7014/TPX44 (para 4-13).

i. Simulator, Radar Signal SM-472/TPX-44 (para 4-14).

j. Interconnecting Box J-2945/TPX-41 (para 4-15).

4-3. Blanker, Interference MX-8795/TPX-41, DC Vom DC Voltage Test

a. Test Equipment and Materials. Multimeter ME-26B/U.

b. Test Conditions and Connections (fig. 4-1).

(1) On MX-8795/TPX-41, place POWER switch S31101 to ON.

(2) On Interconnecting Box J-2945/TPX41, place IFF POWER circuit breaker CB8601 to ON.

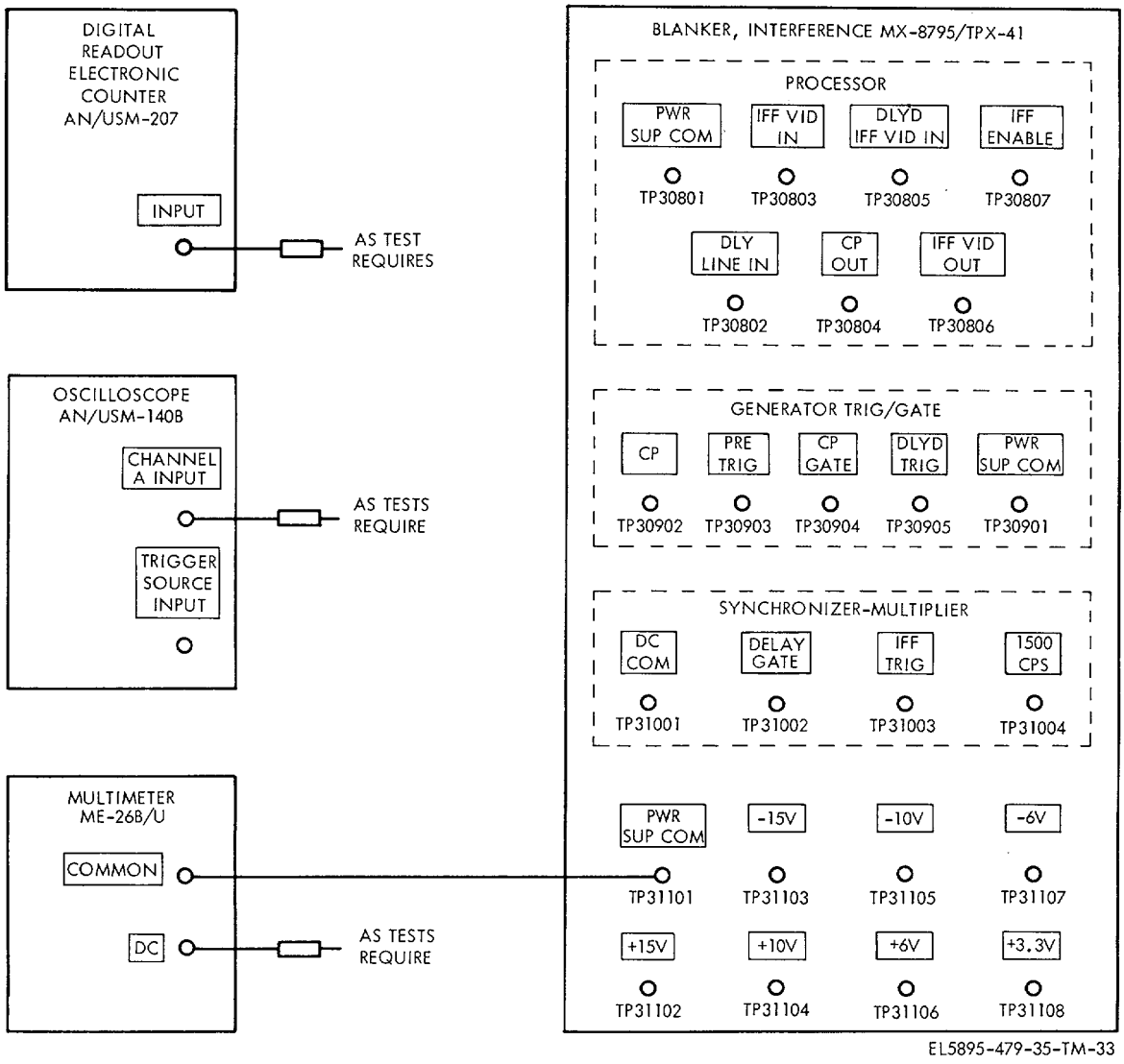


Figure 4-1. Blanker, Interference MX-8795/TPX-41, direct support test connections.

c. Procedure

Step No	Control settings		Test equipment	Performance standard
	Test procedure	Equipment under test		
1	*ME-26B/U* FUNCTION: + RANGE: 30 V	*MX-8795/TPX-41* POWER: ON	On ME-26B/U, connect COMMON test lead to PWR SUP COM test point TP31101 and connect dc test lead to +15V test point TP31102.	+15v
2	Same as step 1	Same as step 1	Connect DC test lead to +10V test point TP31104.	+10 ±1v

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
3	*ME-26B/U* FUNCTION: + RANGE: 10V	Same as step 1 ----------	Connect dc test lead to +6V test point TP31106.	+6 +0.5v
4	Same as step 3 ---	Same as step 1 ----------	Connect dc test lead to +3.3V test point TP31108.	+3.3 +0.25v
5	*ME-26B/U* FUNCTION: - RANGE: 30V	Same as step 1 ----------	Connect dc test lead to -15V test point TP31103.	-15v
6	Same as step 5 ---	Same as step 1 ----------	Connect de test lead to -10V test point TP31105.	-10 +lv
7	*ME-26B/U* FUNCTION: - RANGE: 10V	Same as step 1 ----------	Connect dc test lead to -6V test point TP31107.	-6 +0.5v
8	*ME-26B/U* FUNCTION: OFF	*MX-8795/TPX-40* POWER: OFF	Disconnect ME-26B/U and re-store MX-8795/TPX-41 to service.	None

4-4. Blanker, Interference

MX-8795/TPX-41, Timing Test

a. Test Equipment and Materials Required. Oscilloscope AN/USM-140B, including MX2962/USM subassembly.

b. Test Conditions and Connections (fig. 4-1).

(1) On MX-8795/TPX-41, release four captive screws on front panel and slide chassis forward from dust cover to expose test points on circuit cards.

(2) On MX-8795/TPX-41, place POWER switch S31101 to ON.

(3) On Interconnecting Box J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON.

(4) On MX-8795/TPX-41, disconnect connector P31106 from connector J31106, install adapter UG-274B/U on J31106, connect P31106 to one side of adapter and connect open side of adapter to TRIGGER SOURCE INPUT on AN/USM-140B.

c. Procedure.

Step	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	*AN/USM-140B* POWER: ON ASTIGMATISM: midposition FOCUS: midposition midposition midposition SCALE LIGHT: pulse duration as indicated on fully cw AN/USM-140B. CHANNEL A VER-TICAL POSITION: midposition	*MX-8795/TPX-41* POWER: ON PRF SEL Switch S3: 2	*a.* On AN/USM-140B, connect CHANNEL A INPUT test lead to PRE TRIG test point TP-30903 on trigger/gate gener-ator subassembly. *b.* On trigger/gate generator sub-assembly, adjust PW ADJ con-trol R30907 for a positive	*a.* None. *b.* 0.4 μsec.

Step No	Control settings: Test equipment	Control settings: Equipment under test	Test Procedure	Performance standard
	HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY: INTERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: MICROSECONDS/CM: 1 VERNIER: CAL TRIGGER SLOPE: + TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT DC CHANNEL A-CHANNEL B: CHANNEL A CHANNEL A SENSITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL A AC-DC: DC Remaining controls may be in any position.			
2	As last indicated, except: AN/USM-140B SWEEP TIME: (MILLISECONDS/CM): .2	Same as step 1	*a.* On AN/USM-140B, remove CHANNEL A INPUT from PRE-TRIG test point TP-30903 and connect to IFF ENABLE test point TP30807 on processor subassembly.	*a.* None.
			b. On trigger/gate generator subassembly, adjust IFF GATE control R30902 for a correct negative gate duration.	*b.* 2450 usec.
			c. On AN/USM-140B, remove CHANNEL A INPUT from IFF ENABLE test point TP-30807 and connect to CP GATE test point TP30904 on trigger/gate generator subassembly.	*c.* None.
			d. On trigger/gate generator subassembly, adjust CP GATE control R30936 for a correct positive gate duration.	*d.* 2550 usec.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			e. On AN/USM-140B, remove CHIANNEL A INPUT from CP GATE test point TP30904 and connect to DLYD TR.IGC test point TP30905 on trigger/ gate generator subassembly.	e. None.
3	As last indicated, except: AN/USM-i40Bt *AN/USM-140B* *A* USWF,EP TIME: SWEEP TIME: (MICROSECON:DS, CM): 5	Same as step 1 , ,	*a.* On AN/USM-140B, connect CHANNEL B INPUT to CP test point TP309s2 or, trigger/ gate generator subassembly.	a None.
			b. On trigger/gate generator subassembly, adjust DELAY ADJ control R30942 for delay of 90 µsec between trigger at TP30905 and sync trigger at TP30902.	*b.* None.
4	As last indicated, except: *ANIAUSM-140B* SWEEP TIME: MICROSE CONDSEP (MICROSECONDS/ CM): 1	Same as step 1	On AN/USM-140B, remove CHANNEL A INPUT from DLYD TRIG test Point TP-30905 and connect to IFF TRIG test point TP31003 on synchronizer-multiplier verify pulse width is proper duration.	0.5 µsec
5	As last indicated, except: *SAWEE/US T-I40B* S(W MILLISECONDS/ (MILLISECONDS/ CM): .2	Same as step 1	On AN!USM-140B, remove CHANNEL A INPUT from IFF TRIG test point TP31003 and connect to DEL,AY GATE test point TP31002.	Observe a square wave similar to that shown in M, fig. 3-2.
6	As last indicated except: (MISWEEP TIME: MILLISECONDM:	Same as step 1	On AN/USM-140B, CHANNEL A INPUT from DELAY GATE test point TP31102, connect to 1500 CPS test point TP31104 and observe three complete cycles of the 1500-Hz signal.	removeSine wave: 1500 Hz 20v pp (nom).
7	As last indicated ---- POWER: OFF	*MX-8795/TPX-41*	Disconnect AN/USM-140B and restore MX-8795/TPX-41 to service.	None.

4-5. Blanker, Interference MX-8795/ TPX-41, Video Processing Test

a Test Equipment and Materials Required.

Oscilloscope AN/USM-140B, including MX-29 62/USM subassembly.

b Test Conditions and Connections (fig. 4-1).

(1) On M-8795/TPX-41, release four captive screws on front panel and slide chassis forward from dust cover to expose test points on circuit cards.

(2) On Interconnecting Box J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON, SCAN switch S8601 to ON, and IFF SCAN switch S8602 to OPERATE.

(3) On R-264D/UPX-6, place POWER switch (S104) to ON.

(4) On K-97C/TPX, place POWER switch (S407) to ON, LOCAL-REMOTE switch ($402) to LOCAL, RECEIVER GAIN control (R446) to 10, and CHALLENGE switch (S404) to ON.

(5) On S-472/TPX-44, place POWER switch (Sl) to ON, B + ON switch (S2) to LOCAL, TRIG IN switch (S3) to PULSE, OUTPUT LEVEL control (R51) to midrange, and DELAY control (R25) to scribed mark selected for operating range.

(6) On M-638/TPX-41, place POWER switch (S1301) to ON.

c. Procedure.

Step no.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	*AN/USM-140B* POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALE LIGHT: fully cw CHANNEL A VERTICAL POSITION: midposition HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY: INTERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: (MICROSECONDS/CM): 1 VERNIER: CAL TRIGGER SLOPE: as desired TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT DC CHANNEL A-CHANNEL B: CHANNEL A CHANNEL A SENSITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL A AC-DC: DC Remaining controls may be in any position.	*MX-8795/TPX-41* POWER: ON PROCESSED VIDEO-RAW VIDEO: RAW VIDEO PRF SEL Switch S3: 2	On AN/USM-140B, connect CHANNEL A INPUT to IFF VID IN test point TP30803 on processor subassembly and using UG-274/U T-connector, connect TRIGGER SOURCE INPUT to IFF trigger connector J31105 on MX-8795/TPX-41.	None.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
2	As last indicated	Same as step 1	*a.* On SM-472/TPX-44, rotate DELAY control R25, and OUTPUT LEVEL control R51 until 3v peak pulse train is observed on AN/USM-140B. If necessary, on left side of RT-264D/UPX-6 (TM 11-5895-468-12), rotate video limiting control R325 cw to increase limiting level of video input to MX-8795/TPX-41.	*a.* Video pulse train (5v nom).
			b. On AN/USM-140B, move CHANNEL A INPUT to IFF VID OUT test point TP30806 on processor subassembly	*b.* Synchronous, and nonsynchronous replies due to interrogation from other ground stations, are displayed.
3	As last indicated	*MX-8795/TPX-41* *PROCESSED* VIDEO-RAW VIDEO: PROCCESSED VIDEO	Observe IFF video on AN/USM 140B	Nonsynchronized replies are removed, and standardized synchronous replies remain.
4	As last indicated-	*MX-8795/TPX-41* POWER: OFF	Disconnect AN/USM-140B and return MX-8795/TPX-41 to service.	None.

4-6. Coder-Control KY-97C/TPX, Direct Support Testing

For information pertaining to the testing of Coder-Control KY-97C/TPX, refer to TM 11-5895-201-35.

4-7. Control, Remote Switching C-1271A/TPX-22,

Continuity Test

a. Test Equipment and Materials Required Multimeter TS-352B/U.

b. Test Conditions and Connections (fig. 4-2). All external cables disconnected.

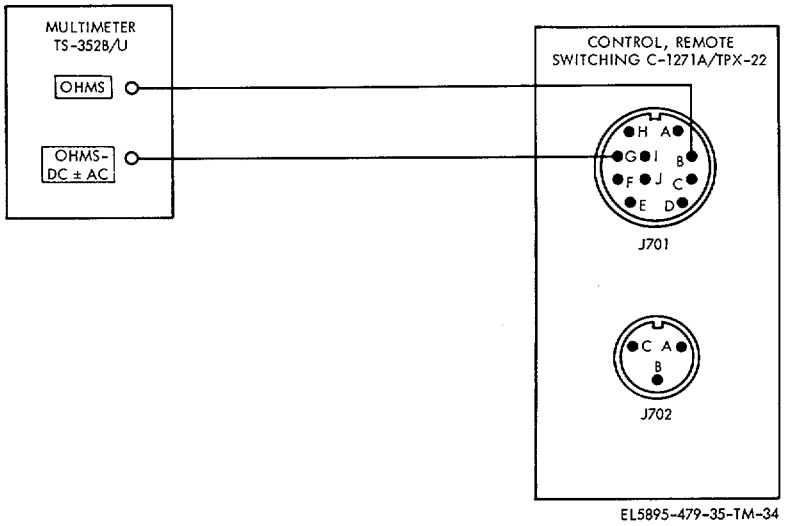


Figure 4-2. Control, Remote Switching C-1271A/TPX-22, direct support test connections.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	*TS-352/U* FUNCTION: OHMS Range: RX10 OHMS ZERO ADJ: for meter Q with test leads shorted	*C-1271A/TPX-22* MODE SELECTOR switch S731: 1 GTC switch S734: LONG CHOP switch S732: OFF RECEIVER GAIN control R731 : fully cw	*a.* On TS-352/U, observe indication on OHMS (top) scale while, on C-1271A/TPX-22, rotating MODE SELECTOR switch S701 to all three positions.	a. TS-352/U should indicate Q on MODE 1 position and infinity on MODE 2 and MODE 3 positions.
			b. On TS-352/U, remove red test lead from pin B and connect to pin H on J731.	b. None.
			c. Repeat step a above	c. TS-352/U should indicate 0 on MODE 3 position and infinity on positions MODE 2 and MODE 1.
			d. On TS-352/U, remove red test lead from pin H at J731 and connect to pin A on J732.	*d.* None.
			e. Repeat step a above	*e.* Same as step a above.
			f. On TS-352/U, remove red test lead from pin A and connect to pin C on J732.	*f.* None.
			g. Repeat step a above ----------	*g.* Same as step c above.
			h. On TS-352/U, remove red test lead from pin C and connect to pin B on J732.	*h.* None.
			i. On TS-352/U, observe indication	*i.* TS-352/U should indicate 0 ohms.
			j. On TS-352/U, remove red test lead from J732 pin B and connect to pin E on J731.	j. None.
			k. On TS-352/U, observe indication on OHMS scale	*k.* T S-352/U indicates 15+5 ohms.
			l. On TS-352/U, remove red test lead from pin E and connect to pin A on J731.	*l.* None.
m. TS-352/U indicates 0 ohms.			*m.* CHOP switch S732 to ON, and on TS-352/U, observe indication.	On C-1271A/TPX-22, place
			n. On TS-352/U, remove red test lead from pin A and connect to pin F on J731.	*n.* None.
			o. On C-1271A/TPX-22, place GTC switch S734 to SHORT and observe TS-352/U.	*o.* Same as step *m* above.
			p. On TS-352/U, remove red test lead from pin F and connect to pin C on J731.	*p.* None.
			q. On C-1271A/TPX-22, momentarily depress PUSH-TO-CHAL switch S733 and observe TS-352/U.4-8	*q.* Same as step m above.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			r. On TS-352/U, remove red test lead from pin C and connect to pin I on J731.	*r.* None.
			s. On TS-352/U, observe indication	s. TS-352/U indicates 15 _5 ohms.
			t. On TS-352/U, remove red test lead from pin I and connect to pin D on J731.	*t.* None.
			u. On TS-352/U, remove black test lead from pin G and connect to pin J on J731.	u. None.
			v. On TS-352/U, place range switch to RX10.	v. None.
			w. On TS-352/U. observe indication on OHMS scale, while on C-1271A!TPX-22, slowly rotating RECEIVER GAIN control R731 fully ccw of 1000 +100 ohms (100 on OHMS scale).	*w.* On TS-352/U, indication should increase smoothly, without fluctuation. On TS-352/U, with control R731 fully ccw, observe indication
			x. Disconnect TS-352/U, and restore C-1271A/TPX-22 to service.	x. None.

4-8. Modulator, Pulse MD-638/TPX-41, DC Voltage Test

a. Test Equipment and Materials Required.
Multimeter ME-26B/U.

b. Test Conditions and Connections. On Interconnecting Box J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON.

c. Procedure.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	*ME-26B/U* FUNCTION: - RANGE: 1OOV	*MD-638/TPX-41* POWER: ON SLS: ON	On ME-26B/U, connect COMMON test lead to CKT COM test point TP1301 and connect DC test lead to -30V test point TP1302.	-30 ±3v
2	*ME-26B/U* FUNCTION: + RANGE:300V	Same as step 1	On ME-26B/U, remove DC test lead from -30V test point TP1302 and connect to +250V test point TP1303.	+250 ±25v
3	*ME-26B/U* FUNCTION: OFF	*MD-638/TPX-41* POWER: OFF SLS: OFF	Disconnect ME-26B/U and restore MD-638/TPX-41 to service.	None

4-9. Modulator, Pulse MD-638/TPX-41, Pulse Test

a Test Equipment and Materials Required.

(1) Oscilloscope AN/USM-140B, including MX-2962/USM subassembly.

(2) Test Set, Radar AN/UPM-6B.

b Test Conditions and Connections (fig. 4-3).

(1) Connect test equipment as shown in figure 4-3.

(2) On J-2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON.

(3) On RT-264D/UPX-6, place POWER switch (S104) to ON.

(4) On MX-8745/TPX-41, place POWER switch (S31101) to ON.

(5) On K-97C/TPX, place LOCALREMOTE switch (S402) to LOCAL, MODE SELECTOR switch (S403) to 1, and CHALLENGE switch (S404) to ON.

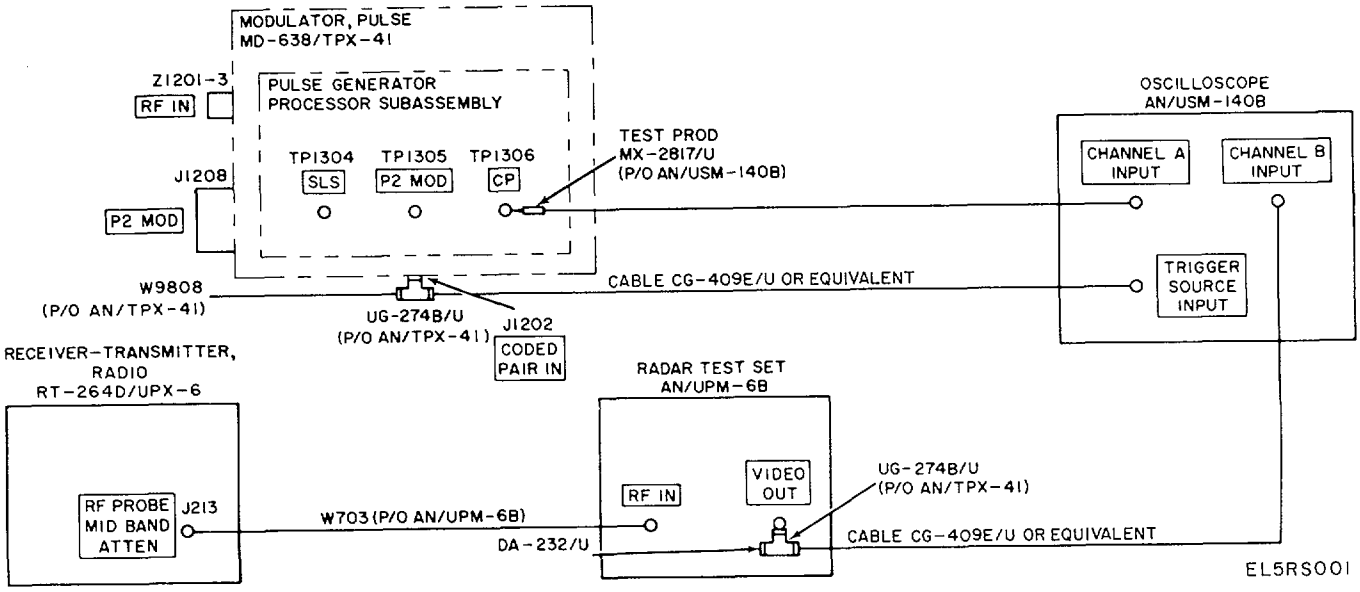


Figure 4-3. Modulator, Pulse MD-638/TPX-41, direct support test connections.

c. Procedure.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/USM-140B POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALE LIGHT: fully cw CHANNEL A VERTICAL POSITION: midposition HORIZONTAL POSITION: midposition	MD-638/TPX-41 POWER: ON SLS: ON	On ANIUSM-140B, CHANNEL B, observe interpulse spacing of P1 and P2 pulses.	Half-amplitude points on leading edges of pulses P1 and P2 are 1.9usec apart.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	HORIZONTAL DISPLAY INTERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: (MICRO-SECONDS/CM): 1 VERNIER: CAL TRIGGER SLOPE: as desired TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT DC CHANNEL A-CHANNEL B: ALTERNATE CHANNEL A SEN-SITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL A AC-DC: DC CHANNEL B SEN-SITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL B AC-DC:DC Remaining controls may be in any position.			
2	As last indicated	As last indicated	On AN/USM-140B, CHANNEL B, observe pulse width of P2 pulse at half-amplitude points.	0.7 µsec
3	As last indicated	As last indicated	On AN/USM-140B, CHANNEL B, observe amplitude and pulse width of control pulse taken at CP test point TP1306.	Amplitude: 55v peak (min), with baseline at -20 ±6v. Pulse width: 1.2 ±0.2 µsec.
4	As last indicated	As last indicated---	*a.* On AN/USM-140B, use HORIZONTAL POSITION control to position trailing edge of P2 pulse on vertical grid line for reference.	a. None.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			b. On AN/USM-140B, observe time relationship of trailing edge of P2 pulse and CP pulse.	*b.* Coincident.
5	As last indicated	As last indicated	On AN/USM-140B, connect CHANNEL A INPUT TO P2 MOD testpoint TP1305 and observe amplitude of P2 pulse	+180v peak (min).
6	As last indicated, except: *AN/USM-140B* POWER: OFF	*MD-638/TPX-41* POWER: OFF SLS: OFF	Disconnect all test equipment and restore MD638/TPX-41 to service.	None.

4-10. Receiver-Transmitter, Radio RT-264D/UPX-6, Direct Support Testing

For information pertaining to the testing of Receiver-Transmitter, Radio RT-264/UPX-6, refer to TM 11-5895-245-35.

4-11. Antenna AS-1796/GPS-119, Radiation Test

a. Test Equipment and Materials Required.

(1) Oscilloscope A/USM-140B.

(2) Test Se, Radar AN/UPM-6B.

(3) Antenna AssemblyAT-197/GP.

b. Test Conditionsand Connections (fig. 4-4).

(1) Connect test equipment as shown in figure 4-4.

(2) On -2945/TPX-41, place IFF POWER circuit breaker CB8601 to ON.

(3) On R--264D/UPX-6, place POWER switch (S104) to ON.

(4) On M-8745/TPX-41, place POWER switch (S31101) to ON.

(5) On K-97C/TPX, place LOCALREMOTE switch (S402) to LOCAL, MODE SELECTOR switch (S403) to 1, and CHALLENGE switch (S404) to ON.

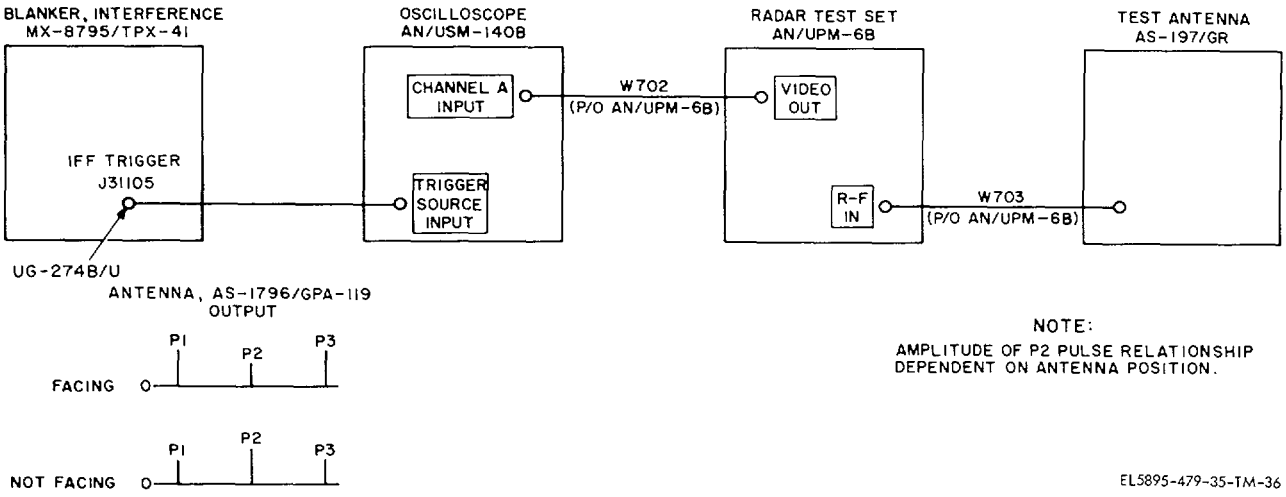


Figure 4-4. Antenna AS-1796/GPA-119, direct support test connections.

c. Procedure

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	*AN/USM-140B* POWER:ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALE LIGHT: fully cw CHANNELA VERTICAL POSITION: midposition HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY.- INTERNAL SWEEP MAGNIFIER: XI EXTERNAL VERNIER: CAL AC-DC:DC SWEEP TIME: MICROSECOND/CM): 1 VERNIER: CAL TRIGGER SLOPE: as desired TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT DC CHANNEL A-CHANNELB: CHANNELA CHANNELASENSITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL A AC-DC:DC Remaining controls may be in any position.	*AS-1796lGPA-119* None.	*a.* Temporarily mount AT-197/GR on convenient object at least 8 feet above ground, between 25 to 50 feet from AS-1796/GPA-119. *b.* Manually rotate AS-1796/GAP-119 to point directly at AT-197/GR. Observe waveform on AN/USM-140B. *c.* On J-2945/f?X-41, place SCAN switch S8601 to ON and IFF SCAN switch S8602 to OPERATE.	a. None. *b.* P2 pulse is lower in amplitude than PI and P3 pulses (as shown in fig. 4-4). c. On AN/USM-140B, observe that during antenna rotation, P2 pulse has greater amplitude than PI and P3 pulses, except during time AS-1796/GPA-119 points directly, or almost directly, at AT-197/GR. At time AS-1796/GPA-119 is almost pointing directly at AS-197/GR, amplitude of P2 should decrease while amplitude of PI and P3 increase until they are significantly greater than P2.
2	As last indicated	As last indicated	*a.* Place AN/FPN-40 in operating condition. *b.* On ppi indicator, locate easily discernible radar target with accompanying IFF reply.	a. Antenna AS-1079/FPN-40 rotates, and aircraft targets appear on ppi. *b.* IFF reply is centered directly behind radar target.
3	As last indicated, except: *ANIUSM-140B* POWER:OFF	As last indicated	Disconnect all test equipment and restore AS-1796/GPA-119 to service.	None

4-12. Decoder, Video KY-593/TPX-44, Direct Support Testing

For information pertaining to the testing of Decoder, Video KY-593/TPX-44, refer to TM 11-5840-309-35.

4-13. Control, Remote Switching C-7014/TPX-44, Direct Support Testing

For information pertaining to the testing of Control, Remote Switching C-7014/TPX-44, refer to TM 11-5840-309-35.

4-14. Simulator, Radar Signal SM-472/ TPX-44, Direct Support Testing

For information pertaining to the testing of Simulator, Radar Signal SM-472/TPX-44, refer to TM 11-5840-326-35.

4-15. Interconnecting Box J-2945/ TPX-41, Continuity Test

a. Test Equipment and Materials Required.
Multimeter ME-26B/U.

b. Test Conditions and Connections (fig. 4-5).
All external cables disconnected and side panel removed.

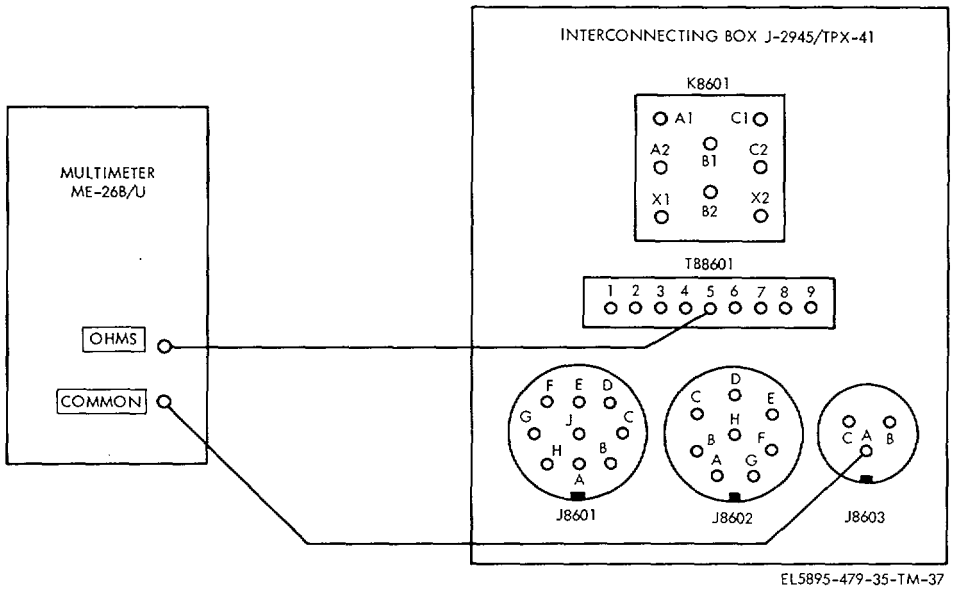


Figure 4-5. Interconnecting Box J-2945/TPX-41, direct support test connections.

c. Procedure.

Step no.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	*ME-26B/U* FUNCTION: OHMS RANGE: RX10 OHMS ADJ: Set for ∅ indication with OHMS test lead and COMMON test lead connected.	*J-2945/TPX-41* IFF POWER: OFF SCAN: OFF *IFF* SCAN:	*a.* On ME-26B/U, connect COMMON test lead to J8603-A and connect OHMS test lead to TB8601-5. *b.* On ME-26B/U, connect SAFE COMMON test lead to J8603-A and connect OHMS test lead to TB8601-6. c. On ME-26B/U, connect COMMON test lead to J8603-A and connect OHMS test lead to TB8601-4.	a. ME-26B/U indicates infinity. b. ME-26B/U indicates infinity. c. ME-26B/U indicates infinity.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			d. On ME-26B/U, connect COMMON test lead to J8603-A and connect OHMS test lead to K8601-B1.	*d.* ME-26B/U indicates infinity.
2	As last indicated except: *J-2945/TPX-41* IFF POWER: ON	As last indicated	*a.* Same as step la (above) *b.* Same as step lb (above) *c.* Same as step ic (above) *d.* Same as step ld (above)	a. ME-26B/U indicates 0 ohms. b. ME-26B/U indicates 0 ohms. c. ME-26B/U indicates 0 ohms. *d.* ME-26B/U indicates 0 ohms.
3	As last indicated .	As last indicated	On ME-26B/U, connect COMMON test lead to J8603-B and connect OHMS test lead to TB8601-7.	ME-26B/U indicates 0 ohms.
4	As last indicated	As last indicated.	On ME-26 B/U, connect COMMON test lead to J8601-J and connect OHMS test lead to TB8601-9.	ME-26B/U indicates 0 ohms.
5	As last indicated---	--. As last indicated----	*a.* On ME-26B/U, connect COMMON test lead to J8601-C and connect OHMS test lead to J8601-G.	a. ME-26B/U indicates infinity.
	As last indicated, except: *J-2945/TPX-41* SCAN: ON	*b.* Same as step 5 a (above)	*b.* ME-26B/U indicates 0 ohms.	
6	As last indicated	As last indicated	*a.* On ME-26B/U, connect COMMON test lead to J8601-G and connect OHMS test lead to K8601-X2.	a. ME-26B/U indicates infinity.
		As last indicated, except: *J-2945/TPX-41* IFF SCAN: OPERATE	*b.* Same as step 6a(above)	b. ME-26B/U indicates ∅ ohms.
7	As last indicated	As last indicated .	On ME-26B/U, connect COMMON test lead to J8601-H and connect OHMS test lead to K8601-B2.	ME-26B/U indicates ∅ ohms.
8	As last indicated	-- As last indicated	- On ME-26B/U, connect COMMON test lead to K8601-X1 and OHMS test lead to K8601-X2.	ME-26B/U indicates 170 +20 ohms.
9	As last indicated, except: *ME-26BIU* FUNCTION: OFF	*J-2945/TPX-41* IFF POWER: OFF SCAN: OFF FF SCAN: SAFE	Disconnect ME-26B/U and restore J-2945/TPX-41 to service.	None.

CHAPTER 5

GENERAL SUPPORT MAINTENANCE

Section I GENERAL

5-1. Scope of General Support Maintenance

The specific maintenance duties of the genera support maintenance repairman are listed in *a* through *d* below with references to the paragraph covering the specific maintenance function Ideally, the performance of these duties entails only those maintenance operations designated specifically for general support maintenance. How ever, some equipment problems which are correct able at the direct support level of maintenance may be referred to general support maintenance due to the difficulty involved in identifying the problem. For this reason, the maintenance duties of the general support maintenance repairman also in include the maintenance responsibilities of the direct support maintenance repairman as described i paragraph 3-1.

a. Troubleshooting (para 5-3).

b. Adjustment and alignment (para 5-4).

c. Repair para 5-5).

d. Removal and replacement (para 5-6).

5-2. Tools, Test Equipment, and Materials Required

a. Tools. Tools required for general support maintenance are listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

b. Test Equipment. Test Equipment required for general support maintenance is listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

c. Materials. The applicable repair parts allocated for general support maintenance are listed in TM 11-5895-479-35P.

Section II. GENERAL SUPPORT TROUBLESHOOTING

5-3. General

This section references pertinent troubleshooting data to aid the general support repairman in the rapid identification and correction of equipment malfunctions. This data is comprised of the information contained in the direct support troubleshooting section of this manual. Specific types of troubleshooting data are listed in *a* through *i* below with references to the paragraphs providing coverage of each.

a. Troubleshooting techniques (para 3-4).

b. Identification of intermittents (para 3-5).

c. Diagrams para 3-6).

d. Reference designations (para 3-7).

e. Voltage and resistance measurements (para 3-8).

f. Parts substitution (para 3-9).

g. Waveform analysis (para 3-10).

h. System troubleshooting chart (para 3-11).

i. Major component troubleshooting (para 3-12).

5-4. Adjustment and Alignment Procedures

These procedures are contained in the direct support adjustment and alignment section of this manual. Each procedure is preceded by a list of test equipment required to perform the procedure and the prerequisite equipment conditions necessary to accomplish the procedure. Specific adjustment and alignment procedures are listed in *a* through *n* below with references to the paragraphs containing detailed instructions for the performance of each procedure. Where adjustment and alignment procedures for specific components are covered in separate manuals, the applicable TM is referenced as necessary.

a. Blanker, Interference MX-8795/TPX-41, positive 15-volt power supply adjustment (para 3-14).

b. Blanker, Interference MX-8795/TPX-41, negative 15-volt power supply adjustment (para 3-15).

c. Blanker, Interference MX-8795/TPX-41, timing adjustment (para 3-16).

d. Coder, Control KY-97C/TPX-41, adjustment and alignment procedures (TM 11-5895-201-35).

e. Control, Remote Switching C-1271A/ TPX-22, adjustment and alignment procedures (para 3-18).

f. Modulator, Pulse MD-638/TPX-41, P2 pulse timing adjustment (para 3-19).

g. Modulator, Pulse MD-638/TPX-41, P2 pulse width adjustment (para 3-20).

i. Receiver-Transmitter, Radio RT-264D/UPX-6, adjustment and alignment procedures (TM 11-5895-245-35).

j. Antenna GroupAN/GPA-119, synchro alignment (para 3-23).

k. Decoder, Video KY-593/TPX-44, adjustment and alignment procedures (TM 11-5840-309-35).

l. Control, Remote Switching C-1271A/ TPX-44, adjustment and alignment procedures (TM 11-5840-309-35).

m. Simulator, Radar Signal SM-472/TPX-41, adjustment and alignment procedures (TM 11-5840-326-35).

n. Interconnecting Box J-2945/TPX-41, adjustment and alignment procedures (para 3-27).

5-5. Repair Procedures

Repair instructions are contained in the direct support repair section of this manual. Specific repair operations are listed in *a* through *d* below with references to paragraphs that provide pertinent instructions for each type of repair operation.

a Electronic component repair (para 3-29).

b Mechanical parts repair (para 3-30).

c Coaxial cable repair (para 3-31).

d Multiconductor cable repair (para 3-32).

Section III. REMOVAL AND REPLACEMENT; DISASSEMBLY AND REASSEMBLY

5-6. General

This section covers complete disassembly and reassembly of Pedestal, Antenna AB-1158/ GPA-119 and references applicable removal, replacement, disassembly, and reassembly procedures for all other major components of Interrogator Set AN/TPX-41. The disassembly and reassembly instructions for the AB-1158/GPA119 (para 5-7) consist of step-by-step procedures keyed to accompanying illustrations that portray the units, assemblies, and parts of the AB-1158/GPA-119 in an exploded view. Before disassembling the AB-1158/GPA-119, study the exploded view and note the relationships between the various parts and subassemblies. During disassembly, give particular attention to the assemblage of complex mechanical assemblies. Close study will provide for ease of disassembly and serve as an aid during reassembly. Major components of the AN/TPX-41,

except the AB-1158/GPA-119, are listed in *a* through *k* below, with references to the paragraphs covering disassembly and reassembly of each. Where disassembly and reassembly instructions for a particular major component are contained in a separate manual, the applicable TM is referenced as necessary.

a. Blanker, Interference MX-8795/TPX-41 (para 3-34).

b. Coder Control KY-97C/TPX (TM 11-5895201-35).

c. Control, Remote Switching C-1271A/ TPX-22 (para 3-36).

d. Modulator, Pulse MD-638/TPX-41 (para 3-37).

e. Receiver Transmitter, Radio RT-264D/ UPX-6 (TM 11-5895-245-35).

f. Antenna GroupAN/GPA-119 (para 3-39).

g. Antenna A-1796/GPA-119 (paras 3-41 and 3-42).

h. Decoder, Video KY-593/TPX-44 (TM 11-5840-309-35).

i. Control, Remote Switching C-7014/TPX-44 (TM 11-5840-309-35).

j. Simulator, Radar Signal SM-472/TPX-44 (TM 11-5840-326-35).

h. Interconnecting BoxJ-2945/TPX-41 (para 3-46).

5-7. Pedestal, Antenna AB-1158/GPA-119, Disassembly and Assembly (fig. 5-1)

a. Disassembly. To disassemble Pedestal, Antenna AB-1158/GPA-119, proceed as follows:

(1) Remove four screws (1), lockwashers (2), flat washers (3), and two protection angles (4).

(2) Disconnect and remove rotary joint (5).

(3) Remove packing (6).

(4) On one protection angle, remove nut (7), lockwasher (8), flat washer (9), screw (10), and dust cap (11).

(5) Remove two guide pins (12) on rotating plate.

(6) Remove 12screws (13), lockwashers (14), and flat washers (15) from drive housing.

NOTE

Lift upper drive housing off lower drive housing and proceed with antenna pedestal disassembly.

(7) Remove six nuts (16), screws (17), flat washers (18), and rotating plate (19).

(8) Remove felt seal (20), antenna drive gear (21), grease seal (22), and bearing (23).

(9) Remove eight screws (24) and bearing retainer (25).

(10) Remove three screws (26), lockwashers (27), flat washers (28), and bearing cover (29).

(11) Remove packing (30) and plug (31).

(12) Remove packing (32) and two guide pins (33).

(13) Remove two screws (34), lockwashers (35), flat washers (36), and gear shaft support (37).

(14) Remove two guide pins (38).

(15) Remove bearing (39), washer (40), and spacer (41).

(16) Remove pin (42) and modified gear (43).

(17) Remove bearing (44) and two spacers (45 and 46).

(18) Remove pin (47), gear (48), and shaft (49).

(19) Remove screw (50), dust cap (51), lockwasher (52), and flat washer (53).

(20) Disconnect connector P20001 (54) from drive housing.

(21) Remove four screws (55), lockwashers (56), flat washers (57), and drive motor B20002 (58).

(22) Remove screw (59), bearing retainer (60), pin (61), and bearing (62).

(23) Remove gear spacer (63), key (64), and pinion gear (65).

(24) Remove pin (66) and data takeoff gear (67).

(25) Remove two laminated washers (68 and 69) and gear spacer (70).

(26) Remove three screws (71), lockwashers (72), and flat washers (73).

(27) Remove bearing retainer (74) and bearing (75).

(28) Remove six screws (76), lockwashers (77), and pinion shaft (78).

(29) Remove harmonic drive flexspine (70) and grease cartridge (80).

(30) Remove retainer ring (81) and harmonic drive wave generator (82).

(31) Remove key (83), six pins (84), harmonic drive circular spline (85), and packing (86).

(32) Remove four screws (87), lockwashers (88), flat washers (89), and pedestal support base (90).

(33) Remove packing (91) from pedestal support base.

(34) Remove two screws (92), lockwashers (93), flat washers (94), and scope mount assembly (95).

(35) Remove plug (96) from pedestal support base.

(36) Remove cable grip (97) and cable assembly W20001 from pedestal support base.

(37) Unsolder and remove connector P20002 (98) from cable assembly W20001 (101).

(38) Unsolder and remove connector J20003 (99) and dust cap (100) from cable assembly W20001 (101).

(39) Remove 13screws (102), lockwashers (103), flat washers (104), lower cover (105), and gasket (106).

(40) Remove two screws (107), lockwashers (108), flat washers (109), and clamps (110).

(41) Remove two screws (111), lockwashers (112), flat washers (113), and bracket (114).

(42) Tag and unsolder wires to capacitor C20002.

(43) Remove capacitorC20002 (115) from drive housing.

(44) Remove two screws (116), lockwashers (117), flat washers (118), and mounting block (119).

(45) Remove two screws (120), lockwashers (121), flat washers (122), and relay K20001 (123).

(46) Tag and unsolder wires to relay K20001.

(47) Unsolder and remove resistor R20001 (124).

(48) Tag and unsolder wires to two terminals (125).

(49) Remove two terminals (125) from drive housing.

(50) Tag and unsolder wires to capacitor C20001

(51) Remove two screws (126), lockwashers (127), flat washers (128), clamps (129), and capacitor C20001 (130).

(52) Remove four nuts (131), lockwashers (132), flat washers (133), washers (134), and screws (135).

(53) Tag and unsolder wires to connector J20004.

(54) Remove gasket (136) and connector J20004 (137).

(55) Remove four nuts (138), lockwashers (139), flat washers (140), washers (141), and screws (142).

(56) Tag and unsolder wires to connector J20001.

(57) Remove gasket (143) and connector J20001 (144).

(58)) Remove screw (145), lockwasher (146), flat washer (147), and terminal (148) from drive housing.

(59) Remove plug (149) from drive housing.

(60) Remove four screws (150), lockwashers (151), and flat washers (152).

(61) Remove synchro cover (153), gasket (154), and packing (155).

(62) Remove four clamps (156) from synchro.

(63) Remove clamp (157) and gear (158) from synchro shaft.

(64) Tag and disconnect five wired terminals (159) from synchro.

(65) Remove synchro B20001 (160) from antenna drive housing (161).

b. Assembly. To assemble Pedestal, Antenna AB-1158/GPA-119, proceed as follows:

(1) Using Pedestal, Antenna AB-1158/GPA-119, wiring diagram as guide (fig. FO7), connect five wired terminals (159) to synchro B20001 (160).

(2) Install clamp (157) and gear (158) on synchro shaft.

(3) Install synchro in antenna drive housing (161) using four clamps (156).

(4) Install synchro cover (153), gasket (154), and packing (155) using four screws (150), lockwashers (151), and flat washers (152).

(5) Install plug (149) in drive housing.

(6) Install terminal (148) using screw (145), lockwasher (146), and flat washer (147).

(7) Using Pedestal, Antenna AB-1158/GPA-119, wiring diagram as guide (fig. FO7), solder wires to connector J20001.

(8) Install connectorJ20001 (144) and gasket (143) using four nuts (138), lockwashers (139), flat washers (140), washers (141), and screws (142).

(9) Using Pedestal, Antenna AB-1158/GPA-119, wiring diagram as guide (fig. FO7), solder wires to connector J20004.

(10) Install connector J20004 (137) and gasket (136) using four nuts (131), lockwashers (132), flat washers (133), washers (134), and screws (135).

(11) Using Pedestal, Antenna AB-1158/GPA-119, wiring diagram as guide (fig. FO7), solder wires to capacitor C20001.

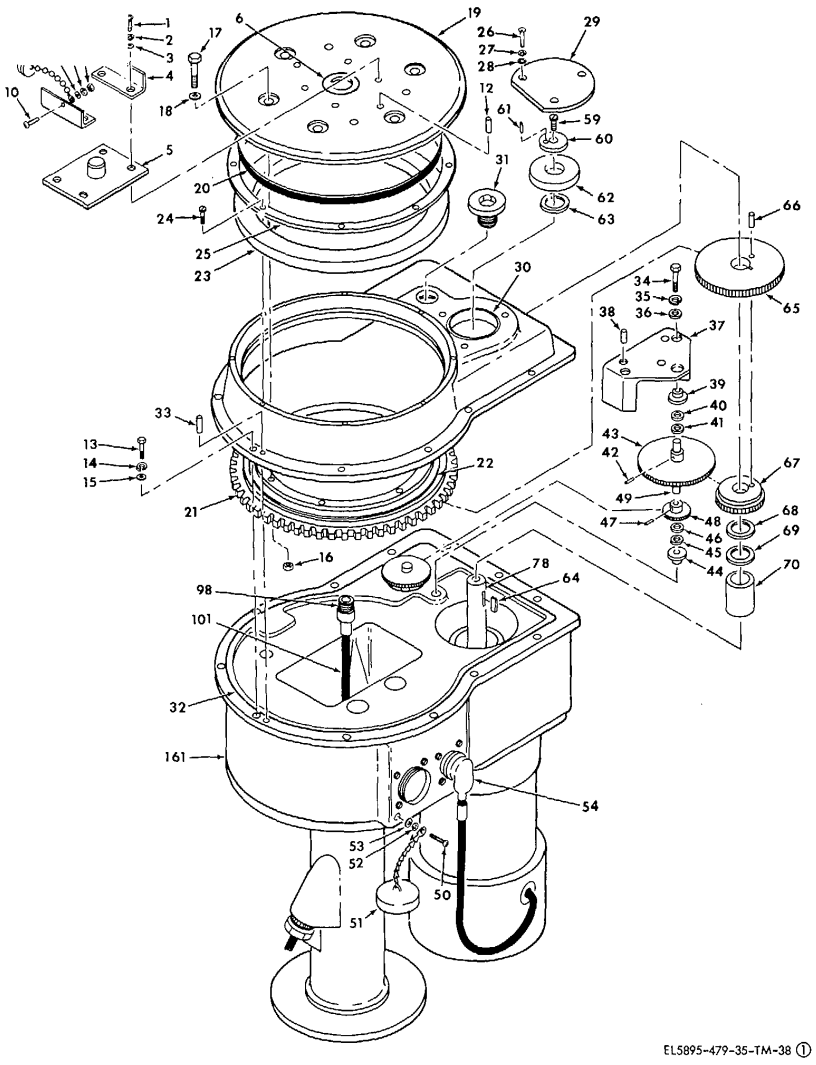
(12) Install capacitor C20001 (130) using two clamps (129), screws (126), lockwashers (127), and flat washers (128).

(13) Install two terminals (125) in drive housing.

(14) Install resistor R20001 (124) across two terminals (125).

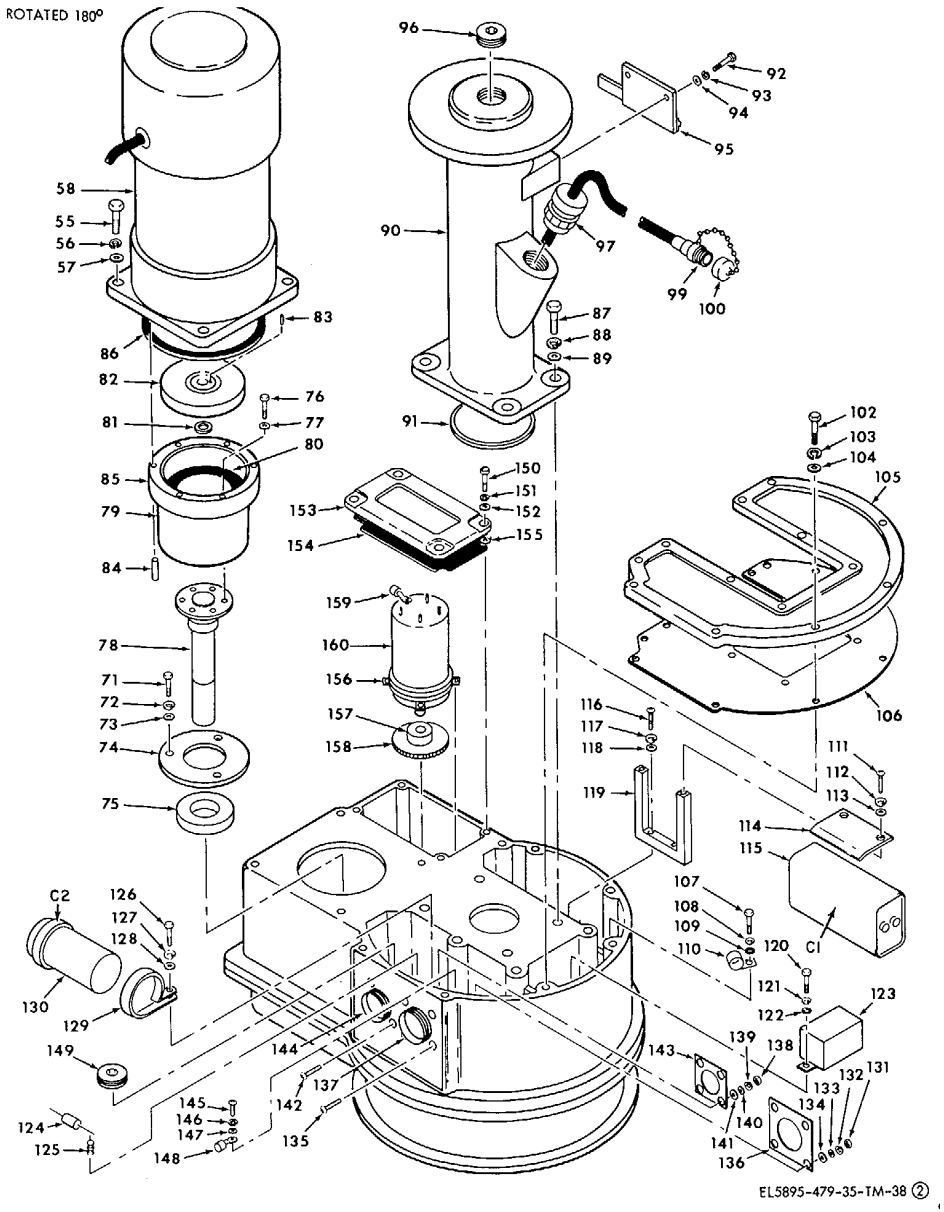
(15) Using Pedestal, Antenna AB-1158/GPA-119,wiring diagram as guide (fig. FO7), solder wires to two terminals (125) and relay K20001.

(16) Install relayK20001 (123) using two screws (120), lockwashers (121), and flat washers (122).



1 Screw (4)
2 Lockwasher (4)
3 Flat washer (4)
4 Protection angle (2)
5 Rotary joint
6 Packing
7 Nut
8 Lockwasher
9 Flat washer
10 Screw
11 Dust cap
12 Pin (2)
13 Screw (12)
14 Lockwasher (12)
15 Flat washer (12)
16 Nut (6)
17 Screw (6)
18 Flat washer (6)
19 Rotating plate
20 Felt seal
21 Drive gear
22 Grease seal
23 Bearing
24 Screw (8)
25 Bearing retainer
26 Screw (3)
27 Lockwasher (3)
28 Flat washer (3)
29 Bearing cover
30 Packing
31 Plug
32 Packing
33 Pin (2)
34 Screw (2)
35 Lockwasher (2)
36 Flat washer (2)
37 Gearshaft support
38 Pin (2)
39 Bearing
40 Washer
41 Spacer
42 Pin
43 Gear
44 Bearing
45 Spacer
46 Spacer
47 Pin
48 Gear
49 Shaft
50 Screw
51 Dust cap
52 Lockwasher
53 Flat washer
54 Connector P20001
55 Screw (4)
56 Lockwasher (4)
57 Flat washer (4)
58 Drive motor B20002
59 Screw
60 Bearing retainer
61 Pin
62 Bearing
63 Gear spacer
64 Key
65 Pinion gear
66 Pin
67 Data takeoff gear
68 Laminated washer
69 Laminated washer
70 Gear spacer
71 Screw (3)
72 Lockwasher (3)
73 Flat washer (3)
74 Bearing retainer
75 Bearing
76 Screw (6)
77 Lockwasher
78 Pinion shaft
79 Harmonic drive flexspline
80 Grease cartridge

Figure 5-1 (1). Pedestal, Antenna AB-1158/GPA-119, disassembly and parts location (sheet I of 2).



81 Retainer ring
82 Harmonic drive wave generator
83 Key
84 Pin (6)
85 Harmonic drive circular spline
86 Packing
87 Screw (4)
88 Lockwasher (4)
89 Flat washer (4)
90 Pedestal support base
91 Packing
92 Screw (2)
93 Lockwasher (2)
94 Flat washer (2)
95 Scope mount assembly
96 Plug
97 Cable grip
98 Connector P20002
99 Connector J20003
100 Dust cap
101 Cable assembly W20001
102 Screw (13)
103 Lockwasher (13)
104 Flat washer (13)
105 Lower cover
106 Gasket
107 Screw (2)
108 Lockwasher (2)
109 Flat washer (2)
110 Clamp (2)
111 Screw (2)
112 Lockwasher(~2)
113 Flat washer(2)
114 Bracket
115 Capacitor C20001
116 Screw (2)
117 Lockwasher (2)
118 Flat washer (2)
119 Mounting block
120 Screw (2)
121 Lockwasher (2)
122 Flat washer (2)
123 Relay K20001
124 Resistor R20001
125 Terminal (2)
126 Screw (2)
127 Lockwasher (2)
128 Flat washer (2)
129 Clamp (2)
130 Capacitor C20002
131 Nut (4)
132 Lockwasher (4)
133 Flat washer (4)
134 Washer (4)
135 Screw (4)
136 Gasket
137 Connector J20004
138 Nut (4)
139 Lockwasher (4)
140 Flat washer (4)
141 Washer (4)
142 Screw (4)
143 Gasket
144 Connector J20001
145 Screw
146 Lockwasher
147 Flat washer
148 Terminal
149 Plug
150 Screw (4)
151 Lockwasher (4)
152 Flat washer (4)
153 Synchro cover
154 Gasket
155 Packing(4)
156 Clamp (4)
157 Clamp
158 Gear
159 Terminal (5)
160 Synchro B20001
161 Drive housing

Figure 5-1 (2). Pedestal, Antenna AB-1158/GPA-119, disassembly and parts location (sheet 2 of 2).

(17) Install mounting block (119) using two screws (116), lockwashers (117), and flat washers (118).

(18) Using Pedestal, Antenna AB-1158/ GPA-119, wiring diagram as guide (fig.
FO), solder wires to capacitor C20002.

(19) Install capacitorC20002 (115) using bracket (114), two screws (111), lockwashers (112), and flat washers (113).

(20) Install two clamps (110) using two screws (107), lockwashers (108), and flat washers (109). Route pedestal wiring through clamps.

(21) Install lower cover (105) and gasket (106) using 13 screws (102), lockwashers (103), and flat washers (104).

(22) Assemble cable assembly W20001 (101) using cable grip (97), connector P20002 (98), connector J20003 (99), and dust cap (100).

(23) Install cable assembly W20001 in pedestal support base.

(24) Attach scope mount assembly (95) to pedestal support base using two screws (92), lockwashers (93), and flat washers (94).

(25) Install packing (91) and plug (96).

(26) Attach pedestal support base (90) to drive housing using four screws (87), lockwashers (88), and flat washers (89).

(27) Install harmonic drive circular spline (85) using six pins (84).

(28) Install packing (86) on drive motor.

(29) Install harmonic drive wave generator (82) on drive motor shaft using key (83) and retainer ring (81).

(30) Insert grease cartridge (80) in harmonic drive flexspline (79) and attach to pinion shaft (78) using six screws (76) and lockwashers (77). Torque screws to 180+10 inch-pounds.

(31) Install bearing (75) in drive housing using bearing retainer (74), three screws (71), lockwashers (72), and flat washers (73).

(32) Install gear spacer (70), two laminated washers (68 and 69), data takeoff gear (67), and pinion gear (65) on pinion shaft.
Use pin 66) and key (64).

(33) Install gear spacer (63), bearing (62), and bearing retainer (60) using pin (61) and screw (59).

(34) Attach drive motor B20002 (58) to drive housing using four screws (55), lockwashers (56), and flat washers (57).

(35) Connect connector P20001 (54) to connector J20001.

(36) Attach dust cap (51) to drive housing using screw (50), lockwasher (52), and flat washer (53).

(37) Install bearing (44), two spacers (45 and 46), gear (48), gear (43), spacer (41), washer (40), and bearing (39) on shaft (49).

(38) Position gears on shaft using two pins (42 and 47) insuring lower gear (48) engages synchro gear and upper gear (43) engages data takeoff gear.

(39) Attach gear shaft support (37) to drive housing using two pins (38), screws (34), lockwashers (35), and flat washers (36).

(40) Install packing (32) on lower drive housing.

(41) Install plug (31) and packing (30) on upper drive housing.

(42) Attach bearing cover (29) to upper drive housing using three screws (26), lockwashers (27), and flat washers (28).

(43) Install grease seal (22) on drive gear (21).

(44) Install bearing retainer (25) using eight screws (24).

(45) Install felt seal (20) on rotating plate (19).

(46) Position bearing (23) on drive gear.

(47) Install rotating plate and drive gear using six nuts (16), screws (17), and flat washers (18).

(48) Install packing (6), rotary joint (5), and two protection angles (4) using four screws (1), lockwashers (2), and flat washers (3).

(49) Attach dustcap (11) to protection angle using nut (7), lockwasher (8), flat washer (9), and screw (10).

(50) Install two guide pins (12) on rotating plate.

(51) Connect connectorP20002 of cable assembly W20001 to rotary joint.

(52) Position upper drive housing on lower drive housing using two guide pins (33).

(53) Use 12screws (13), lockwashers (14), and flat washers (15) to complete antenna pedestal assembly.

CHAPTER 6

GENERAL SUPPORT TESTING

6-1. Introduction

This chapter covers general support testing of the major components that comprise Interrogator Set AN/TPX-41. These tests should be performed to evaluate equipment performance after completion of repair and adjustment operations. The tools, test equipment, and test fixtures required to perform these tests consist of those allocated to general support maintenance as indicated in maintenance allocation chart (MAC) contained in TM 11-5895-479-12. Each test in this chapter is preceded by a list of test equipment and materials required to perform the test, equipment conditions that are a prerequisite to accomplishing the test, references to test connection diagrams as applicable, and any special instructions required to perform the test. Instructions for connecting and operating the test equipment required for each test are contained in the respective test procedures. Perform the tests in the order presented and follow the procedural steps in each test in the order given.

6-2. General Support Test Procedures

The major components of the AN/TPX-41 are listed in *a* through j below with references to the paragraphs covering general support testing of each.

a. Blanker, Interference MX-8795/TPX-41 (paras 6-3 through 6-11).

b. Coder-Control KY-97C/TPX (para 6-12).

c. Control, Remote Switching C-1271A/ TPX-22 (para 6-13).

d. Modulator, Pulse MD-638/TPX-41 paras 6-14 through 6-17).

e. Receiver-Transmitter Radio RT-264D/ UPX-6 (para 6-18).

f. Antenna Group AN/GPA-119 (para 6-19 through 6-21).

g. Decoder, Video KY-593/TPX-44 (para 6-22).

h. Control, Remote Switching C-7014/TPX-44 (para 6-23).

i. Simulator, Radar Signal SM-472/TPX-44 (para 6-24).

j. Interconnecting Box J-2945/TPX-41 (para 6-25).

6-3. Blanker, Interference MX-8795/TPX-41, Physical Tests and Inspection

a. Test Equipment and Materials Required.

Light Assembly, Electric, MX-1292/PAQ.

b. Test Connections and Conditions.

(1) Disconnect all external cables.

(2) Remove MX-8795/TPX-41 from dust cover and place on suitable work surface.

(3) Connect MX-1292/PAQ to 117-volt 60-Hz power source and install wide-band transmission filter.

Step no.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	None	-	*a.* Operate front panel switches.	a. Switches should operate in normal manner.
			b. Inspect front panel lamps for completeness.	*b.* Lamps should be complete.
			c. Inspect front panel lamps and switches for evidence of looseness.	c. Lamps and switches should be securely mounted.
			d. Inspect connectors through J31109 for evidence of damage or looseness.	J31101 *d.* Connectors should be physically undamaged and securely mounted to chassis.
			e. Inspect wiring for condition of insulation.	e. Insulation should be free from cracks or fraying.
			f: Inspect metal surfaces for condition of finish and panel markings.	*f* All metal surfaces intended to be painted must not show bare metal. Panel markings should be legible.
			Note: Touchup painting is recommended in lieu of refinushing whenever practicable.	
2	*MX-1292/PAQ 245V* for M.V. lamps: ON	*MX-8795/TPX-41*	*a.* On MX-8795/TPX-41, expose chassis and each plug-in circuit card to direct rays of MX-1292/ PAQ. Inspect components, wiring, and chassis surfaces for evidence of a polyurethane coating. Inspect connector, switch contacts, and jacks for absence of a polyurethane coating.	*a.* All components, wiring, and chassis surfaces should be completely covered with a polyurethane coating. There should be no evidence of polyurethane or connectors and switch contacts.
			Note: Polyurethane coating glows grayish-blue when exposed to rays of MX-1292/PAQ.	*Note:* Do not apply polyurethane coating to parts not originally finished with polyurethane.
			b. On MX-1292/PAQ, turn off ac power and disconnect.	b. None.

6-4. Blanker, Interference MX-8795/TPX-41, Positive Power Supply Regulation Test

a Test Equipment and Materials Required.

(1) Electronic VoltmeterME-202/U.

(2) Voltmeter M-30/U.

(3) Transformer, Variable, Power CN-16B/U.

(4) Blanker, Interference MX-8795/TPX-41, test fixture TF181530, (fig. FO-16).

b. Test Conditions and Connections (fig. 6-1). Connect Transformer, Variable, Power CN-16B/U to 117-volt 60-Hz power source. Connect OUTPUT of CN-16B/U to connector P2 of TF181530.

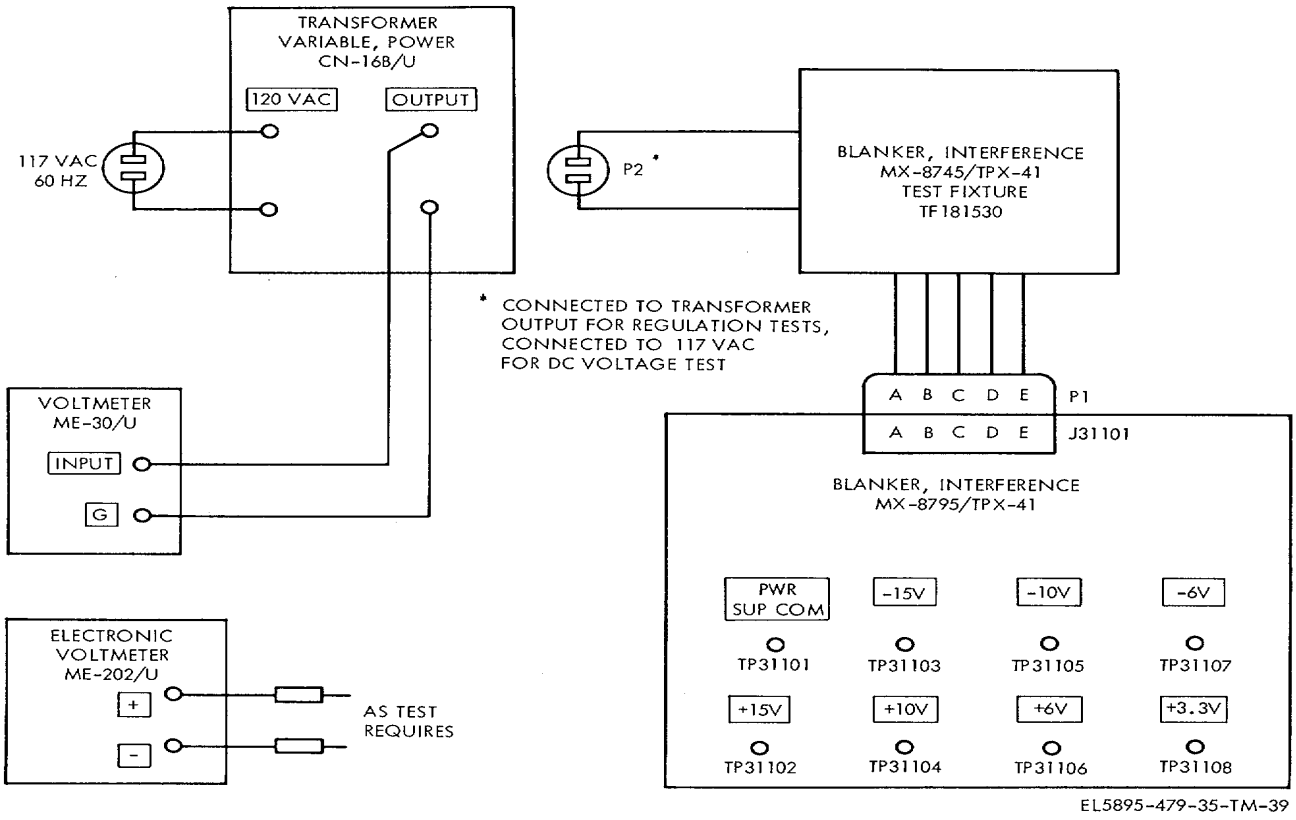


Figure 6-1. Blanker, Interference MX-8795/TPX-41, power supply regulation and dc voltage test connections.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	ME-30/U POWER: ON Selector: 300 VOLTS	MX-8795/TPX-41 POWER: ON	a. On ME-30/U, connect INPUT test lead to one OUTPUT terminal on CN-16B/U and connect G test lead to other OUTPUT terminal on CN-16B/U.	a. None.
	TF 181530 117 VAC: ON		b. On CN-16B/U, adjust for 117 ac as indicated on ME-30/U.	b. None
2	As last indicated, except: ME-202/U POWER: ON		a. On ME-202/U, connect a fabricated test lead between negative (-) terminal and PWR SUP COM testpoint TP31101, and a second fabricated test lead between positive (+) terminal and +15V testpoint TP31102 on MX-8795/TPX-41 (fig. 6-1).	a. None

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	OPERATE-CALIBRATE: OPERATE RANGE: DC 50 NULL: .1 NULL: .1 B: 5 C: 0 D:0 E: 0		b. On MX-8795/TPX-41, adjust +15V ADJ control R31101 until +15V is indicated on ME-202/U. c. On CN-16B/U, adjust for 125 vac as indicated on ME-30/U. d. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches. e. On CN-16B/U, adjust for 105 vac as indicated on ME-30/U. f. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches. g. On CN-16B/U, adjust for 117 vac as indicated on ME-30/U. h. Disconnect ME-202/U and ME-30/U.	b. None c. None. d. +14.95min,+15.05max. e. None. f. +14.95 min, +15.05 max. g. None h. None
3	As last indicated, except: ME-30U Selector: .001 VOLTS .001		a. On ME-30/U, connect a fabricated test lead between G and PWR SUP COM test-point TP31101, and a second fabricated lead to +15V test-point TP31102 on MX-8795/TPX-41. b. On ME-30/U, observe ripple voltage.	a. None b. 0.5 mv rms max.
	ALL TEST EQUIPMENT: POWER: OFF	As last indicated, except: MX-8795/TPX-41 POWER: OFF	c. Disconnect all test equipment.	c. None.

6-5. Blanker, Interference MX-8795/ TPX-41, Negative Power Supply Regulation Test

a. Test Equipment and Materials Required.

(1) Electronic Voltmeter ME-202/U.

(2) Voltmeter ME-30/U.

(3) Transformer, Variable, PowerCN-16B/U.

(4) Blanker, Interference MX 8795/TPX-41, test fixture TF181530, (fig. FO-17).

b. Test Conditions and Connections (fig. 6-1). Connect Transformer, Variable, to 117 volt Power CN-16B/U 60-Hz power source. Connect the output of CN-16B/U to connector P2 of TF181530.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	ME-30/U POWER: ON Selector: 300 VOLTS	MX-8795/TPX-41 POWER: ON	a. On ME-30/U, connect INPUT test lead to one OUTPUT terminal of CN-16B/U and connect G test lead to other OUTPUT terminal of CN-16B/U.	a. None
			b. On CN-16B/U, adjust for 117 vac as indicated on ME-30/U.	b. None
2	As last indicated, except: ME-202/U POWER: ON OPERATE-CALIBRATE: OPECALIBRATE: RANGE: DC 50 NULL:.1 A: 1 B: 5 C: 0 D: 0 E: 0	As last indicated	a. On ME-202/U, connect fabricated test lead between positive (+) terminal and PWR SUP COM test point TP31101, and second fabricated test lead between negative (-) terminal and -15V testpoint TP31103 on MX-8795/TPX-41 (fig. 6-1).	a. None
			b. On MX-8795/TPX-41, adjust -15V ADJ control R31102 for -15 as indicated on ME-202/U.	b. None
			c. On CN-16B/U, adjust for 125 vac as indicated on ME-30/U.	c. None
			d. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches.	d. -14.95 min, -15.05 max.
			e. On CN-16B/U, adjust for 105 vac as indicated on ME-30/U.	e. None
			f. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage on switches.	f. -14.95 min, -15.05 max.
			g. On CN-16B/U, adjust for 117 vac as indicated on ME-30/U.	g. None
			h. Disconnect ME-202/U and ME-30/U.	h. None
3	As last indicated, except: ME—30/U Selector: .001 VOLTS		a. On ME-30/U, connect a fabricated test lead between G and PWR SUP COM'test point TP31101, and a second fabricated lead to -15V test point TP31103 on MX-8795/TPX-41.	a. None
			b. On ME-30/U, observe ripple voltage.	b. 0.5 mv rms max

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	ALL TEST EQUIPMENT POWER: OFF POWER: OFF	As last indicated, except: MX--8795/TPX-41	c. Disconnect all test equipment	c. None

6-6. Blanker, Interference MX-8795/ TPX-41, DC Voltage Test

a. Test Equipment and Materials

(1) Differential Voltmeter ME-202/U

(2) Blanker, Interference MX-8795/TPX-41, test fixture TF 181530, (fig. FO-16)

b. Test Conditions and Connections (fig. 6-1). Connect Transformer to 117-volt, Variable, Power CN-16B/U, 60-Hz power source. Connect connector P2 of F181530 to 117-volt, 60-Hz power source.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	ME-202/U POWER: ON OPERATE-CALIBRATE OPERATE RANGE: DC 50 NULL:.1 A: 1 B: 5 C: 0 D: 0 E: 0 indicated on ME-202/U.	MX-8795/TPX-41 POWER: ON	a. On ME-202/U, connect fabricated test lead between negative (-) terminal and PWR SUP COM test point TP31101, and second fabricated test lead between positive (+) terminal and +15V test point TP31102 (fig. 6-1). b. On MX-8795/TPX-41, adjust +15V ADJ control R31101 until +15v is	a. None b. +15 +0.05v
2	As last indicated, except: A: 1 B: 0 C: 0 D:0 E: 0	As last indicated ------	a. On ME-202/U, remove positive (+) fabricated test lead from +15V test point TP31102 and connect to +10OV test point TP31104. b. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches.	a. None. b. +9.45vmin,+10.55vmax.
3	As last indicated except: A: 0 B: 5 C: 0 D: 0 E: 0	As last indicated .-----	a. On ME-202/U, remove positive (+) fabricated test lead from +10V test point TP31104 and connect to +6V test point TP31106. b. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches.	a. None b. +5.86vmin,+6.54vmax.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
4	As last indicated, except: A: 0 B: 0 C: 0 E: 0	As last indicated-----	a. On ME-202/U, remove positive (+) fabricated test lead from +6V test point TP31106 and connect to +3.3V test point TP31108. b. On ME-202/U, set RANGE to 5, and adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for switches.	a. None b. +3.12v min, +3.48v max.
5	As last indicated, except: A: 1 B: 5 C: 0 D: 0 E: 0	As last indicated-----	a. On ME-202/U, remove positive (+) fabricated test lead from +3.3V test point TP31108 and connect to PWR SUP COM test point TP31101. b. On ME-202/U, remove negative (-) fabricated test lead from PWR SUP COM test point TP31101 and connect to -15V test point TP31103. c. On MX-7280/TPX, adjust -15V ADJ control R31102 for -15v as indicated on ME-202/U.	a. None. b. None. c. -15 +0.05v.
6	As last indicated, except: A: 1 B: 0 C: 0 D: 0	As last indicated.------	a. On ME-202/U, remove negative (-) fabricated test lead from -15V test point TP31003 and connect to -10V test point TP31105. b. On ME-202/U,adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for all switch positions.	a. None b. -9.45v min, -10.55v max.
7	As last indicated, except: RANGE: 50 A: 0 B: 0 C: 0 D: 0 E: 0	As last indicated -----	a. ON ME-202/U, remove negative (-) fabricated test lead from -10V test point TP31105 and connect to -6V test point TP31107. b. On ME-202/U, adjust switches A, B, C, D, and E for a null on meter. Observe indicated voltage for all switch positions.	a. None. b. -5.86v min.
	ALL TEST EQUIPMENT POWER: OFF POWER: OFF	As last indicated, except: MX-8795/TPX-41	Disconnect all test equipment	None.

6-7. Blanker, Interference MX-8795/ TPX-41, Trigger Test

a. Test Equipment and Materials Required.

(1) Oscilloscope AN/USM-140B.

(2) Time Delay Generator MX-2962/USM.

(3) Digital Readout, Electronic Counter AN/USM-207.

(4) Signal Generator SG-299/U.

(5) Resistor, 510-ohm, 2-watt.

(6) Resistor, 2K, 2-watt (2 required).

(7) Blanker, Interference MX-8795/TPX-41, test fixture TF181530.

(8) Connector, Adapter UG-274B/U (2 required).

b. Test Conditions and Connections (fig. 6-2). Connect all test equipment as shown in figure 6-2.

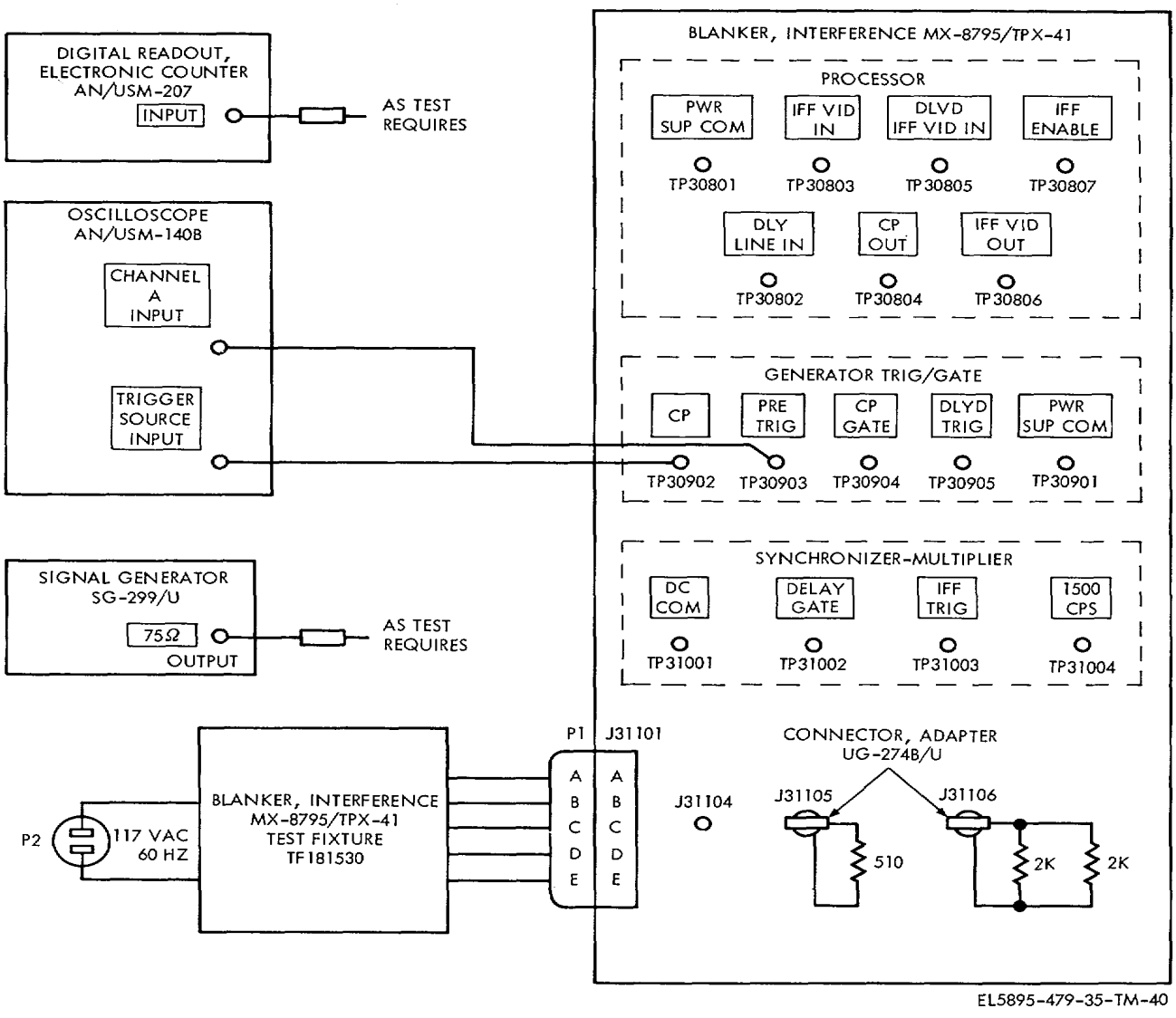


Figure 6-2. Blanker, Interference MX-8795/TPX-41, trigger test connections.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/USM-140B POWER:ON ASTIGMATISM: misposition FOCUS: mid-position INTENSITY: SCALE LIGHT: fully cw CHANNEL A VER- CHANNEL A VER-TICAL Position: midposition HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY: IN-TERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: (MICRO-SECONDS/CM): 1 VERNIER: CAL TRIGGER SLOPE: as desired TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT DC CHANNEL A-CHANNEL B: CHANNEL A CHANNEL A SEN-SITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED CHANNEL A AC-DC: DC Remaining controls may be in any position. TF181530 117 VAC: ON	MX-8795/TPX-41 POWER: ON PRF SEL SWITCH S3: 2	a. On AN/USM-140B, connect CHANNEL A INPUT test lead to PRE TRIG test point TP30903 on trigger/gate gen-erator subassembly. b. On trigger/gate generator sub-assembly, adjust PW ADJ control R30907 for a positive pulse duration as indicated AN/USM-140B.	a. None. b. 0.4 μsec.
2	As last indicated except: AN/USM-140B SWEEP TIME:NDS/ MILLISECONDS/ CM): .5	As last indicated-----	a. On AN/USM-140B, remove CHANNEL A INPUT from PRE TRIG test point TP30903 and connect to IFF ENABLE test point TP30807 on processor subassembly.	a. None

Step	Control settings			

No.	Test equipment	Equipment under test	Test procedure	Performance standard
			b. On trigger/gate generator sub-assembly, adjust IFF GATE control R30920 for a correct negative gate duration.	b. 2600 μsec.
			c. On AN/USM-140B, remove CHANNEL A INPUT from IFF ENABLE test point TP30807 and connect to CP GATE testpoint TP30904 on trigger/gate generator subassembly.	c. None.
			d. On trigger/gate generator sub-assembly, adjust CP GATE control R30936 for a correct positive gate duration.	d. 3000 μsec.
			e. On AN/USM-140B, remove CHANNEL A INPUT from CP GATE test point TP30904 and connect -to DLYD TRIG testpoint TP30905 on trigger/gate generator subassembly.	e. None.
3	As last indicated, except: AN/USM—140B SWEEP TIME: (MICROSECONDS CM): 10	As last indicated ------- TP30905.	On trigger/gate generator sub-assembly, adjust DELAY ADJ control R30942 for correct pulse delay. After adjustment, remove AN/USM-140B, CHANNEL A INPUT from DLYD TRIG test point	90 μsec.
4	SG-299/U POWER: ON 75Ω ATTEN: 0 DB OUTPUT AMPLITUDE (75Ω): 0 RANGE: X1K FREQUENCY: 1.5 AN/USM-207 POWER: TRACK FUNCTION: FREQ GATE TIME: 10-1		a. On SG-299/U, install Adapter UG-274B/U on 75Ω output connector.	a. None.
			b. On AN/USM-140B, connect CHANNEL A INPUT to one side of adapter installed in a above	b. None.
			c. On AN/USM-207, connect INPUT to one side of adapter installed in a above.	c. None
			d. On SG-299/U, adjust OUTPUT AMPLITUDE control for a 4v pp signal as indicated on AN/USM-140B.	d. None
			e. On SG-299/U, adjust FREQUENCY control for an indication of 1500 +8 Hz as indicated on AN/USM-207.	e. None
5	As last indicated except: AN/USM-140B SWEEP TIME: (MILLISECONDS/ CM): .2		a. On AN/USM-140B, remove CHANNEL A INPUT from 75Ω output of SG-299/U and connect to 1500 CPS test point TP31004 on synchronizer-multiplier subassembly.	a. 1500 Hz sine wave is present.

Step	Control settings	Equipment under		

No.	Test equipment	test		Test procedure		Performance standard
			b.	On synchronizer-multiplier subassembly, turn LEVEL control R3 1037 counterclockwise one-quarter turn past the point where oscillations cease.	b.	None.
			c.	On AN/USM-207, remove INPUT connection and connect to pin V of connector J31109 (accessible from bottom of MX-8795/TPX-41 chassis) and on the synchronizer-multiplier subassembly, connect a jumper between test points TP31001 and TP31002.	c.	None.
			d.	On synchronizer-multiplier subassembly, adjust FREQ control R31024 for max. amplitude of 1500-Hz sine wave. If clipping occurs during adjustment of R31024, readjust OUTPUT AMPLITUDE (75Ω) on SG-299/U to eliminate clipping. Continue adjustment of R31024.	d.	None.
			e.	On SG-299/U adjust OUTPUT AMPLITUDE (75Q) control R31037 for small amount of clipping of the 1500 Hz sinewave.	e.	None.
	As last indicated-----	As last indicated-----	f.	On synchronizer-multiplier subassembly, adjust BAL control R31039 for symmetrical clipping of the 1500-Hz sine wave.	f.	None.
			g.	On AN/USM-140B, temporarily remove CHANNEL A INPUT from 1500 CPS test point TP31004 and connect to one side of adapter at 75Ω output connector of SG-299/U.	g.	None.
			h.	On SG-299/U, adjust OUTPUT AMPLITUDE (75Ω) for 5.5v pp indication on AN/USM-140B.	h.	None.
			i.	On AN/USM-140B, reconnect CHANNEL A INPUT to 1500 CPS test point TP31004 on synchronizer-multiplier subassembly.	i.	1500-Hz sine wave is present.
			j.	On synchronizer-multiplier subassembly, adjust LEVEL control R31037 for max amplitude of sine wave with no clipping.	j.	1500-Hz sine wave amplitude is 20v pp.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
6	As last indicated except: SG-299/ U POWER: OFF	As last indicated	Disconnect SG-299 /U	None
7	As last indicated	As last indicated	Remove jumper connected in 5 c above and on AN / USM-140B. remove A INPUT from 1500 CPS testpoint TP31004 and connect to DELAY GATE testpoint TP31002 on the synchronizer-multiplier subassembly.	A square wave similar to that shown in M of fig. 3-2 is present.
8	As last indicated	As last indicated	a. On AN / USM-207, connect INPUT to IFF trigger connector J31105 on MX-8795/ TPX-41.	a. None
			b. On AN / USM-207observe digital readout.	b. 299.9 pps min. 300.2 pps max.
			b.1 On MX-8795/TPX-41. set PRF SEL switch S3 to position 1 and observe digital readout on AN/USM-207.	b.1 374.9 pps min, 375.1 ppps max.
			b.2 On MX-8795/TPX-41, set PRF SEL switch S3 to position 3 and observe digital readout on AN/USM-207.	b. 2 249.9 pps min. 250.1 pps max.
			b.3 On MX-8795 / TPX-41, return PRF SEL switch to position 2.	b. 3 None.
			c. Disconnect AN / USM-207	c. None.
9	As last indicated except: AN/ USM-140B SWEEP TIME: (MICROSECONDS / CM): I TRIGGER SOURCE: INT	As last indicated pulse	a. On AN/USM-140B, remove CHANNEL A INPUT from Delay GATE testpoint TP31002 and connect to IFF trigger connector J31105 on MX-8795 / TPX-41.	a. None.
			b. On AN/USM-140B, observe characteristics of positive max. Rise Time: 0.1 /µsec max.	b. Amplitude: 12v peak min Duration: 0.5 1sec min, 4 ,sec
			c. On AN/USM-140B, remove CHANNEL A INPUT from IFF trigger connector J31105 and connect to display trigger connector J31106 on MX-8795 / TPX-41.	c. None.
			d. On AN/USM-140B. observe characteristics of positive pulse	d. Amplitude: 2.5v peak min. Duration: 0.3 µsec min, 0.7 µsec max. Rise Time: 0.1 µsec max.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
10	As last indicated, except: AN/USM-140B SWEEP TIME: (MICRO-SECONDS/ CM): 5 TRIGGER SOURCE: EXT DC	As last indicated-----	a. On US M/ 14 0 B, remove CHANNEL A input from display trigger connector J31106 and connect to DLYD TRIG test point TP30905 on trigger/gate generator subassembly. b. On trigger/gate generator subassembly, adjust DELAY ADJ control R30942 from fully ccw to fully cw while observing pulse at DLYD TRIG test point TP30905 on AN/USM-140B. c. On trigger/gate generator subassembly, adjust DELAY ADJ control R30942 for correct pulse delay	a. None. b. Pulse delay may be varied from 70μsec to 110 μsec. c. 90μsec. Note: Final adjustment must be made during alignment with associated radar set.
11	As last indicated, except: ALL TEST EQUIPMENT POWER: OFF	As last indicated, except: MX-8795/TPX-41 POWER :OFF	Disconnect all test equipment and restore MX-8795/TPX-41 to service.	None.

6-8. Blanker, Interference MX-8795/ TPX-41, Trigger/Gate Generator Test

a. Test Equipment and Materials.

(1) Pulse Generator Set AN/UPM-15.

(2) Oscilloscope AN/USM-140B.

(3) Time Delay Generator MX-2692/USM.

(4) Connector, Adapter UG-274B/U.

(5) Trigger/Gate Generator Test Fixture TF125601.

b. Dc Power Requirements. The dc power requirements listed in the chart below are required to perform the Blanker, Interference MX-8795/TPX-41, trigger gate generator test.

Note

If available test equipment will not supply the power requirements listed in the following chart, a bench test power supply may be locally fabricated in accordance with figure FO-23 to provide the necessary voltages.

Voltage	Current (ma)	Regulation	Maximum rms ripple (mv)
+10v	2	+5%	100
+6v	11	+5%	100
-6v	2	-5%	100
+3.3v	3	+5%	100

c. Test Conditions and Connections (fig. 6-3). Connect all test equipment as shown in figure 6-3.

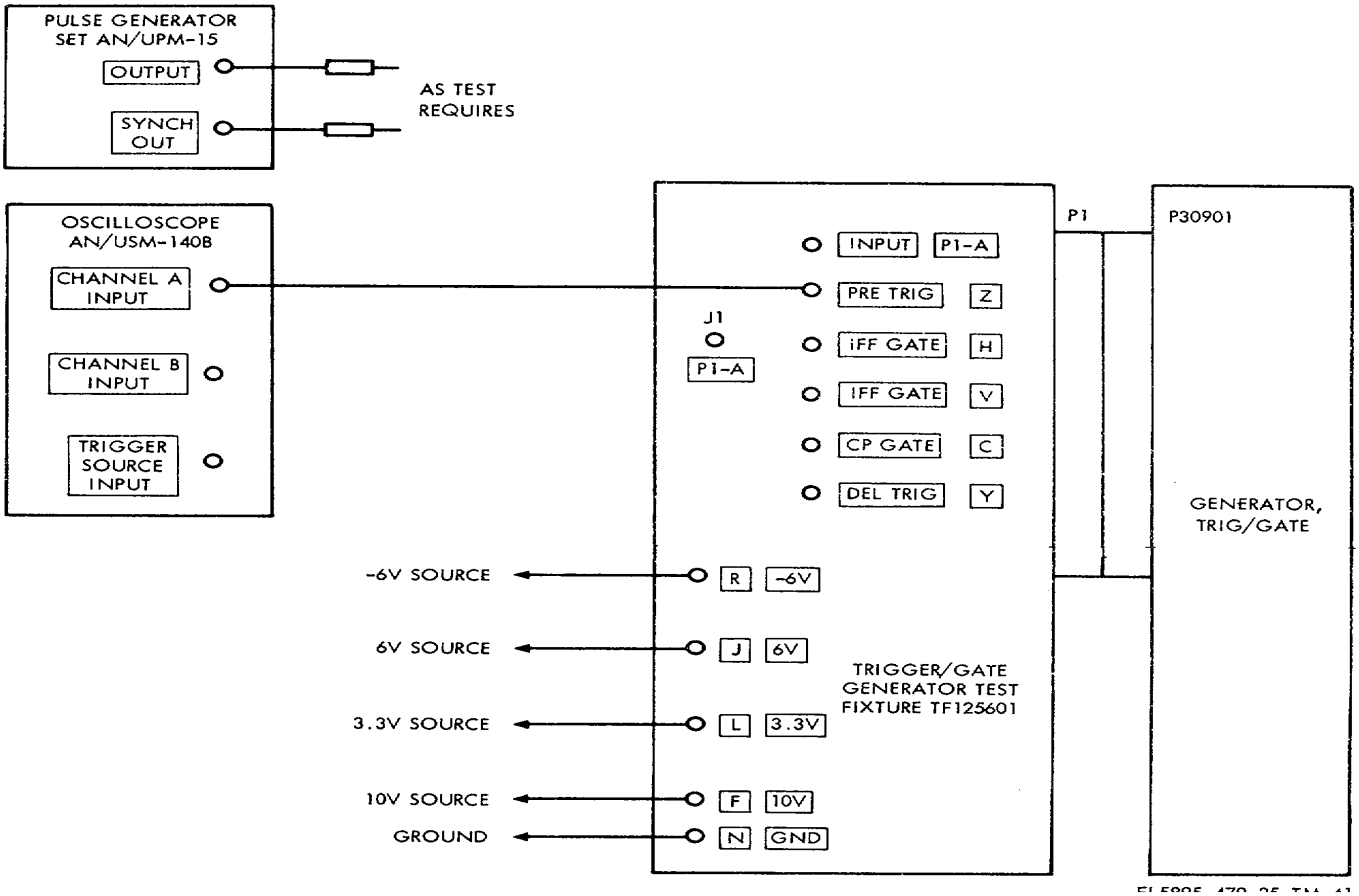


Figure 6-3. Blanker, Interference MX--8795/TPX-41, trigger/gate generator test connections.

c. Procedures.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/USM-140B POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALE LIGHT: fully cw CHANNEL A VERTICAL POSITION: midposition	MX-8795/TPX-41 POWER: ON	a. On AN/USM-140B, connect CHANNEL A INPUT to PRE TRIG test point Z on TF125601. b. On AN/USM-140B, observe interpulse period.	a. None. b. Greater than 4050 usec.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY INTERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: (MILLISECONDS/CM): 5 VERNIER: CAL TRIGGER SLOPE: as desired. TRIGGER LEVEL: as desired. SWEEP MODE: PRESET TRIGGER SOURCE: INT CHANNEL A-CHANNEL B: CHANNEL A CHANNEL A SENSITIVITY: (VOLTS/CM): 1 VERNIER: CALIBRATED CHANNEL A AC-DC: DC Remaining controls may be in any position. TF 125601 10V, 3.3V: ON +6V, -6V: ON			
2	As last indicated, except: AN/UPM-15 POWER: ON SYNC selector knob: INT B BIAS: midposition PULSE RATE: 300 pps SYNC switch: LEAD DELAY switch: SHORT DELAY dial: minimum. SEPARATION: midposition WIDTH switch: NAR WIDTH dial: .5μsec PULSE NO. 2: OUT POLARITY: POS COARSE ATTN knob: 1 FINE ATTN dial: 3 RISE TIME: min	As last indicated	a. On AN/UPM-15, connect OUTPUT to connector J1(P1-A) on TF125601, and SYNC OUT to TRIGGER SOURCE INPUT on AN/USM-140B. b. On AN/USM-140B, remove CHANNEL A INPUT from PRE TRIG test point Z on TF25601 and connect to INPUT test point A on TF125601. c. On AN/UPM-15, adjust WIDTH, COARSE ATTN, and FINE ATTN controls for a 300-pps positive 3v peak, 0.5-μ sec duration pulse as indicated on AN/USM-140B.	a. None. b. None. c. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	AN/USM--140B SWEEP TIME: (MICROSECONDS/ CM: 1 TRIGGER SOURCE: EXT AC			
3	As last indicated--------	As last indicated---------	a. On AN/USM-140B, remove CHANNEL A INPUT from INPUT test point A and connect to PRE TRIG test point Z on TF125601.	a. None.
			b. On trigger/gate generator subassembly adjust PW ADJ control R30907 for 0.5 usec duration of pulse observed on AN/USM-140B.	b. Pulse is adjustable to 0.5/sec duration and is synchronized with pulse at INPUT test point A on TF125601.
4	As last indicated, except: AN/USM-140B CHANNEL A-CHANNEL B: CHANNEL B: ALTERNATE CHANNEL B SENSIVITY VOLTS/CM): 1 VERNIER: CALIBRATED CHANNEL B AC-DC: DC CHANNEL B VERTICAL POSITION: midposition SWEEP TIME: (MICROSECONDS/ CM): 5	As last indicated .-----	a. On AN/USM-140B, connect CHANNEL B INPUT to TNPUT test point A on TF125601.	a. None.
			b. On AN/USM-140B, remove CHANNEL A INPUT from PRE TRIG test point Z and connect to DEL TRIG test point Y on TF125601.	b. None.
			c. On trigger/gate generator subassembly, adjust DELAY ADJ control R30942 from fully ccw to fully cw	c. On AN/USM-140B, at CHANNEL A INPUT observe that delay of positive pulse is adjustable between 70ousec min and 110 usec max.
			d. On trigger/gate generator subassembly, rotate DELAY ADJ control R30942 to delay positive pulse 90usec NEL B INPUT.	d. On AN/USM-140B, observe that positive pulse at CHANNEL A INPUT is delayed 90,μsec from pulse on CHAN-
			e. On AN/USM-140B, at CHANNEL A INPUT, observe amplitude of positive pulse at DEL TRIG testpoint on TF125601.	e. 2v peak min.
5	As last indicated, except: AN/USM-140B SWEEP TIME: (MILLISECONDS/ CM): 2 CHANNEL A (VOLTS/CM): 2	As last indicated-------	a. On AN/USM-140B, remove CHANNEL A INPUT from DEL TRIG test point Y and connect to CP GATE test point C on TF125601.	a. None.
			b. On trigger/gate generator subassembly, adjust CP GATE control R30936	b. On AN/USM-140B, at CHANNEL A INPUT, observe 2550 usec pos gate.
			c. On AN/USM-140B, observe : positive gate amplitude.	c. 2v peak min.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
6	As last indicated, except: AN/ USM-140B SWEEP TIME: (MICROSECONDS /CM): 1	As last indicated	On AN/USM-140B, observe delay of leading edge of positive gate at CP GATE testpoint C from pulse at INPUT testpoint A on TF125601.	1.3 μsec min 3.0 μsec max.
7	As last indicated, except: AN/ USM-140B SWEEP TIME: (MILLISECONDS / CM): .2	As last indicated	a. On AN / USM-140B, remove CHANNEL A INPUT from CP GATE testpoint C and connect to IFF GATE testpoint H on TF125601. b. On trigger / gate generator subassembly, adjust IFF GATE control R30920. c. On AN / USM-140B, observe amplitude of negative gate.	a. None. b. 2600 μsec negative gate. c. 2v peak min.
8	As last indicated, except: AN/ USM-140B SWEEP' TIME: MICROSECONDS/ /CM: 1	As last indicated	On AN/USM-140B, observe delay of leading edge of negative gate at IFF GATE testpoint H from pulse at INPUT testpoint A on TF125601.	1.3 μsec min, 3 μsec max (at 50% amplitude point).
9	As last indicated, except: AN/USM-140B SWEEP TIME: MILLISECONDS/ CM: .2	As last indicated	On AN/USM-140B, remove CHANNEL B INPUT from INPUT testpoint A and connect to IFF GATE testpoint V on TF125601.	Negative gate at IFF GATE testpoint V similar to negative gate at IFF GATE testpoint H.
9.1	As indicated for step 2 above, except on AN / UPM-15, set PULSE RATE for 37-5 pps	As last indicated	Make initial test connections as shown in figure 6-3 and repeat steps 2 through 9 above, substituting 375 pps wherever 300 pps appears in step 2.	Steps 2 through 9 above.
9.2	As indicated for step 2 above, except on AN / UPM-15, set PULSE RATE for 250 pps	As last indicated	Make initial test connections as shown in figure 6-3 and repeat steps 2 through 9 above, substituting 250 pps wherever 300 pps appears in step 2.	Steps 2 through 9 above.
10	As last indicated, except: ALL TEST EQUIPMENT POWER: OFF		Disconnect all test equipment and restore trigger / gate generator subassembly to service.	None.

6-9. Blanker, Interference MX-8795 / TPX-41, Synchronizer-Multiplier Test

a. Test Equipment and Materials.

(1) Oscilloscope AN / USM-140B.
(2) Time Delay Generator MX-2962/USM.
(3) Digital Readout, Electronic Counter AN / USM-207.
(4) Signal Generator SG-299 / U.
(5) Pulse Generator AN/UPM-15.
(6) Synchronizer-Multiplier Test Fixture TF170114.
(7) Connector Adapter US-274B / U.

b. Dc Power Requirements. The dc power requirements listed in the chart below are required to perform the Blanker, Interference MX8795 / TPX-41, synchronizer-multiplier test.

NOTE

If available test equipment will not supply the power requirements listed in the following chart, a bench test power supply may be locally fabricated in accordance with figure FO-23 to provide the necessary voltages.

Voltage	Current (ma)	Regulation	Maximum rms ripple (mv)
+15v	2.4	+5%	10
-15v	2.4	+5%	10

c. Test Conditions and Connections)fig. 6-4). Connect all test equipment as shown in figure 6-4.

d. Procedures.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/USM-140B POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALES LIGHT: Fully cw		a. On SG-299/U, install Adapter UG-274B/U on 754 output connector. b. On AN/USM-140B, connect CHANNEL A INPUT to one side of adapter installed in *a* above.	a. None. b. None.

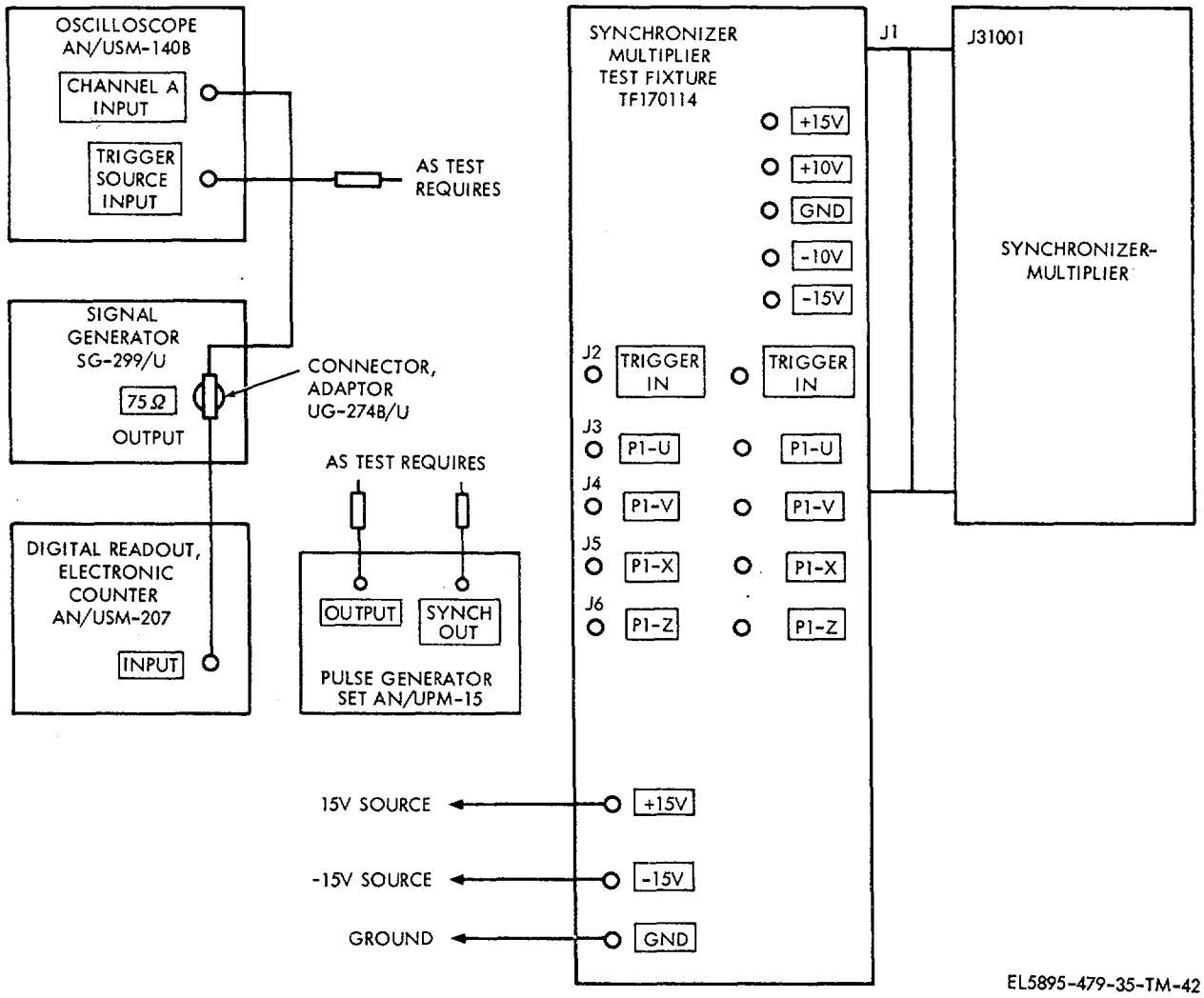


Figure 6-4. Blanker, Interference MX-5795/TPX-41, synchronizer-multiplier test connections.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	CHANNEL A VERTICAL POSITION: midposition HORIZONTAL DISPLAY: INTERNAL SWEEP MAGIFIER: X1 EXTERNAL VERNier: CAL AC-DC: DC SWEEP TIME: 9 MILLISECOND/CM): .5 VERNIER: CAL TRIGGER SLOPE: as desired. TRIGGER LEVEL: as desired. SWEEP MODE: PRESET TRIGGER: SOURCE: INT CHANNEL A-CHANNEL B: CHANNEL A CHANNEL A SENSITIVITY: (VOLTS/CM): 1 VERNIER: CALIBRATED CHANNEL A AC-DC: DC SG-299/U POWER: ON 75Ω ATTN: 0 db OUTPUT AMPLITUDE (75Ω): 0 db RANGE: X1K FREQUENCY: 1.5 AN/USM-207 POWER: TRACK FUNCTION: FREQ GATE TIME: 10-1 TF1 70114 POWER: ON		c. On AN/USM-207, connect INPUT to one side of adapter installed in a above. d. On SG-299/U, adjust OUTPUT AMPLITUDE control for 4 vpp signal as indicated on AN/USM-140B. e. On SG-299/U, adjust FREQUENCY control for an indication of 1500 +8 Hz as indicated on AN/USM-207.	c. None. d. None. e. None.
2	As last indicated, except: AN/USM-140B SWEEP TIME: (MILLISECONDS/CM): .2		a. On AN/USM-140B, remove CHANNEL A INPUT from 75Ω output of SG-299/U and connect to test point P1-Z on TF170114. b. On synchronizer-multiplier subassembly, turn LEVEL control R31037 ccw one-quarter turn past point at which oscillations cease. c. On AN/USM-207, remove test lead connected to INPUT and connect to connector J4 (P1-V) test point on TF170114.	a. 1500-Hz sine wave is present. b. None. c. 1500-Hz signal observed on AN/USM-140B.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			d. On synchronizer-multiplier subassembly, adjust FREQ control R31024 for max. amplitude of 1500-Hz sine wave. If clipping occurs during adjustment of R31024, readjust OUTPUT AMPLITUDE (75£) on SG-299/U to eliminate clipping. Continue adjustment of R31024.	d. None.
			e. On SG-299/U, adjust OUTPUT AMPLITUDE (75£) control for small amount of clipping of 1500-Hz sine wave.	e. None.
			f. On synchronizer-multiplier subassembly, adjust BAL control R31039 for symmetrical clipping of 1500-Hz sine wave.	f. None.
			g. On AN/USM-140B, temporarily remove CHANNEL A INPUT form P1-Z test point on TF170114 and connect to 75Ω output on SG-299/G.	g. None.
			h. On SG-299/U, adjust OUTPUT AMPLITUDE (7552) for 5.5v pp indication on AN/USM-140B.	h. None.
			i. On AN/USM-140B, reconnect CHANNEL A INPUT to P1-Z test point on TF170114.	i. 1500-Hz sine wave is present.
			j. On syncbronizer-multiplier subassembly, adjust LEVEL control R31037 for max amplitude of sine wave with no clipping	j. 1500-Hz sine wave amplitude is 20v pp min.
3	As last indicated, except: SG-299/U POWER: OFF	As last indicated------	Disconnect SG-299/U	None.
4	As last indicated, except: AN/UPM-15 POWER: ON SYNC selector knob: INT B BIAS: midposition pps SYNC switch: LEAD DELAY switch: SHORT DELAY dial: min.	As last indicated-----	a. On AN/USM-140B, remove CHANNEL A INPUT from P1-Z test point on TF170114 and connect to OUTPUT on AN/UPM-15. b. On AN/UPM-15, adjust WIDTH, COARSE ATTN, and FINE ATTN controls for 300 pps positive 3v peak, 0.5µsec pulse as viewed on AN/USM-140B.	a. None. b. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	SEPARATION: midposition WIDTH switch: NAR WIDTH dial: .5usec PULSE NO. 2: OUT POLARITY: POS COARSE ATTN knob: 1 FINE ATTN dial: 3 RISE TIME: min. AN/USM-140B SWEEP TIME: MICROSECONDS CM : 1 TRIGGER SOURCE EXT DC			
5	As last indicated, except: AN/USM-140B TRIGGER SOURCE EXT DC	As last indicated	a. On AN/UPM-15, disconnect AN/USM-140B, CHANNEL A INPUT connection from OUTPUT connector and install adapter UG-274B/U on OUTPUT connector. b. On AN/UPM-15, connect one side of adapter installed in a above to AN/USM-140B, TRIGGER SOURCE INPUT and other side of adapter to connector J3(P1-U) on TF 170114.	a. None. b. None.
6	As last indicated, except: AN/USM-140B SWEEP TIME: (MILLISECONDS/ CM): .2 VERNIER: for one full cycle	As last indicated-----	a. On AN/USM-140B, connect CHANNEL A INPUT to DELAY GATE test point TP31002 on synchronizer-multiplier subassembly. b. On synchronizer-multiplier subassembly, adjust DELAY ADJ R31017 from ccw limit to cw limit c. On AN/USM-140B, remove CHANNEL A INPUT FROM DELAY GATE test point TP31002 and connect to P1-Z test point on TF170114. d. Observe 1500-Hz waveform and verify waveform max and envelopes are within specified limits.	a. None. b. Square wave: Positive half-cycle Duration: adjustable from 450 ±90 µsec to 670 µsec. c. 1500-Hz sine wave present. d. 1500-Hz sine wave: Max envelope: 21 to 29v pp Min envelope: 16 to 24v pp
7	As last indicated, except: AN/UPM--15 WIDTH dial: 10.0Oµsec AN/USM-140B SWEEP TIME: (MICROSECONDS/ CM): 5	As last indicated. -----	a. On AN/UPM-15 remove OUTPUT from connector J3(P1-U) on TF170114 and connect to TRIGGER IN connector J2 on TF170114.	a. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			b. On AN/USM-140B remove HANNEL A INPUT from 1-Z test point and connect o TRIGGER IN test point n TF170114.	b. None.
			c. On N/UPM-15, adjust IDTH,COARSE ATTN, and FINE ATTN controls for 300 pps positive, 5v peak, 10.0-µsec pulse as viewed on AN/USM-140B.	c. one.
8	As last indicated, except: AN/USM-140B SWEEP TIME: (MICROSECONDS' CM): 5	As last indicated ------	On AN/USM-140B, remove CHANNEL A INPUT from TRIGGER IN test point Connect to P1-X test point and observe positive pulse.	Amplitude: +12.0v peak min. Pulse width:0.5µsec min. Prf: 300 pps.
9	As last indicated, except: ALL TEST EQUIPMENT POWER: OFF	As last indicated--------	Disconnect all test equipment and restore synchronizer-multiplier subassembly to service.	None.

6-10. Blanker, Interference MX-8795/ TPX-41, Processor Test

a. Test Equipment and Materials Required.

(1) Oscilloscope AN/USM-140B.

(2) Time Delay Generator MX-2962/USM.

(3) Pulse Generator AN/PPM-1A (2 required).

(4) Processor Test Fixture TF 125600.

(5) Connector UG-201A/U.

(6) Connector, Adapter UG-274B/U.

b. Dc Power Requirements. The dc power requirements listed in the chart below are required to perform the Blanker, Interference MX-8795/TPX-41, processor test.

NOTE

If available test equipment will not supply the power requirements listed in the following chart, a bench test power supply may be locally fabricated in accordance with figure FO-23 to provide the necessary voltages.

Voltage	Current (ma)	Regulation	Maximum rms ripple (mv)
-15v	2.4	+5%	10
+6v	11	+5%	100
-6v	2	+5%	100
3.3v	3	+5%	100

c. Test Conditions and Connections (fig. 6-5). Connect all test equipment as shown in figure 6-5.

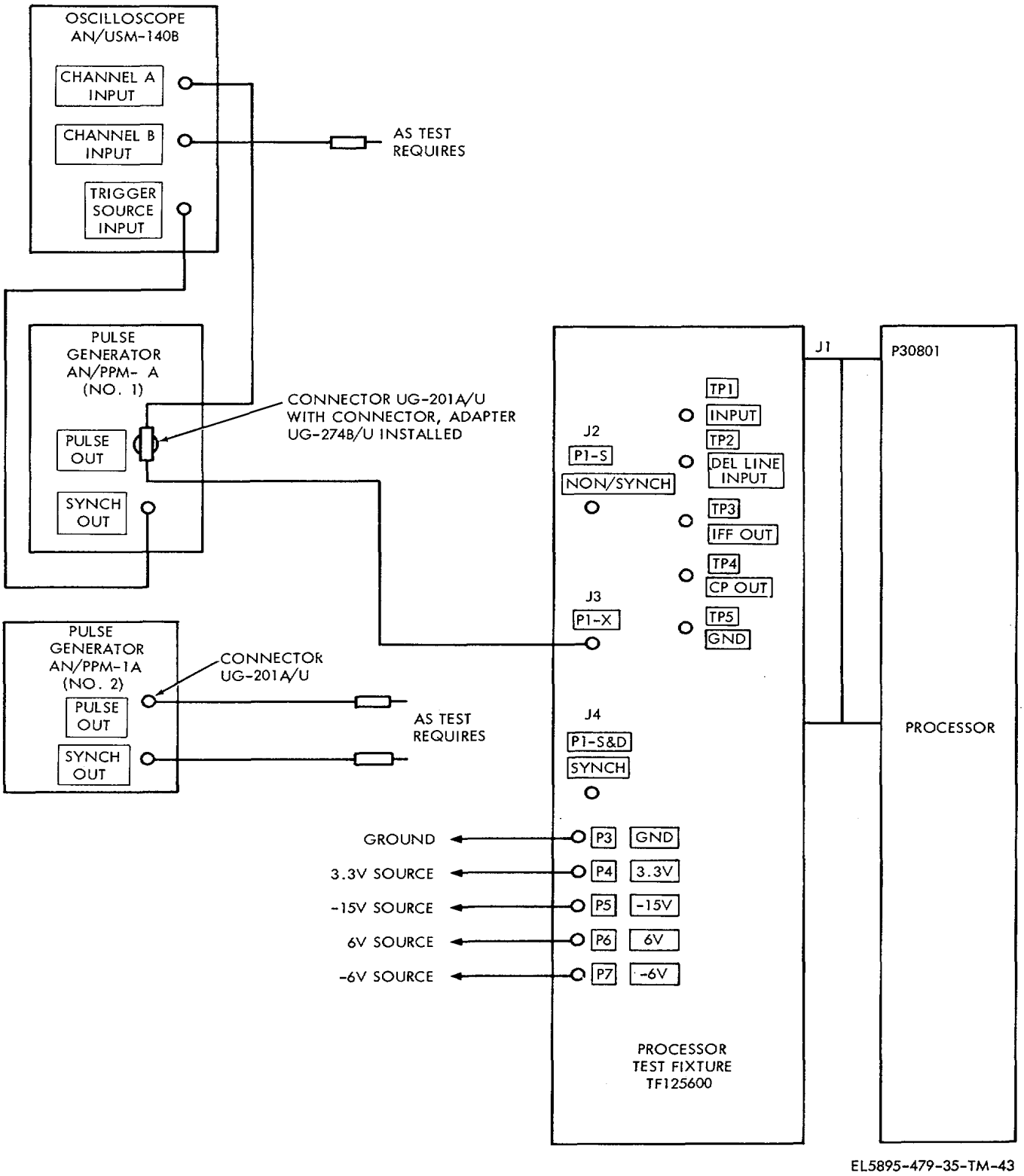


Figure 6-5. Blanker, Interference MX-8795/TPX-41, processor test connections.

d. Procedures.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/PPM-IA (No. 1) POWER: ON POLARITY: + SYNC SELECTOR X1 PULSE RATE:400 AMPLITUDE:4 AMPLITUDE :4 USEC: .45 AN/USM-140B INTENSITY:fully ccw FOCUS: center ASTIGMATISM: center SCALE LIGHT: center HORIZONTAL DISPLAY: EXT SENSITIVITY SWEEP MODE: PRESET TRIGGER SOURCE: EXT AC TRIGGERING LEVEL: center TRIGGERING SLOPE: center SWEEP SELEC- TOR: MAIN SWEEP TF12500 +6, -6: ON +3.3: ON IFF DEF: OFF CP: ON IFF: ON		a. On AN/PPM-IA, adjust PULSE OUT FOR 400-pps, positive 4v peak, 0.45-/asec duration, 0.02-/.sec rise time, as indicated on AN/USM-140B. b. On AN/USM-140B, move CHANNEL A INPUT connection to DEL LINE INPUT testpoint TP2 on TF125600. and measure positive pulse amplitude. c. On AN/USM-140B, measure pulse rise time at TP2 testpoint (10 to 90%). d. On AN/USM-140B, measure pulse width at TP2 testpoint e. On AN/PPM-1A (no. 1) move PULSE OUT connection to SYNC connector J4 on TF-125600. f. On TF125600 place CP switch S1 to OFF. g. On AN/USM-140B, connect CHANNEL A INPUT to CP OUT test point TP4 on TF-125600 h. On TF125600 place CP switch S1 to ON. i. On AN/USM-140B, observe positive pulse at CP OUT test point TP4 and measure amplitude. j. On AN/USM-140B, observe pulse width k. On AN/USM-140B, measure pulse rise time (10 to 90%amplitude point). l. On AN/USM-140B, remove CHANNEL A INPUT connection from CP OUT test point TP4 and connect to DEL LINE INPUT test point TP2 on TF125600. m. On AN/USM-140B, measure positive pulse amplitude. n. On AN/USM-140B, measure rise time of pulse at TP2 (10 to 90%). o. On AN/USM-140B, measure pulse width at TP2.	a. None b. 4.5v min. c. 0.2 µsec max. d. 0.4 µsec min. 0.6 µsec max. e. None. f. None. g. Observe no output. h. None. i. 2v min. j. 0.4 , µsec min. 0.6 ,usec max. k. 0.15 µsec. l. None. m. 4.5v min. n. 0.2 µsec max. o. 0.4 to 0.6 ,sec.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			p. On TF125600 place IFF switch S2 to OFF.	p. None.
			q. On AN/USM-140B, observe output at DEL LINE INPUT test point TP2.	q. No pulse present.
			r. On TF125600 place IFF switch S2 to ON	r. Pulse measured in m, n, and o above is present.
2	As last indicated, except: AN/PPM-IA (No.2) POWER: ON POLARITY: + SYNC SELECTOR: X1 PULSE RATE: 400 AMPLITUDE: 4 PULSE LENGTH µSEC: .45		a. On AN/PPM-1A (No. 2), connect PULSE OUTPUT to NON/SYNC connector J2 on TF125600.	a. None.
			b. On TF125600, place IFF DEF switch S3 to ON. *Note*. Do not synchronize AN] PPM-1A (No. 1) to AN/PPM--1A (No. 2)	b. None.
			c. On AN/USM-140B, move CHANNEL A INPUT to IFF OUT test point TP3 on TF-125600 and observe synchronous and nonsynchronous positive pulses.	c. None.
			d. On TF125600, place IFF DEF switch S3 to OFF.	d. None.
			e. On AN/USM-140B, observe that only synchronized pulses appear at IFF OUT test point TP3.	e. None.
			f. On AN/USM-140B, observe amplitude of positive pulse at IFF OUT test point TP3.	f. 3v min.
			g. On AN/USM-140B, observe pulse width at IFF OUT test point TP3.	g. 0.4 to 0.6 µsec.
			h. On AN/USM-140B, observe pulse rise time at 10 to 90% of amplitude point.	h. 0.1 ,µsec max.
			i. On TF125600, place IFF switch S2 to OFF.	i. None.
			j. On AN/USM-140B, observe output at IFF OUTPUT test point TP3.	j. No pulse present.
			k. On TF125600, place IFF switch S2 to ON	k. Pulse measured in f, g and h above is present.
3	As last indicated, except: AN/USM-1403B POWER: OFF AN/PPM--A (No.1 and No. 2) POWER: OFF TF1 25600 POWER: OFF		a. Disconnect all test equipment and restore processor sub-assembly to service.	a. None.

6-11. Blanker, Interference MX-8795/TPX-41, Video Test

a. Test Equipment and Materials

(1) Oscilloscope AN/USM-140B.

(2) Time Delay Generator MX-2962/USM.

(3) Pulse Generator Set AN/UPM-15 (2 required).

(4) Blanker, Interference MX-8795/TPX-41 test fixture TF 181530.

(5) Dummy Load, Electrical DA-232/U.

(6) Connector, Adapter UG-274B/U (4 required).

(7) Resistor, 510-ohm, 2-watt.

(8) Resistor, 2k, 2-watt (2 required)

b. Test Conditions and Connections (fig. 6-6). Connect all test equipment as shown in figure 6-6.

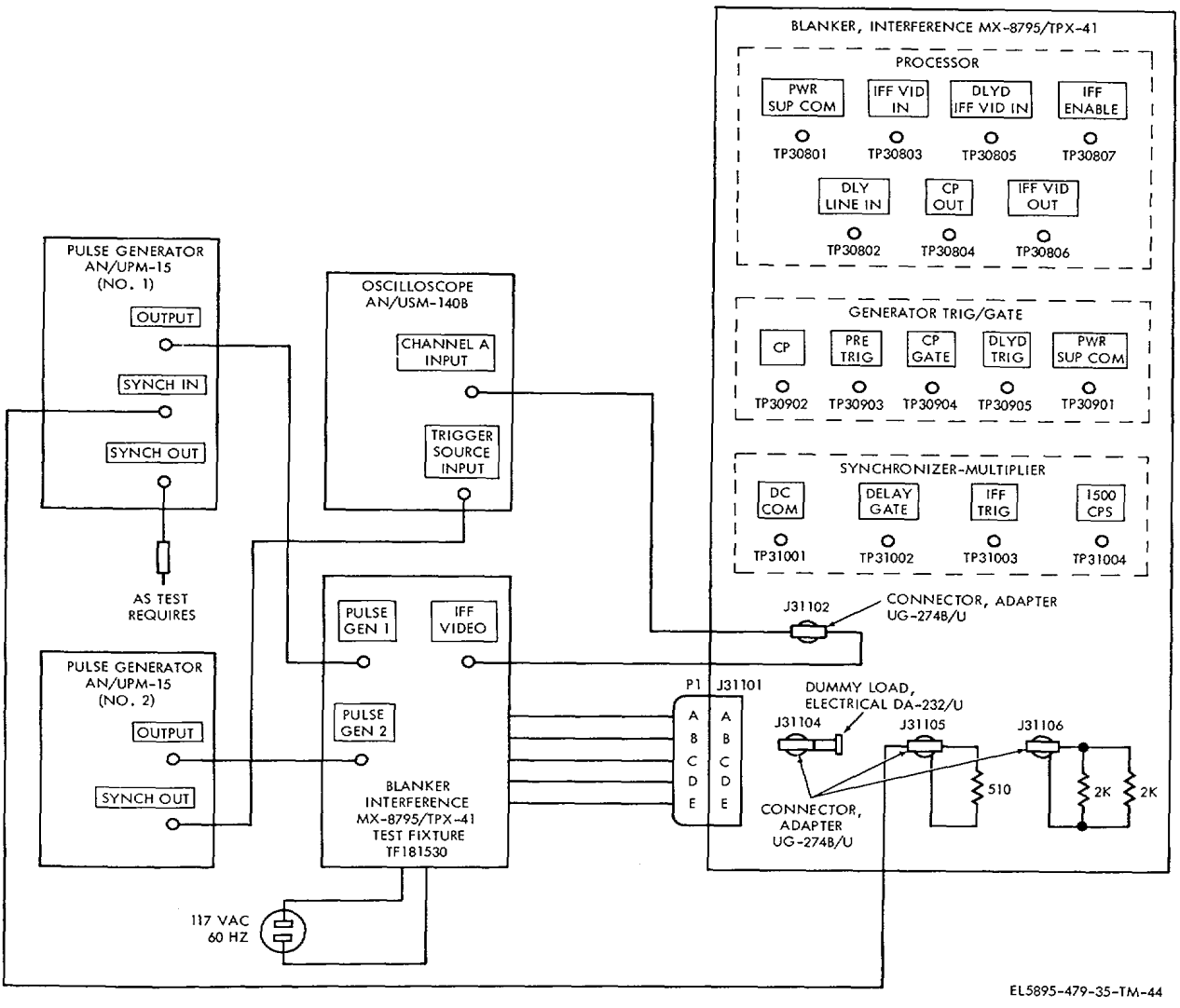


Figure 6-6. Blanker, Interference MX--8795/TPX--41, video test connections.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/UPM-15 (No. 1) POWER: ON SYNC selector knob: EXT GOING- BIAS: midposition PULSE RATE: 300 pps SYNC switch: LEAD DELAY dial: min DELAY switch: SHORT SEPAPATION: midnosition WIDTH switch: NAR switch: and FINE ATTN controls for PULSE NO. 2: OUT POLARITY: POS RISE TIME: min COARSE ATTN knob: 1 FINE ATTN dial: 6 AN/UPMV-15 (No. 2) POWER: -ON SYNC control: B INT B BIAS: midposition SYNC switch: LEAD PULSE RATE: 300 pps DELAY dial: min DELAY switch: SHORT SEPARATION: midposition WIDTH switch: NAR WIDTH dial: 5µsec PULSE NO. 2: OUT POLARITY: POS COARSE ATTN knob: 1 FINE ATTN dial: 6 RISE TIME: min AN/USM-140B POWER: ON ASTIGMATISM: midposition FOCUS :midposition INTENSITY: mid-position SCALE LIGHT: fully cw CHANNEL A VERTICAL POSI-TION: midposition	MX-8795/TPX-41 POWER: ON **PRF SEL Switch S3: 2**	a. On trigger/gate generator sub-assembly, rotate PW ADJ con-trol R30907 fully cw. b. On AN/UPM-15 (No. 2), ad-just WIDTH, COARSE ATTN, and FINE ATTN controls for 300-pps, positive 6v peak, 0.5 µsec duration pulse as in-dicated on AN/USM-140B. c. On AN/UPM-15 (No. 2), re-move cable from SYNC OUT and connect to SYNCH OUT connector on AN/UPM-15 (No. 1). d. On AN/UPM-15 (No. 1), ad-just WIDTH, COARSE ATTN, 300-pps, positive 6v peak, 0.5 µsec duration pulse, de-layed 0 µsec from SYNC pulse as indicated on AN/USM-140B. e. On AN/UPM-15 (No. 1), re-move cable from SYNC OUT connector and connect to CP test point TP30902 on trigger gate generator subassembly.	a None. b. None. c. None. d. None. e. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	HORIZONTAL DISPLAY: INTERNAL SWEEP MAGNI- FIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: MICROSECONDS/ CM: 1 VERNIER: CAL TRIGGER SLOPE: as desired. TRIGGER LEVEL: as desired. SWEEP MODE: PRESET TRIGGER SOURCE:EXT AC CHANNEL A- CHANNEL B: CHANNEL A CHANNEL A SENSITIVITY: (VOLTS/CM): 2 VERNIER: CALIBRATED CHANNEL A AC- DC: DC Remaining controls may be in any position. TF 181530 117 VAC: ON VIDEO REMOTE: RAW			
2	As last indicated, except: AN/USM-140B CHANNEL A SENSITIVITY: (VOLTS/CM): 5	As last indicated----------	a. On AN/USM-140B, remove CHANNEL A INPUT from IFF video in connector J31102 and connect to PRE TRIG test point TP30903 on trigger/gate generator sub-assembly. b. On trigger/gate generator sub-assembly, adjust PW ADJ control R30907 for correct positive pulse duration.	a. None. b. 0.4 μsec duration.
3	As last indicated, except: SEAN/USM-I:40B SENSITIVITY: .5 SWEEP TIME: MICROSECONDS/ CM: 2	As last indicated .-------	a. On AN/USM-140B, remove CHANNEL A INPUT from PRE TRIG test point TP 30903 and connect to IFF ENABLE test point TP 30807 on processor subassembly.	a. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	HORIZONTAL DISPLAY: INTERNAL SWEEP MAGNIFIER X100		b. On trigger/ gate generator subassembly, adjust IFF GATE control R30920 for correct negative gate duration.	b. 2450 µsec.
			c. On AN/UPM-15 (No 2), temporarily remove OUTPUT lead to PULSE GEN 2 connector on TF181530.	c. None.
			d. On AN / USM-140B, remove CHANNEL A INPUT from IFF ENABLE testpoint TP 30807 and connect to CP GATE testpoint TP30904 on trigger / gate generator subassembly.	d. None.
			e. On trigger/ gate generator subassembly, adjust CP GATE control R30936 for correct positive gate duration.	e. µsec
			f. On AN/UPM-15 (No 2), replace OUTPUT lead removed in c above	f. Same as e above. Observe that jitter present on trailing edge of wavefrom does not exceed 100 µsec max.
			g. On AN / USM-140B, remove CHANNEL A INPUT from CP GATE testpoint TP30904 and connect to DLYD TRIG testpoint TP30905 on trigger / gate generator subassembly.	g. None.
4	As last indicated, except: AN/USM-140B SENSITIVITY: 1 SWEEP TIME: (MICROSEC-ONDS/CM): 10	As last indicated	On trigger/gate generator subassembly, adjust DELAY ADJ control R30942 for correct pulse delay.	90 0 µsec. Observe that pulse position is variable between 70 to 110 µsec from start of sweep.
5	As last indicated, except: AN/ USM-207 POWER: TRACK FUNCTION: FREQ GATE TIME: 10-1	As last indicated	a. On AN / USM-207, connect SIGNAL INPUT to adapter on IFF trigger connector J31105 on MX-8795 / TPX-41.	a. None.
			b. On AN / USM-207, adjust DISPLAY TIME control as needed to observe frequency as indicated.	b. 299.8 pps min, 300.2 pps max.
			c. On MX-8795/TPX-41, set PRF SEL switch to position l. Observe digital readout.	c. 374.9 pps min, 375.1 pps max.
			d. On MX-8795/TPX-41, set PRF SEL switch to position 3. Observe digital readout.	d. 249.9 pps min. 250.1 pps max.
			e. On MX-8795 / TPX-41, return PRF SEL switch to position 2.	e. None.
			f. Disconnect AN/USM-207	f. None.
6	As last indicated	.....	a. On AN / USM-140B, connect TRIGGER SOURCE IN-PUT To SYNC OUT on AN/UPM-115 (No. I).	a. None.
			b. On MX-8795 / TPX-41, temporarily install connector UG-274 / U with DA-232 / U on IFF video out connector J31103	b. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			c. On AN/USM-140B, remove CHANNEL A INPUT from DLYD TRIG testpoint TP30905 and connect to adapter on IFF video out connector J31103 on MX-87 9./TPX-41.	c. Observe positive free running pulses.
	TF 181530 VIDEO) REMOTE: PROCESS ED	MX-8795/TPX-41 PROCESSED VIDEO- RAW VIDEO: ROCESSED	d. On AN/USM-140B, observe presentation	d. Positive free running pulses are removed.
7	As last indicated, except: AN/USM-140B CHANNEL A- CHANNEL B: : CHANNEL A	As last indicated	On AN/USM-140B, observe characteristics of positive pulse	Amplitude: 3v peak min. Duration: 0.3 μsec min. 0.6 μsec max. Rise time: 0.1 μsec max.
8	ALL TEST EQUIPMENT POWER: OFF	MX-8795/TPX-41 PO'WER: OFF	Disconnect all test equipment and restore MX-8795/TPX-41 to service.	None.

6-12. (Coder-Control KY-97C/TPX, General Support Testing

For information pertaining to the testing of Coder-Control KY-97C/TPX, refer to TM 11-5895-201-3 5.

6-13. Control, Remote Switching C1271A/ TPX-22, Physical Test and Inspection

a. Test Equipment and Materials filter.

Required. Light Assembly, Electric MX-1292/PAQ.

b. Test Connections and Conditions.

(1) Disconnect all external cables to C-1271A/TPX-22.

(2) Connect MX-1292/PAQ to 117-vac power source and install wide band transmission

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	None	Controls may be in any position	a. On C-1271A/TPX-22. rotate RECEIVER GRAIN control R731 throughout limits of travel.	a. Control R731 should rotate smoothly without sticking or binding.
			b. Operate front panel switches throughout all positions	b. Switches should operate smoothly, without sticking or binding.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			c. Inspect front panel lamps for completeness. d. Inspect front panel lamps, switches, and controls for evidence of looseness. e. Inspect connectors J731 and J732 for evidence of damage or looseness f. Inspect wiring for condition of insulation g. Inspect metal surfaces for condition of finish and panel markings *Note*. Touchup painting is recommended in lieu of refinishing whenever practicable.	c. Lamps should be complete. d. Lamps, switches, and controls should be securely mounted. e. Connectors should be physically undamaged and securely mounted to chassis. f. Insulation should be free from cracks or fraying. g. All metal surfaces intended to be painted must not show bare metal. Panel markings should be legible.
2	MX-1292/PAQ 245V for M.V lamps: ON	C-1271A/TPX-22	a. On C-1271A/TPX-22, expose chassis to direct rays of MX-1292/PAQ. Inspect components, wiring, and chassis surfaces for evidence of polyurethane coating. Inspect connector, switch contacts, and jacks for absence of polyurethane coating *Note*. Polyurethane coating glows grayish-blue when exposed to rays of MX-1292/PAQ. b. On MX-1292/PAW, turn off ac power and disconnect.	a. All components, wiring, and chassis surfaces should be completely covered with MFP varnish. There should be no evidence of MFP on connector and switch contacts. *Note.* Do not apply polyurethane coating to parts not originally finished with polyurethane. b. None.

6-14. Modulator, Pulse MD-638/TPX-41, Physical Test and Inspection

a. Test Equipment and Materials Required.
Light Assembly, Electric MX-1292/PAQ

b. Test Connections and Conditions

(1) Disconnect all external cables.

(2) Connect MX-1292/PAQ to a 117 vac power source and install wideband transmission filter.

(3) Remove pulse generator processor subassembly from MD-638/TPX-41.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	None	Controls may be in any position	a. Operate front panel switches in both directions b. Inspect front panel lamp for completeness. Rotate controls throughout limits of travel	a. Switches should operate smoothly without sticking or binding. b. Lamp should be complete. Controls should rotate smoothly without binding or sticking.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			c. Inspect front panel lamp, switches, and controls for evidence of looseness.	c. Lamp, switches, and controls should be securely mounted.
			d. Inspect connectors for evidence of damage or looseness mounted to chassis.	d. Connectors should be physically undamaged and securely
			e. Inspect wiring for condition of insulation	e. Insulation should be free from cracks or fraying.
			f. Inspect metal surfaces for condition of finish and panel markings. Note. Touchup painting is recommended in lieu of refinishing whenever practicable.	f. All metal surfaces intended to be painted must not show bare metal. Panel markings should be legible.
2	MX-1292/PAQ 245V for M.V	MD-638/TPX-41	a. On MD-638/TPX-41, expose main chassis and plug-in subassembly to direct rays of MX-1292/PAQ. Inspect components, wiring and chassis surfaces for evidence of polyurethane coating. Inspect connector, switch contacts, and jacks for absence of polyurethane with polyurethane. *Note.* Polyurethane coating glows grayish-blue when exposed to rays of MX-1292/PAQ.	a. All components, wiring, and chassis should be completely covered with polyurethane coating. There should be no evidence of polyurethane coating on connector contacts. *Note.* Do not apply polyurethane coating to parts not originally finished
			b. On MX--1292/PAW, turn off ac power and disconnect.	b. None.

6-15. Modulator, Pulse MD-638/TPX-41, Power Supply Test

a. Test Equipment and Materials.

(1) MultimeterTS-352/U

(2) Voltmeter, Electronic ME-30/U.

(3) Transformer, Variable Power CN-16B/U

(4) Generator, Pulse Test Fixture TF112312.

b. Test Conditions and Connections (fig. 6-7).

(1) Remove pulse generator processor subassembly from Modulator, Pulse MD-638/TPX-41.

(2) Connect all test equipment as shown in figure 6-7. Meter connections are shown only for initial measurements.

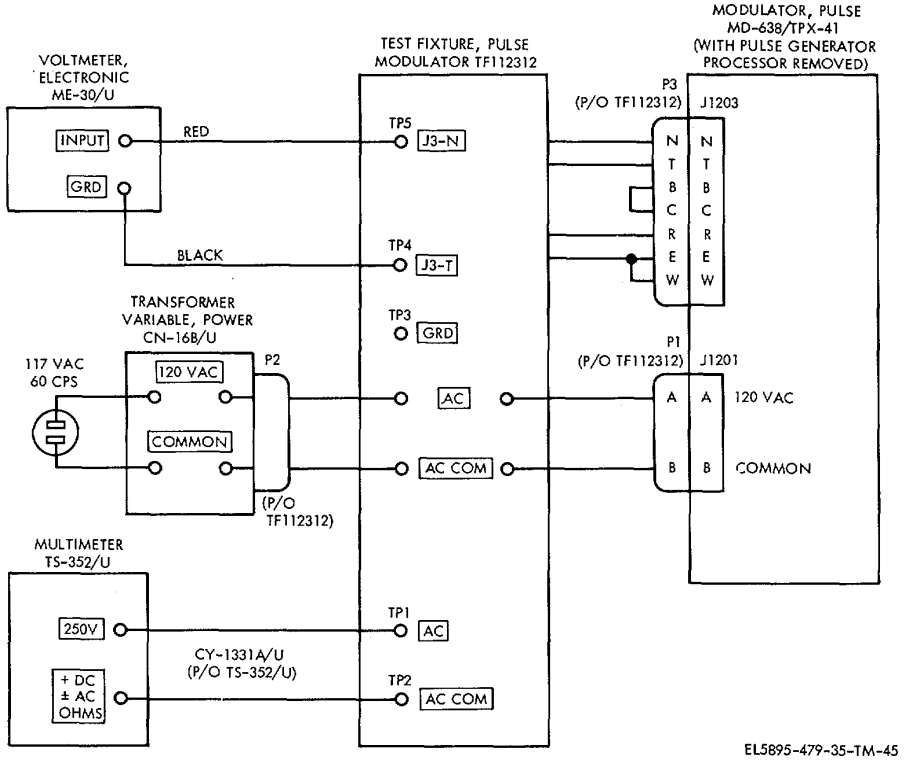


Figure 6-7. Modulator, Pulse MD-638/TPX-41, power supply test connections.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	***TS-352/U*** **FUNCTION: AC VOLTS**	***MD-638/TPX-41*** **With pulse generator processor subassembly removed**	***a.*** **On CN-16B/U, adjust output control for 107 vac as indicated on TS-352/U.**	***a.*** **None.**
	CN/-16B/U **Power control: fully ccw:**	**POWER switch S1301: ON**	***b.*** **On TS-352/U, remove red lead from AC test point TP1**	**b. None**
	ME-30/U ON-OFF: OFF	**ON**	**AC COM test point TP2 on**	**and remove black lead from TF112312.**
	TF112312 VAR. AC POWER: ON	***c.***	**On TS-352/U, place FUNCTION switch to DIRECT.**	**c. None.**
d.	**None.**		***d.*** **lead to GRD test point TP3 of TF112312. Connect red lead between 500V connector on 20, 000 OHMS PER VOLT DC range and J3-N test point TP5 on TF112312.**	**On TS-352/U, connect black**
	e.	**Observe voltage on TS-352/U.**	***e.*** **+250 ±30v.**	

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			f. On TS-352/U, remove red lead between 500V connector and pin J3-N test points TP5 on TF112312, and connect between 50V connector on same range and GRD test point TP3 on TF112312.	*f.* None.
			g. On TS-352/U, remove black lead from GRD test point TP3 on TF112312 and connect to J3-T test point TP4 on TF112312.	*g.* None.
			h. On TS-352/U, observe voltage (with leads reversed, negative voltage is indicated by positive value).	*h.* -30 +3v.
			i. Remove TS-352/U from circuit.	*i.* None.
	As last indicated - except: *ME-30/U* VOLTS: 10	As last indicated------	j. On ME-30/U, observe ripple voltage on 0--1.0 RMS VOLTS	*j.* Should indicate no greater than 3v rms. scale.
	As last indicated except: ME-*30.U* VOLTS: 3	As last indicated------	*k.* On ME-30/U, remove positive test lead from J3-N test point on TF112312 and connect to J3-T test point TP4 on TF112312.	k. None.
greater		*l.*	On ME-30/U, observe ripple voltage on 0-3 RMS VOLTS scale.	*l.* Should indicate no than 1v rms.
		m.	Remove ME-30/U from circuit.	*m.* None.
2	As last indicated, except: *TS-352/U* FUNCTION: AC VOLTS	As last indicated ------	*a.* On TS-352/U, connect black connector and AC COM test point TP2 on TF112312. Connect red test lead between 250V connector on 1000 OHMS PER VOLT AC range and AC test point TP1 of TF112312.	*a.* None.
		b.	On CN-16B/U, adjust control for 117 vac as indicated on TS-352/U.	*b.* None.
		c.	Repeat steps 1c through 1m above.	*c.* As indicated in steps 1c through through 1m above.
3	As last indicated	As last indicated -----	*a.* On TS--352/U, connect black lead between OHMS-DC +AC connector and COM test point TP2 on TF112312. Connect red test lead between 250V connector on 1000 OHMS PER VOLT AC range and AC test point TP1 of TF112312.	*a.* None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			b. **On CN-16B/U, adjust control for 130 vac as indicated on TS-352/U.**	***b.*** **None.**
			c. Remove TS-352/U from circuit.	**c. None.**
			d. **Repeat steps 1c through 1m and observe limits of performance standards.**	**d. As indicated 1c through 1m above.**
			e. Remove ac power from test equipment and test fixture.	**e. None.**
			f. **Remove test equipment and test fixture connector P3 from MD-638/TPX-41.**	***f.*** **None.**
			g. **Replace pulse generator processor subassembly and restore MD-638/TPX-41 to service.**	**g. None.**

6-16. Modulator, Pulse MD-638/TPX-41, Pulse Generator Processor Output Test

a. Test Equipment and Materials.

(1) Pulse Generator AN/PPM-1A (2 required).

(2) Oscilloscope AN/USM-140B.

(3) Multimeter TS-352/U.

(4) Transformer, Variable Power CN-16B/U.

(5) Adapter, Connector UG-201A/U (3 required).

(6) Adapter, Connector UG-274B/U (7 required).

(7) Test Fixture, Pulse Modulator, TF112312.

b. Test Conditions and Connections.

(1) Insure that pulse generator processor subassembly is installed in Modulator, Pulse MD-638/TPX-41.

(2) Connect all test equipment as shown in figure 6-8. Meter connections are shown for initial measurements.

(3) Apply 120 vac to AN/PPM-1A (No. 1 and No. 2), and AN/USM-140B. Allow 5 minutes for stabilization.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/PPM-1A (No. 1) POWER: ON PULSE RATE: 500 pps ATTENUATION:0 SYNCH SELEC- TOR: XI POLARITY: POS PULSE LENGTH 1 μsec5 AMPLITUDE: 55 POS OR NEG: POS PULSE POSITION: 0 AN/PPM-IA (No. 2) POWER: ON -, PULSE RATE: 500 pps ATTENUATION: 0 SYNC SELEC- TOR: POS POLARITY: POS PULSE LENGTH: 1 μsec AMPLITUDE: 55 POS OR NEG: POS CN--16B/U. PULSE POSITION: 30 μsec AN/USM-140B POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: Midposition SCALE LIGHT: fully cw. CHANNEL A VERTICAL POSITION: midposition POLARITY: + UP HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY: IN- TERNAL SWEEP MAGNI- FIER: X1 EXTERNAL VER- NIER: CALIBRATE	MD-638/TPX-41 POWER switch S1301: OFF CN-1B/U	a. On AN/USM-140B, observe CHANNEL A INPUT is +30v amplitude, 1 /a sec duration, 0.1 a sec max rise time; adjust AN/PPM-1A (No. 1) as required. b. On AN/USM-140B, observe CHANNEL B INPUT is +30v amplitude, 1 p sec duration, just AN/PPM-1A (No. 2) as required. c. On AN/USM-140B, place SWEEP TIME TO MICRO-SECONDS/CM: 5 d. On AN/PPM-1A (No. 2), rotate PULSE POSITION control until delay between pulses indicated on AN/USM-140B is 30 p sec (leading edge to leading edge). e. On CN-16B/U, connect 120 vac output to test fixture connector P2 and test fixture J1201 on MD-638/TPX-41. Apply120vac to f. On TS-352/U, connect black test lead between OHMS-DC ±AC and AC COM test point TP2 on TF112312; connect red test lead between 250V on 1000 OHMS PER VOLT AC range and AC test point g. On CN-16B/U, adjust control for 120 vac as indicated on TS-352/U. h. Remove TS-352/U from circuit, and on AN/USM-140B, remove cable CG-409E/U between PULSE OUT on AN/PPM 1A (No. 1) and CHANNEL A INPUT.	a. None. b. None. 0.1 μsec max rise time; ad- c. None. d. None. e. None. connector P1 to connector f. None. TP1 on TF112312. g. None. h. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	AC-DC: DC SWEEP TIME: MICROSECONDS/CM:.5 VERNIER: CAL TRIGGER SLOPE: as desired TRIGGER LEVEL: as desired SWEEP MODE: PRESET TRIGGER SOURCE: EXT AC CHANNEL A- CHANNEL B: ALTERNATE CHANNEL A SENSITIVITY: (VOLTS/CM): 10 VERNIER: CALIBRATED AC-DC: DC Remaining controls may be in any position.			
	As last indicated, except: *TS-352/U* FUNCTION: AC VOLTS *CN-16B/U* Variable control: fully ccw. *TF112312* VAR. AC POWER: ON	As last indicated, except: *MD-638/TPX-41* POWER switch S1301: ON SLS switch S1302: ON		
2	As last indicated, except: AN/USM-140B CHANNEL A- CHANNEL B: CHANNEL A SWEEP TIME: (MICROSECONDS /CM): .5	As last indicated	*a.* On AN/USM-140B, using NEL A INPUT to UG-274A/U on P2 MOD connector J1208on MD-638/TPX-41 (fig. 6-8). b. On pulse generator processor subassembly, adjust P2 PULSE WIDTH control R1321 for correct pulse width. *c.* On pulse generator processor subassembly, rotate CP DELAY ADJ control R1343 fully ccw.	a. None CG-409E/U, connect CHAN- b. 0.8 p sec (50-percent amplitude points). c. None

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			d. On AN/USM-140B, connect CG-409E/U between CHANNEL B INPUT and connector UG-274B on PULSE OUT connector of AN/PPM-1A (No. 1).	*d.* None.
			e. On pulse generator processor subassembly adjust P2 DELAY ADJ control R1315 for correct delay between pulse from AN/PPM-1A (No. 1) and pulse from P2 MOD connector J1208 on MD-638/TPX-41.	*e.* 1.9 μsec delay (leading edge to leading edge).
			f. On AN/USM-140B, at CHANNEL A INPUT, observe pulse from P2 MOD connector J1208.	f. Positive pulse, 180v peak amplitude or greater, 0.2 usec rise time max.
			g. On AN/USM-140B, at CHANNEL A INPUT, disconnect CG409E/U from J1208, and connect to UG-274B/U through UG-201A/U to RF OUT connector CP1201 on MD-638/TPX-41 (fig. 6-8).	*g.* None.
3	As last indicated, except: *AN/USM-140B* CHANNEL A SENSITIVITY: (VOLTS/CM): 2	As last indicated ------	*a.* On ANIUSM-140B, at CHANNEL A INPUT, observe pulse from RF OUT connector CP121.	a. Positive pulse.
			b. On AN/USM-140B, at CHANNEL B INPUT, observe delay between pulse from AN/PPM-1A (No. 1) and pulse from RF OUT connector CP1201 at CHANNEL A INPUT.	b. Less than 1.5 /μsec (leading edge to leading edge).
4	As last indicated, except: *AN/USM-140B* CHANNEL B SENSITIVITY: (VOLTS/CM): 5 VERNIER: CALIBRATED	As last indicated ------	a. On AN/USM-140B, remove CG-409E/U between CHANNEL B INPUT and PULSE OUT of AN/PPM-1A (No. 1)	*a.* None.
			b. On AN/USM-140B, connect CG-409E/U between CHANNEL B INPUT and P2 MOD connector J1208 of MD-638/TPX-41.	*b.* None.
		c.	On AN/USM-140B, adjust VERNIER SENSITIVITY control on CHANNEL B to equalize amplitude of CHANNEL A INPUT and CHANNEL B INPUT pulses.	c. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			d. On pulse generator processor subassembly, adjust CP DELAY ADJ control R1343 and check on AN/USM-140B, at CHANNEL A INPUT, that trailing edge is coincident with trailing edge at CHANNEL B INPUT.	*d.* None.
			e. On AN/USM-140B, observe CHANNEL A INPUT from RF OUT connector CP1201.	e. 1.2 + 0.2 μsec duration (50% amplitude points; if pulse jitters, measure leading jitter edge of pulse rise to leading jitter edge of pulse fall): 55v peak or greater, 0.3 usec or less rise time (10 to 90% amplitude points).
			f. On AN/USM-140B, at CHANNEL A INPUT, remove CG-409E/U from UG-274B/U on RF OUT connector' CP1201, and at CHANNEL B INPUT on P2 MOD connector J1208 on MD-638/TPX-41.	*f.* None.
5	As last indicated, except: *AM/USM-140B* CHANNEL B: SENSITIVITY:	As last indicated ------	a. On AN/USM-140B, connect CG-409E/U between CHANNEL A INPUT and UG-274B connector on CODED PAIR IN connector J1202. Also, connect second CG409E/U between CHANNEL B INPUT and UG-274B/U on CODED PAIR OUT connector J1209.	a. None.
			b. On AN/UM-140B,adjust CHANNEL B VERNIER sensitivity control to equalize amplitude of CHANNEL A INPUT and CHANNEL B INPUT pulses.	*b.* None.
			c. On AN/USM-140B, observe time relationship of CHANNEL A INPUT pulse from CODED PAIR IN connector J1202 and CHANNEL B INPUT pulse from CODED PAIR OUT connector J1209.	c. Identical pulse pair.
			d. On CN-16B/U, remove ac input power and test fixture connector P2.	*d.* None.
			e. On TF112312, remove all test circuits and power connections.	e. None.
			f. On AN/USM-140B, remove both CG-409E/U from test connections.	f. None.

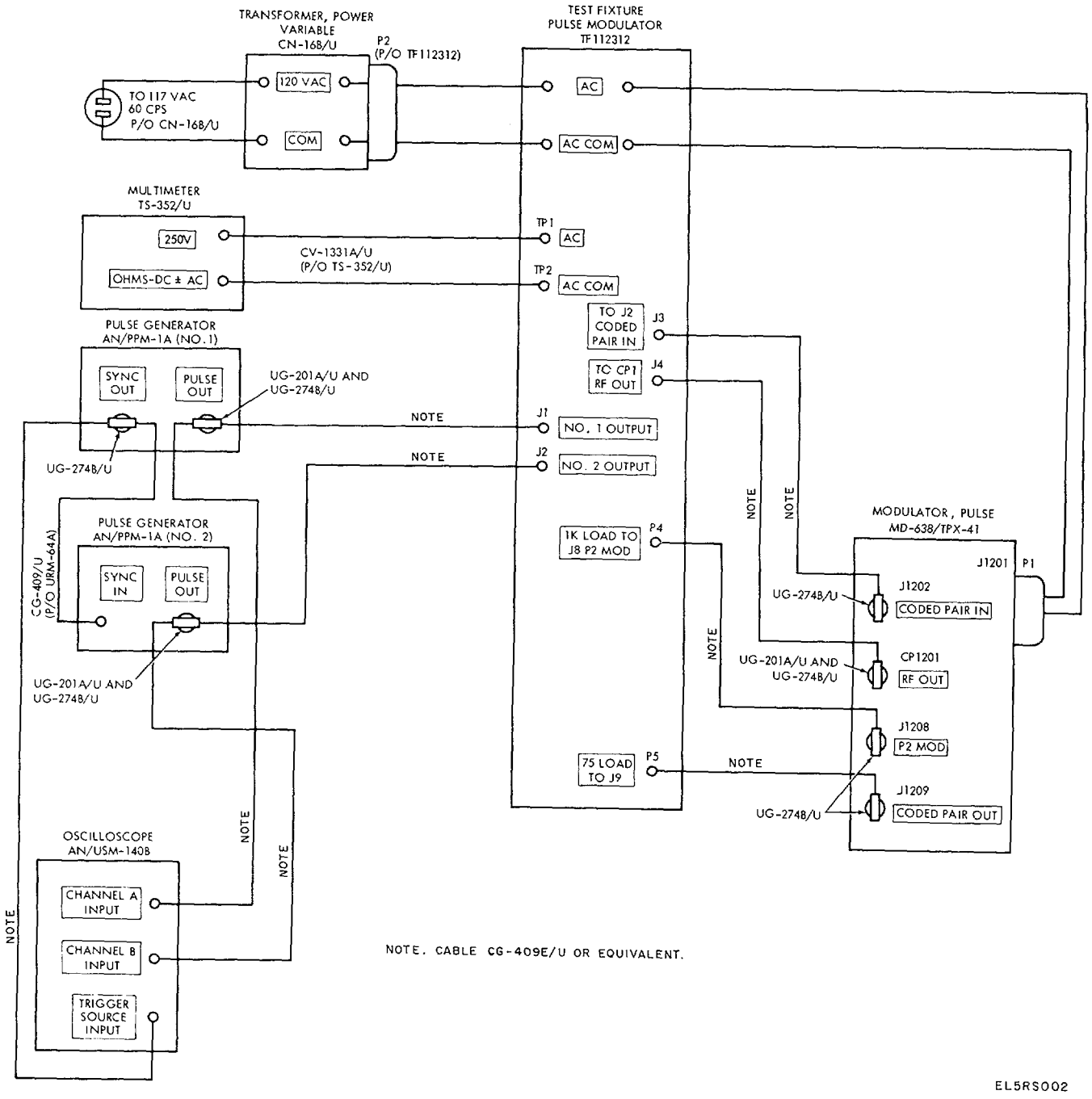


Figure 6-8. Modulator, Pulse MD-638/TPX-41, pulse generator processor output test connections.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			g. Remove all test circuit connectors from MD-638/TPX-41.	g. None.

6-17. Modulator, Pulse MD-638/TPX-41, Pulse Generator Processor Test

a. Test Equipment and Materials.

(1) Multimeter TS-352B/U.

(2) Pulse Generator AN/PPM-1A (2 required).

(3) Oscilloscope AN/USM-140B.

(4) Power Supply PP-3155/U (2 required).

(5) Test Fixture, Pulse Generator Processor, TF119849.

(6) Adapter, Connector UG-201A/U (2 required).

(7) Adapter, Connector UG-274B (3 required).

b. Test Conditions and Connections.

(1) Remove pulse generator processor subassembly from Modulator, Pulse MD-638/TPX-41.

(2) Complete test equipment connections as shown in figure 6-9. Meter connections are shown only for initial measurements.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	TS-352B/U FUNCTION: OHMS RANGE: RX1	Pulse generator processor bly. remove from TF119849 and set switches as follows: POWER switch S1301: OFF SLS switch S1302: OFF	a. On TS-352B/U, connect subassem- Temporarily and TP1 on pulse generator processor subassembly TF119849. Connect red test nector and INPUT J1-F on pulse generator processor subassembly. b.	a. None. black test lead between OHM-DC +AC connector lead between OHMS con- On TS-352B/U, observe b.
75 ±4 ohms.			reading.	
2	As last indicated, except: TS-352B/U FUNCTION: DC CURRENT RANGE: 100 MA PP-3135/U (+250V) AC POWER: ON METER RANGE: 0-500 VOLTS HIGH VOLTAGE: ON HV CONTROL: Set to 250 vdc.	Pulse generator processor subassembly Reinstall in TF119849	a. On TS-352B/U, remove red lead from OHMS connector and connect between +DC CURRENT connector and POS testpoint TP2 on test fixture TF119849. Connect black test lead between OHMS - DC ±AC connector and NEG testpoint TP3 on test fixture TF 119849.	a. None.

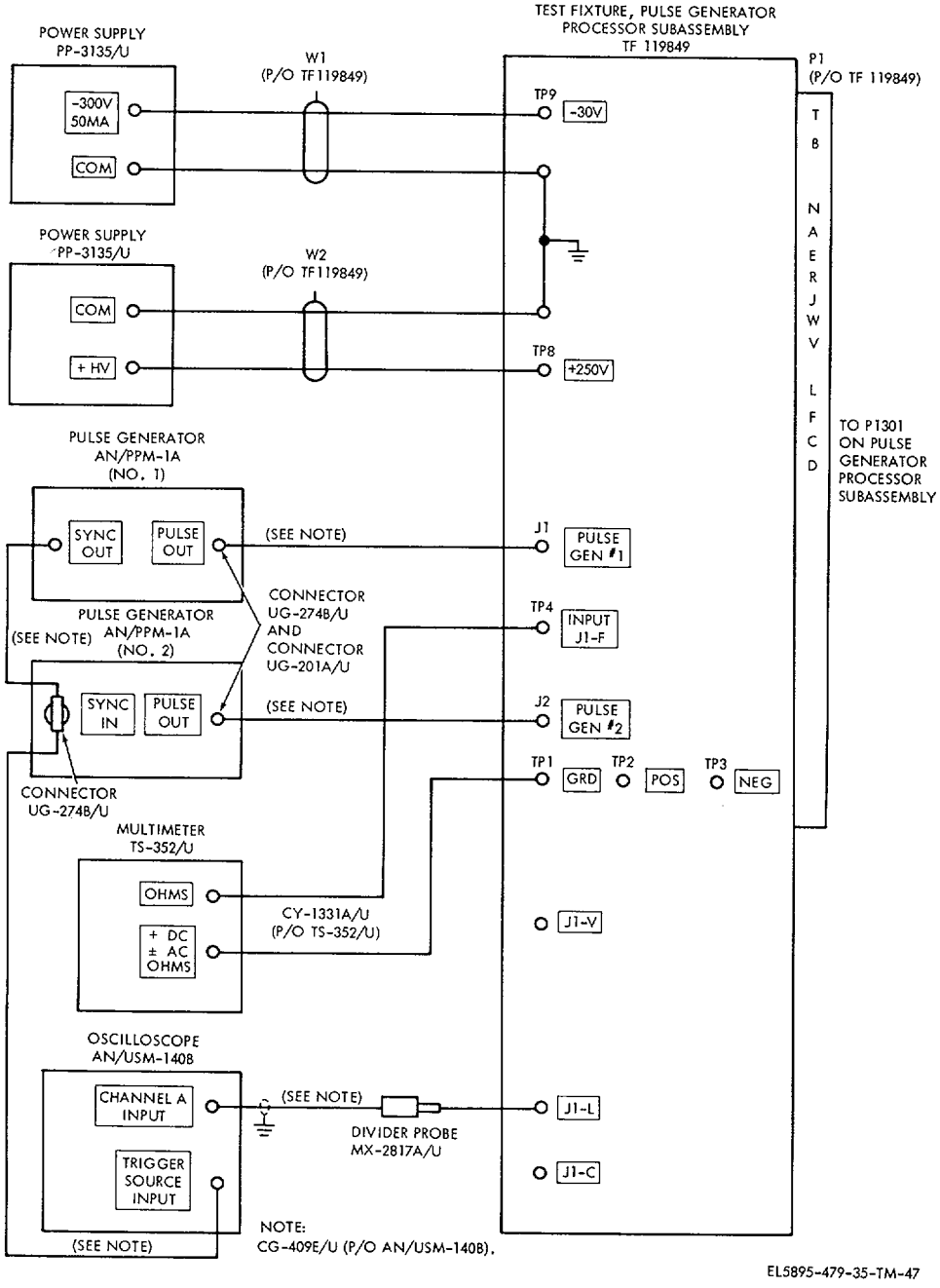


Figure 6-9. Modulator, Pulse MD-638/TPX-41, pulse generator processor test connections.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	PP-3135/U (-30V) AC POWER: ON METER RANGE: 0-50 VOLTS DC VOLTAGE: ON DC CONTROL: Set for -30 vdc. TF 119849 LOAD-GROUNDED-OPEN: LOAD +250V: OFF -30V: OFF			
	As last indicated, except: TF 119849 -30V: ON	As last indicated, except: Pulse generator processor subassembly POWER switch S1301: ON	b. On test fixture TF 119849, current switch S2 to open position. Observe load current indication on	b. 70 ±10 ma. temporarily press momentary TS-352B/U.
	As last indicated, except: TS-352B/U FUNCTION: DIRECT		c. On TS-352B/U, connect red test lead between 50V connector on 20, 000 OHMS PER VOLT range and CKT COM testpoint TP 1301 on pulse generator processor subassembly. On TS-352B/U, connect black test lead between OHMS-DC +AC connector and -30V testpoint TP 1302 on pulse generator processor subassembly.	c. None.
			d. On TS-352B/U, observe voltage indication.	d. -30 +3v.
			e. On pulse generator processor subassembly, remove -30V 1/2A fuse	e. None.
			f. On TS-352B/U, observe no voltage indication.	f. None.
			g. On pulse generator processor subassembly, replace -30 '%A fuse. Observe that BIAS ON indicator lamp DS1301 is lit.	g. None.
3	As last indicated, except: AN/PPM-1A (No. 1) POWER-ON PULSE RATE: 500 pps ATTENUATION: 0 SYNC SELECTOR: X1	As last indicated ------	a. On AN/USM-140B, connect Voltage Divider Probe MX-2817A/U to J1-L test point (TP6) on test fixture TF 119849 and observe pulse pair. At AN/PPM-1A (No. 1 and No. 2), adjust as necessary for peak amplitude of	a. None. 30v.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	POLARITY: POS PULSE LENGTH: 1 μsec AMPLITUDE: 55 POS OR NEG: POS PULSE POSITION: 0 *AN/PPM-1A (No. 2)* POWER: ON PULSE RATE: 500 pps ATTENTUATION: 0 SYNC SELECTOR: POS POLARITY: POS PULSE LENGTH: 1 μsec AMPLITUDE: 55 POS OR NEG: POS PULSE POSITION: 30 μsec *AN/USM-140B* POWER: ON ASTIGMATISM: midposition FOCUS: midposition INTENSITY: midposition SCALE LIGHT: fully cw CHANNEL A CHANNEL B: CHANNEL A VER-_ CHANNEL A VER-TICAL POSITION: midposition POLARITY: +UP SENSITIVITY: 1 VERNIER: CALIBRATED AC-DC: DC None. HORIZONTAL POSITION: midposition HORIZONTAL DISPLAY INTERNAL SWEEP MAGNIFIER: X1 EXTERNAL VERNIER: CAL AC-DC: DC SWEEP TIME: 5 VERNIER: CAL TRIGGER SLOPE: as desired		*b.* On AN/PPM-1A (No. 2), adjust PULSE POSITION control for 30 μsec delay between pulses from AN/PPM-1A (No. 1) and AN/PPM-1A (No. 2) as indicated on AN/USM-140B. c. OnUSM-140B, move MX-2817A/U probe from fixture TF 119849 to SLS test point TP 1304 on pulse generator subassembly; observe that no pulse is displayed. *d.* On AN/USM-140B, remove MX-2817A/U from SLS test point TP 1304 and connect to P2 MOD test point TP 1305 on pulse generator processor subassembly; observe that no signal is displayed. *e.* On AN/USM-140B, remove MX-2817A/U from P2MOD test point TP 1305 and connect to CP test point TP1306; observe no signal is displayed. f. On TS-352B/U, connect black test lead between 50V connector on 20, 000 OHMS PER VOLT range and CP test point TP1306. On TS-352B/U, connect red test lead between OHMS -DC AC connector and ground. Observe voltage reading. *g.* On pulse generator processor subassembly, insure that BIAS ON indicator DS1301 is lit (POWER switch S1301 at ON). *h.* On test fixture TF 119849, place LOAD-GROUNDED-OPEN switch to GROUNDED and observe that BIAS ON indicator DS1301 is extinguished. Remove TS-352B/U connections. *i.* On TS-352B/U, connect black test lead between OHMS-DC _AC connector and ground on TF 119849. Connect red test lead between 250V connector on	b. None. c. None. *d.* None. e. None f. -19 ±2v. g. None. On test fixture TF 119849, h. *i.* +240 +10v.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	TRIGGER LEVEL: as desired TRIGGERSOURCE: EXT. AC SWEEP MODE: PRESET: Remaining controls may be in any position. *TF 119849* LOAD-GROUNDED-OPEN: LOAD +250V: OFF -30V: ON		20, 000 OHMS PER VOLT range and test point J1-C on TF 119849. *j.* On AN/USM-140B, move point TP1306 and connect to J1-L test point TP6 on test fixture TF 119849. Observe *k.* On test fixture TF 119849, place LOAD-GROUND-OPEN switch to OPEN and observe that BIAS ON ind- extinguished. Repeat steps 3i and j above. Observe that results are same. *m.* On pulse generator processor subassembly, remove AC 1/2A SLO BLO fuse and observe that no voltage is indicated on TS-352B/U. *n.* On test fixture TF 119849, p l a c e L O A D-GROUNDED-OPEN switch to LOAD. o. On pulse generator processor subassembly, replace AC 1/2A SLO BLO fuse and remove +250V V8A fuse. On test fixture TF 119849, place +250V switch to ON. *p.* On TS-352B/U, remove red test lead from J1-C test point TP7 on test fixture TF 119849 and connect to +250V test point TP1303 on pulse generator processor subassembly. On TS-352B/U, observe that no voltage is indicated. *q.* On pulse generator processor subassembly, replace +250V V8A fuse. On TS-352B/U, observe that +250v is indicated.	j. None. MX-2817A/U from CP test that no pulse is present. *k.* None. icator DS1301 is *l.* As indicated in 3i and j above. *m.* None. n. None. o. None. *p.* None. *q.* +250 +30v.
4	As last indicated ---- *Pulse generator processor subassembly* SLS switch	As last indicated, except: fully ccw. On pulse generator processor subassembly, rotate CP DELAY ADJ control	a. On pulse generator processor LAY ADJ control R1315 R1343 fully cw.	a. None. subassembly, rotate P2 DE-

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			b. On AN/USM-140B, remove MX-2817A/U from J1-L test point TP6 on test fixture TF 119849 and connect to SLS test point TP1304 and pulse generator processor subassembly. On AN/USM-140B, observe that pulse pair is displayed.	b. None.
	As last indicated, except: CHANNEL A SENSITIVITY: 2 (with 101 ratio of MX-2817A/U), 2 is equivalent to 20 volts/cm) SWEEP TIME: 1 CHANNEL A-CHANNEL B: ALTERNATE	As last indicated------	*c.* On AN/USM-140B, remove MX-2817A/U from SLS test point TP 1304 and connect *to* CP test point TP 1306 on pulse generator processor subassembly. On AN/USM-104B, at CHANNEL A INPUT, observe that amplitude of pulse displayed	c. None. is 55v peak min.
			d. On AN/USM-140B, connect second MX-2817A/U between CHANNEL B INPUT and UG-274/U T-connector at PULSE OUT connector on AN/PPM-1A (No. 1).	*d.* None.
			e. On AN/USM-140B, observe delay of second pulse (leading edge of control pulse) displayed to leading edge of pulse from AN/PPM-1A (No. 1) is 2.8 μsec min.	*e.* None.
			f. On AN/USM-140B, remove MX-2817A/U from CP test point TP 1306 and connect to P2 MOD test point TP 1305.	*f.* None.
	As last indicated, except-: *AN/USM-140B* CHANNEL A SENSITIVITY: (VOLTS/CM) 10	As last indicated------	*g.* OnAN/USM-140B, at CHANNEL A INPUT observe that amplitude of (P2 MOD) pulse is 180v peak min.	g. None.
			h. On AN/USM-140B, observe that delay of second pulse (leading edge of P2 MOD) displayed to leading edge of pulse from AN/PPM-1A (No. 1) is 1.5 μsec max.	*h.* None.
			i. On pulse generator processor subassembly, rotate P2 DELAY ADJ control R1315 fully cw and CP DELAY ADJ control R1343 fully ccw.	i. None.
			j. On AN/USM-140B, observe that delay of second pulse (leading edge of P2 MOD) displayed to leading edge of pulse from the AN/PPM-1A (No. 1) is 2.8 μsec min.	j. None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			k. OnAN/USM-140B, at CHANNEL A INPUT move MX-2817A/U from P2 MOD test point TP 1305 to CP test point TP 1306.	*k.* None.
			l. On AN/USM-140B, place CHANNEL A SENSITIVITY control to 2 and at CHANNEL A INPUT, observe that delay of second pulse (leading edge of control pulse) displayed to leading edge of pulse from the AN/PPM-1A (No. 1) is 1.5 μsec max.	*l.* None.
			m. OnAN/USM-140B, at CHANNEL B INPUT disconnect MX-2817A/U from UG-274B/U T-connector on PULSE OUT connector of AN/PPM-1A (No. 1), and connect to P2 MOD test point TP1305 on pulse generator processor subassembly.	m. None.
			n. On AN/PPM-1A (No. 1), disconnect UG-201A/U connector adapter from PULSE OUT connector. On AN/USM-104B, place CHANNEL B SENSITIVITY control to 10 and observe pulse pair is not displayed.	*n.* None.
			o. On AN/PPM-1A (No. 1), reconnect UG-201A/U on PULSE OUT connector. On AN&USM-140B, at CHANNEL A INPUT move MX-2817A/U from CP test point TP 1306 and connect to UG-274B/U T-connector on PULSE OUT connector at AN/PPM-1A (No. 1). On AN/USM-140B, place CHANNEL A SENSITIVITY control to 1.	o. None.
			p. On pulse generator processor subassembly, adjust P2 DELAY ADJ control R1315 for correct delay referenced to pulse from AN/PPM-1A (No. 1) as indicated on AN/USM-140B.	*p.* 1.9 μsec.
			q. On AN/USM-140B, place CHANNEL B SWEEP TIME control to 5. On pulse generator processor subassembly, adjust P2 PULSE WIDTH ADJ control for correct pulse width as indicated on AN/USM-140B.	q. 0.8 μsec (50% amplitude points between 10 and 90% of rotation).

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			r. OnAN/USM-140B,set SWEEP TIME control to 1, and TRIGGER SOURCE control to INT. Observe pulse rise time at P2 MOD test point TP 1305 at CHANNEL B INPUT.	r. 0.2psecmax.
	As last indicated, except: *AN/USM-140B* CHANNEL A-ALTERNATE CHANNEL A SENSITIVITY: 2 SWEEP TIME: .5 TRIGGER SOURCE: EXT	As last indicated ------	s. OnAN/USM-140B,at CHANNEL A INPUT, move MX-2817A/U from AN/PPM-1A (No. 1) and connect to CP test point TP 1306 on pulse generator processor subassembly. *t.* On pulse generator processor subassembly, adjust CP DELAY ADJ control R1343 to pulse (control pulse) coincident with trailing edge of P2 MOD pulse (slight pulse pulling as R1343 is adjusted is permissible).	s. None. t. None. make trailing edge of second
	As last indicated, except: *AN/USM-140B* CHANNEL A-CHANNEL B: CHANNEL A TRIGGER SOURCE INT SWEEP TIME: 2	As last indicated. -----	u. OnAN/USM-140B, at CHANNEL A INPUT, observe pulse displayed for rise and falltimes and pulse width.	*u.* 0.3 μsec max rise time and falltime; 1.2 ±0.2 μsec pulse width (50% amplitude points; if pulse jitters, measure leading jitter edge of pulse rise to leading jitter edge of pulse fall).
5	*ALL TEST EQUIPMENT* POWER: OFF		Remove power and disconnect test equipment shown in figure 6-9.	None.

6-18. Receiver-Transmitter, Radio RT-264D/UPX-6, General Support Testing

For information pertaining to the testing of Receiver-Transmitter, Radio RT-264D/UPX-6, refer to TM 11-5895-245-35.

6-19. Antenna AS-1796/GPA-119, Physical Test and Inspection 6-48

a. Test Equipment and Materials Required. Light Assembly, Electrical MX-1292/PAQ.

b. Test Connections and Conditions (fig. 6-10). Make no connections to equipment during these tests. The check for moisture-fungusproof (MFP) varnish will be made after repair and before reassembly. Connect MX-1292/PAQ to a 117 vac power source and install wideband transmission filter.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1 All assemblies should be free	None	None	***a.*** **Inspect mechanical assemblies for physical damage.** ***b.*** **Inspect cable connectors for evidence of damage or looseness.** **c. Inspect wiring for condition of insulation.** ***d.*** **Inspect metal surfaces for condition of finish and panel markings.** ***Note.*** **Touchup painting is recommended in lieu of refinishing whenever practicable.**	**On AS-1796/GPA-119, in-** ***a.*** **of dents, bends, and cracks.** **b. Connector should be physically undamaged and securely mounted to chassis.** **c. Insulation should be free from cracks or fraying.** ***d.*** **All metal surfaces intended to be painted must not show bare metal. Panel markings should be legible.**
2	***MX-1292/PAQ*** **245V for M.V. lamps: ON**	***AS-1796/GPA-119***	***a.*** **On AS-1796/GPA-119, expose nameplate to direct rays of MX-1292/PAQ.** ***Note.*** **Polyurethane coating glows grayish-blue when exposed to rays.** ***b.*** **On AS-1796/GPA-119, expose RF switch S1001 and remaining antenna chassis to Direct rays of MX-1292/PAQ.** **originally** ***c.*** **On MX-1292/PAQ, turn off ac power and disconnect.**	***a.*** **The nameplate should be completely covered with polyurethane coating.** ***b.*** **There should be no evidence of polyurethane coating on any surfaces.** ***Note.*** **Do not apply a polyurethane coating to surfaces not finished with polyurethane coating.** **c. None.**

6-20. Antenna AS-1796/GPA-119 VSWR Test

a. Test Equipment and Materials Required.

(1) Adapter, Connector UG-201A/U.

(2) Signal Generator AN/URM-64A.

(3) Slotted Line Coaxial IM-92/U (with crystal detector 1N23B).

(4) Frequency Meter FR-146/U.

(5) Video Cable CG-409E/U.

(6) Indicator, Standing Wave Ratio AN/UPM-108.

(7) Dummy Load, Electrical DA-265/U.

b. Test Connections and Conditions. Install Antenna AS-1796/GPA-119 at a selected site facing an open area clear of RF reflections. This test includes a vswr measurement of bar hybrid HY1001.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	*AN/URM-64A* POWER: ON Sync Selector: RATE X10 PULSE WIDTH:	*AS-1796/GPA-119-* except: Backfill E1002 hybrid	*a.* Complete test equipment reflector and bar HY1001	*a.* None. connections shown in figure 6-10. *b.* Apply 117 vac power to test
b.	None. max cw PULSE RATE: 100 ZERO SET: Adjust for centerline indication on panel meter.	not included.	equipment and allow 5 min for stabilization. c. OnAN/URM-64A,place SIGNAL FREQUENCY control to 1030 on MC dial. *d.*	*c.* 1030 +2MHz. On AN/URM-64A, rotate *d.*
Midrange.	PULSE DEL AY:.3 *AN/UPM--108* BOLO BIAS CURRENT: LOW POWER: ON INPUT SELECTOR: XTAL 200 ohms		OUTPUTATTENUATOR for midscale indication as observed on AN/UPS-108. *e.* On FR-146/U, rotate FREQUENCY control for direct reading of 1030 MHz. *f.*	*e.* 1030 +2 MHz On AN/URM-64A, slowly *f.*
None.	RANGE: 30 db METER SCALE: NORMAL		rotate SIGNAL FREQUENCY until dip is observed on AN/UPM-108. *g.* On FR-146/U, detune FREQUENCY control. *h.* On IM-92/U, adjust slide for midrange indication on 30 db RANGE scale of AN/UPM-108. *i.* OnAN/UPM-108,place RANGE control to 20. *j.* On IM-92/U, adjust probe depth and tuning knob as required (para *15b* through *d* TM 11-5109). *Note.* If necessary, vary VERNIER GAIN on AN/UPM-108, while maintaining min probe depth on IM-92/U. *k.* On IM-92/U, slide carriage probe in one direction for max relative amplitude indication on AN/UPM-108. *l.* OnAN/UPM-108, rotate VERNIER GAIN control for full scale meter deflection. *m.* On IM-92/U, slide carriage in one direction until one minimum indication is observed on AN/UPM-108. *n.* Observe voltage indicated at E1001-A (side 1) on AN/UPM-108 (fig. 6-10).	*g.* None. *h.* None. *i.* None. *j.* Meter indication 1. *k.* None. *l.* Meter indication 1. *m.* None. *n.* Side 1 max vswr should be 1.7:1 or less at 1030 MHz.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
2	As last indicated---	As last indicated ------	*a.* On IFF antenna E1001, move CG-409A/U and UG-201A/U (fig. 6-10) from connector E1001-A (side 1) to connector E1001-B (side 2).	a. None.
			b. On IM-92/U, slide carriage probe in one direction for max relative amplitude indication.	*b.* None.
			c. OnAN/UPM-108, rotate VERNIER GAIN control until full scale meter deflection is observed.	c. Meter indication 1.
			d. On IM-92/U, slide carriage *d* in one direction until one min indication is observed on AN/UPM-108.	*d.* None.
			e. Observe voltage indicated at E1001-B (side 2) on AN/UPM-108.	*e.* Side 2 max vswr is 1.7:1 or less at 1030 MHz.
3	As last indicated---	*AS-1 796/GPA—119* except: backfill reflector E1002 not included.	*a.* Connect test equipment as shown in fig. 6-11 for sum channel vswr measurement.	*a.* None.
			b. On IM-92/U, slide carriage probe in one direction for max relative amplitude indication on AN/UPM-108.	*b.* None.
			c. OnAN/UPM-108, adjust VERNIER GAIN control for full scale meter deflection.	c. Meter indication.
			d. On IM-92/U, slide carriage in one direction until min voltage indication is observed on AN/UPM-108.	*d.* None.
			e. On AN/UPM-108, observe voltage indicated.1.7:1 or less at 1030 MHz.	e. Sum channel max vswr is
4	As last indicated	*AS--1796/GPA—119* Including backfill reflector E1002	*a.* Connect test equipment as shown in fig. 6-12 for difference channel vswr: (including backfill reflector E1002).	*a.* None.
			b. On IM-92/U, slide carriage probe in one direction for max relative amplitude indication on-AN/UPM-108.	*b.* None.
			c. OnAN/UPM-108, adjust VERNIER GAIN for full scale meter deflection.	*c.* Meter indicates 1.
			d. On IM-92/U, slide carriage in one direction until min voltage indication is observed on AN/UPM-108.	*d.* None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			e. Observe voltage indicated on is AN/UPM-108.	*e.* Difference channel max vswr 1.7.1 or less at 1030 MHz.
5	*ALL TEST EQUIP-MENT* POWER: OFF		Disconnect all test equipment and restore as-1796/GPA-119 to service.	None.

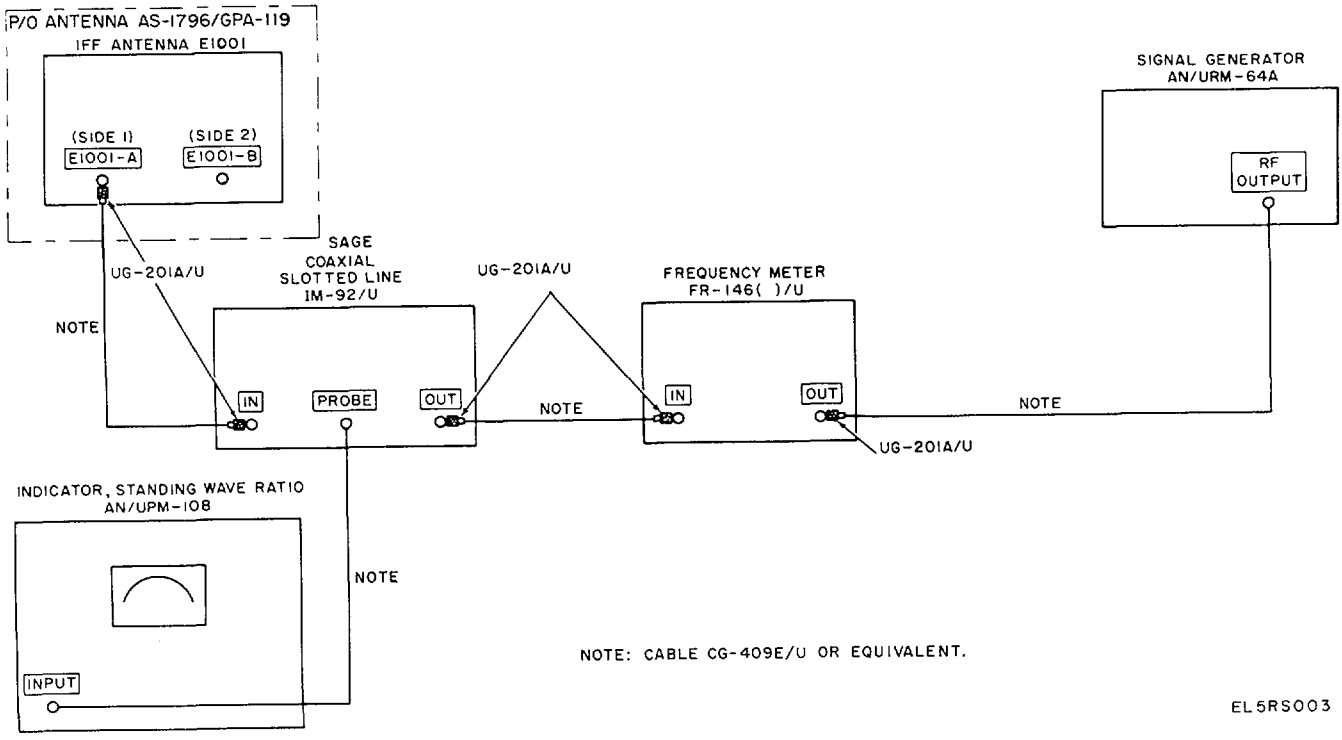


Figure 6-10. Antenna AS--1796/GPA-119, IFF antenna E1001, vswr test connections.

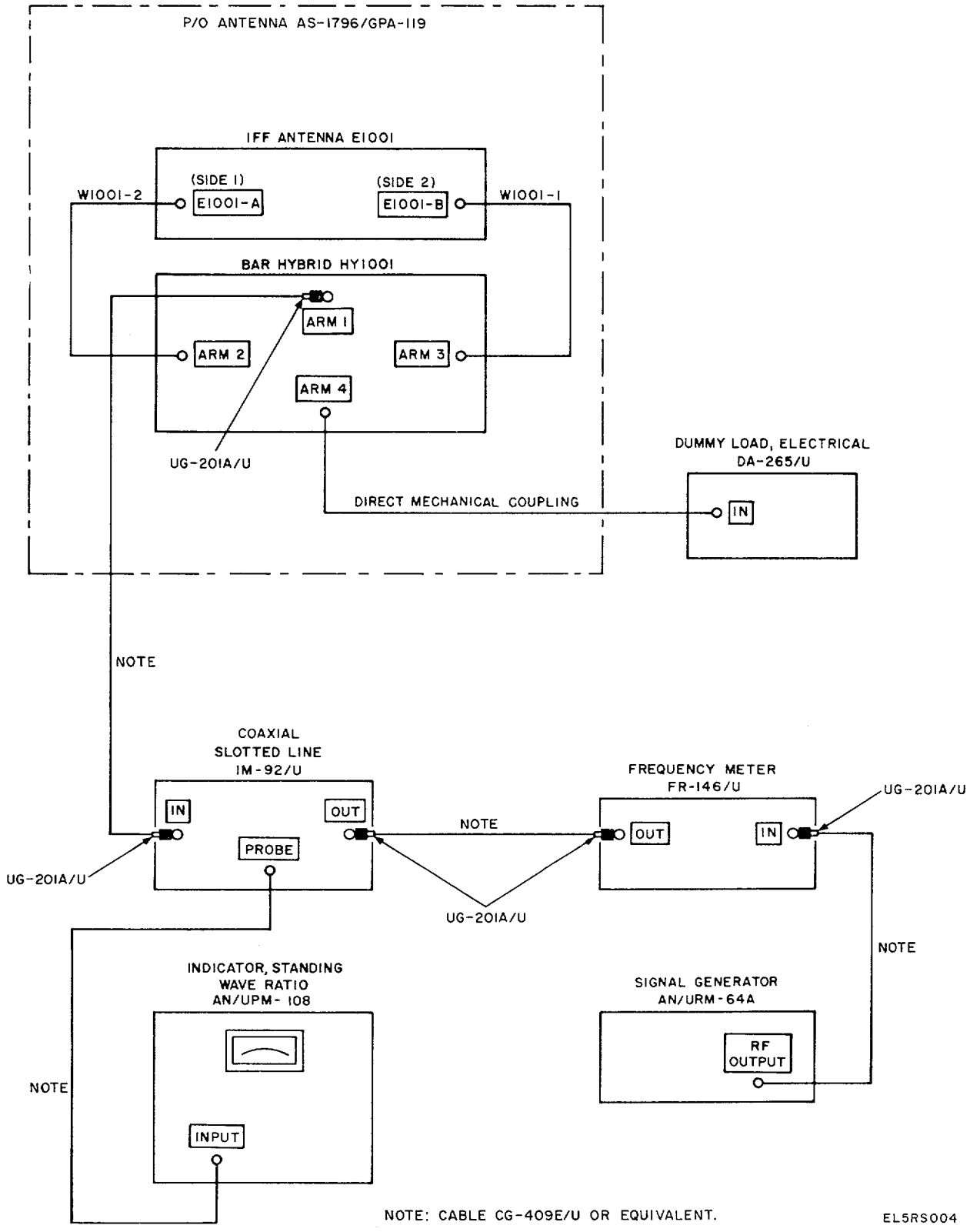


Figure 6-11. Antenna AS-1796/GPA-119, sum channel vswr test connections.

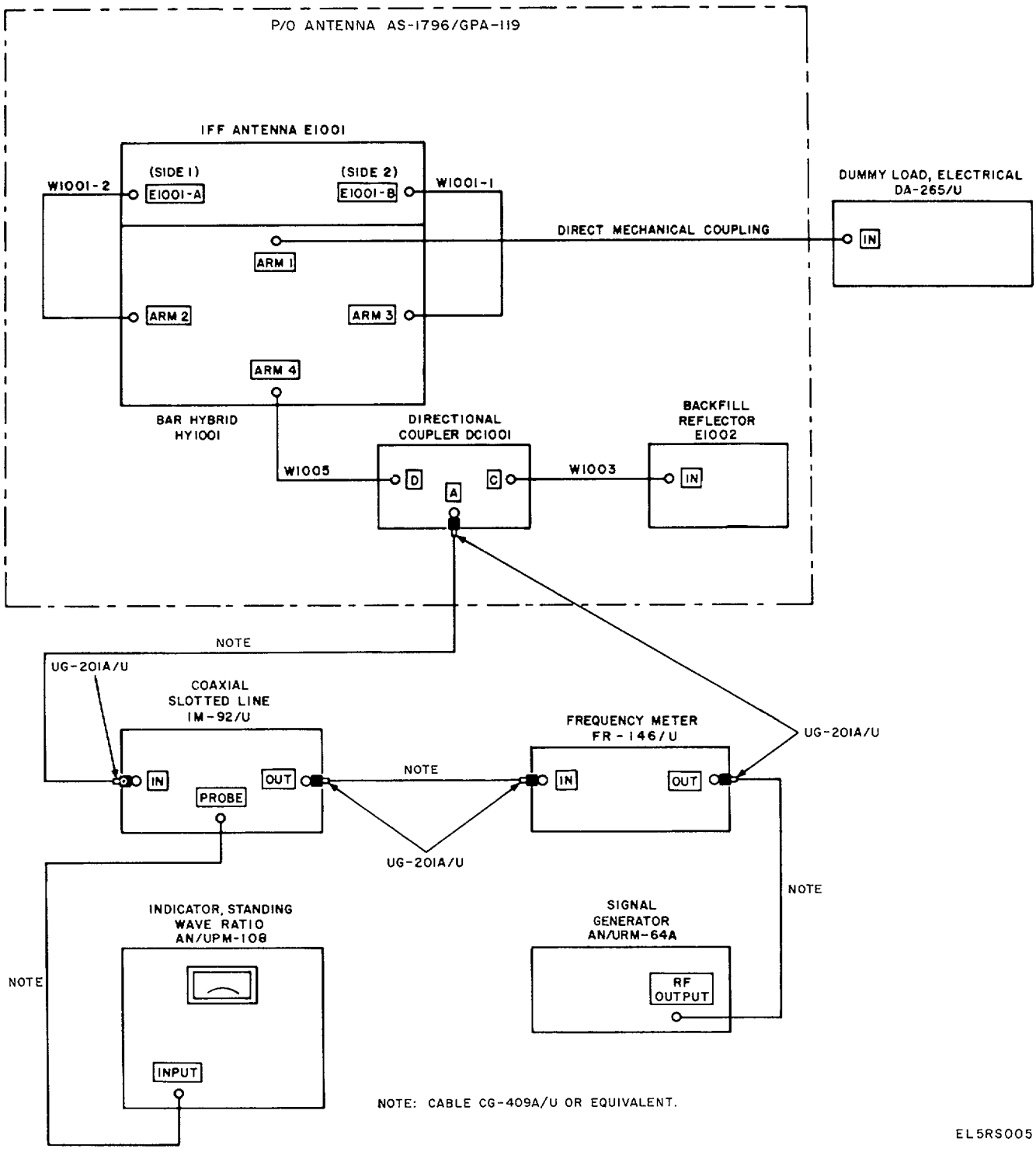


Figure 6-12. Antenna AS-1796/GPA-119, difference channel vswr test connections.

6-21. Pedestal Antenna AB-1158/ GPA1 19, Rotary Coupler E20001 VSWR Test

a. Test Equipment Required.

(1) Adapter, Connector UG-210A/U.
(2) Signal Generator AN/URM-64A.
(3) Slotted Line Waveguide IM-92/U (with crystal detector 1N23B).
(4) Frequency Meter FR-146/U.
(5) Video Cable CG-409/U.
(6) Indicator, Standing Wave Ratio AN/UMP-108.
(7) Dummy Load, Electrical DA-265/U.

b. Test Connections and conditions.

(1) Remove rotary coupler E20001 from Pedestal, Antenna AB-1158/GPA-119.
(2) Connect Equipment as shown in figure 6-13.

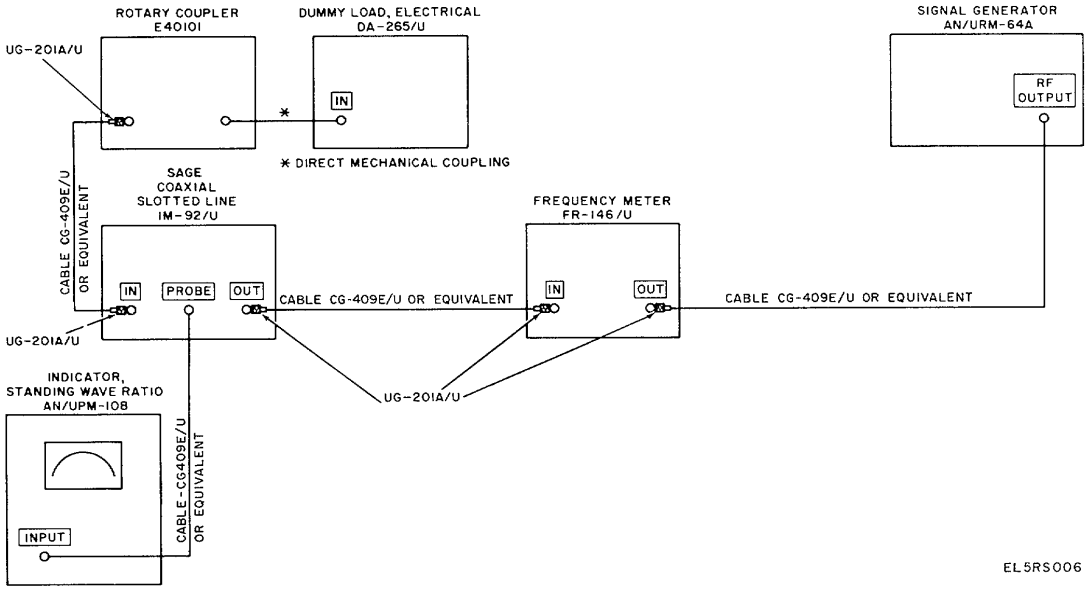


Figure 6-13. Pedestal Antenna AB-1158/GPA-119, rotary coupler E20001 vswr test connections.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	***AN/URM-640A*** ***POWER: ON*** **Sync Selector:** **RATE X10** **PULSE RATE: 100** **PULSE WIDTH** **max cw**	***Rotary coupler E20001***	***a.*** **Apply 117 vac power to test equipment and allow 5 min for stabilization.** ***b.*** **On AN/URM-64A, place SIGNAL FREQUENCY control to 1030 on MC dial.**	***a.*** **None.** ***b.*** **None.**

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	ZERO SET: Adjust for centerline indication on panel meter. POWER SET: Adjust for zero db indication on panel meter. PULSE DELAY: .3 *AN/UPM-108* BOLO BIAS CURRENT:LOW POWER: ON INPUT SELECTOR: BOLO 200 OHMS RANGE: 30 db METER SCALE: normal		*c.* On AN/URM-64A, rotate OUTPUTATTENUATOR for midscale indication as observed on AN/UPM-108. *d.* On Frequency Meter FR-1461U rotate FREQUENCY control for direct reading of 1030 MHz. *e.* On AN/URM-64A, slowly rotate SIGNAL FREQUENCY until dip is observed on AN/UPM-108. f. On FR-146/U, detune FREQUENCY control. g. On IM-92/U, adjust slide for midrange indication on 30-db RANGE scale of AN/UPM-108. *h.* On IM-92/U, adjust probe depth and tuning knobs as required (para 15b through *d* TM 11-5109). *Note.* If necessary, vary VERNIER GAIN on AN/UPM-108, while maintaining min probe depth on IM-92/U. *i.* On IM-92/U, slide carriage probe in one direction for ¾ max relative amplitude indication on AN/UPM-108. *j.* OnAN/UPM-108, rotate VERNIER GAIN control for full scale meter deflection. *k.* On IM-92/U, slide carriage in one direction until one min indication is observed on AN/UPM-108. *l.* Observe voltage ratio (vswr) of max to min voltage indicated on AN/UPM-108.	*c.* Midrange. *d.* None. e. None. f. None. g. None. *h.* Meter indicates 1. *i.* None *j.* Meter indicates 1. *k.* None. *l.* Rotary coupler E20001 max vswr should be 1.7:1 at 1030 MHz.
2	As last indicated --	As last indicated ------	a. On AN/URM-64A,place SIGNAL FREQUENCY control to 190 on MC dial. *b.* On AN/URM-64A, rotate OUTPUT ATTENUATOR for midscale indication as observed on AN/UPM-108. c. On FR-146/U, rotate FREQUENCY control for direct reading of 1090 MHz. *d.* On AN/URM-64A, slowly rotate SIGNAL FREQUENCY until dip is observed on AN/UPM-108.	a. None. *b.* Midrange. c. None. *d.* None.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
		e.	On FR-146/U, detune FREQUENCY control.	*e.* None.
			f. On IM-92/U, adjust slide for midrange indication on 30-db RANGE scale of AN/UPM-108.	*f.* None.
			g. On IM-92/U, adjust probe depth and tuning knob as required (para 15b through *d* TM 11-5109). *Note:* If necessary, vary VERNIER GAIN on AN/UPM--108, while maintaining min probe depth on IM-9 2/U.	*g.* Meter indicates 1.
			h. On IM-92/U, slide carriage probe in one direction for max relative amplitude indication of AN/UPM-108.	*h.* None.
			i. OnAN/UPM-108rotate VERNIER GAIN control until full scale deflection is observed.	*i.* Meter indicates 1.
			j. On IM-92/U, slide carriage in one direction until one min indication is observed on AN/UPM-108.	*j.* None.
			k. Observe voltage ratio (vswr) of max to min. voltage indicated on AN/UPM-108.	*k.* Rotary coupler E20001 max vswr is 1.7:1 at 1090 MHz.
3	*ALL TEST EQUIPMENT* POWER: OFF		Disconnect all test equipment and restore rotary coupler E20001 to service.	None.

6-22. Decoder, Video KY-593/TPX-44, General Support Testing

For information pertaining to the testing of Decoder, Video KY-593/TPX-44, refer to TM 11-5840-309-35.

6-23. Control, Remote Switching C-7014/ TPX-44, General Support Testing

For information pertaining to the testing of Control, Remote Switching C-7014/TPX-44, refer to TM 11-5840-309-35.

6-24. Simulator, Radar Signal SM-472/ TPX-44, General Support Testing

For information pertaining to the testing of Simulator, Radar Signal SM-472/TPX-44, refer to TM 11-5840-326-35.

6-25. Interconnecting Box J-2945/ TPX-41, Physical Test and Inspection

a. Test Equipment and Materials Required. Light Assembly, Electrical MX-1292/PAQ.

b. Test Conditions and Connections.

(1) All external cables disconnected and side panel removed.

(2) Connect MX-1292/PAQ to a 117-vac power source and install wideband transmission filter.

c. Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1		*a.*	Operate front panel switches through all positions.	*a.* Switches should operate smoothly, without sticking or binding.
			b. Inspect front panel hardware for completeness.	*b.* Hardware should be complete.
			c. Inspect front panel switches and controls for evidence of looseness.	*c.* Switches and controls should be securely mounted.
			d. Inspect connectors J8601, J8602, and J8603 for evidence of damage or looseness.	*d.* Connectors should be physically undamaged and mounted securely to chassis.
			e. Inspect wiring for condition of insulation.	*e.* Insulation should be free from cracks or fraying.
			f. Inspect metal surfaces for condition of finish and panel markings.	*f.* All metal surfaces intended to be painted must not show bare metal. Panel markings should be legible.
			Note. Touchup painting is recommended in lieu of refinishing whenever practicable.	
2	*MX-1292/PAQ* 245V for M.V. lamps: ON	*J2945/TPX-41*	*a.* On J2945/TPX-41, expose chassis to direct rays of MX-1292/PAQ. Inspect components, wiring, and chassis surfaces for evidence of polyurethane coating. Inspect connectors, switch contacts, and jacks for absence of polyurethane coating.	*a.* All components, wiring, and chassis surfaces should be completely covered with MFP varnish. There should be no evidence of MFP on Connector and switch contacts.
			Note. Polyurethane coating glows grayish-blue when exposed to rays of MX-1292/PAQ.	*Note.* Do not apply polyurethane coating to parts not originally finished with polyurethane.
			b. On MX-1292/PAQ, turn off ac power and disconnect.	b. None.

CHAPTER 7

DEPOT MAINTENANCE

Section I. GENERAL

7-1. Scope of Depot Maintenance

Specific maintenance duties of the depot maintenance repairman are listed in a through *d* below with references to the paragraphs covering the specific maintenance function. In addition to these duties, the depot maintenance repairman is also responsible for equipment overhaul which often entails complex rewiring, fabrication, mechanical rework, and other maintenance functions requiring the use of specialized facilities. Ideally, the performance of depot maintenance duties entails only those maintenance operations designated specifically for depot maintenance. However, some equipment problems correctable at the general support level of maintenance may be referred to depot maintenance due to the difficulty involved in identifying the problem. For this reason, the maintenance duties of the depot maintenance repairman also include the maintenance responsibilities of the general support maintenance repairman as described in paragraph 5-1.

a. Troubleshooting (para 7-3).

b. Adjustment and alignment (para 7-4).

c. Repair (para 7-5).

d. Removal and replacement (para 7-6).

7-2. Tools, Test Equipment, and Materials Required

a. Tools. Tools required for depot maintenance are listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

b. Test Equipment. Test equipment required for depot maintenance is listed in the maintenance allocation chart (MAC) in TM 11-5895-479-12.

c. Materials The applicable repair parts allocated for depot maintenance are listed in TM 11-5895-479-35P.

Section II. DEPOT MAINTENANCE TROUBLESHOOTING

7-3. General

This section references pertinent troubleshooting data to aid the depot repairman in the rapid identification and correction of equipment malfunctions. The data consists of information contained in the direct support troubleshooting section of this manual. Specific types of troubleshooting data are listed in a through *i* below with references to the paragraphs providing coverage of each.

a. Troubleshooting techniques (para 3-4).

b. Identification of intermittents (para 3-5).

c. Diagrams (para 3-6).

d. Reference designations (para 3-7).

e. Voltage and resistance measurements (para 3-8).

f. Parts substitution (para 3-9).

g. Waveform analysis (para 3-10).

h. System troubleshooting chart (para 3-11).

i. Major component troubleshooting (para 3-12).

7-4. Adjustment and Alignment Procedures

This paragraph references adjustment and alignment procedures required to insure optimum performance of the major components comprising Interrogator Set AN/TPX-41. These procedures are contained in the direct support adjustment and alignment section of this manual. Each procedure is preceded by a list of test equipment required to perform the procedure and required equipment conditions necessary to accomplish the procedure. Specific adjustment and alignment procedures are listed in a through *n* below with references to the paragraphs containing detailed instructions for the performance of each procedure. Where adjustment and alignment procedures for specific components are covered in separate manuals, the applicable TM is referenced as necessary.

a. Blanker, Interference MX-8795/TPX-41, positive 15-volt power supply adjustment (para 3-14).

b. Blanker, Interference MX-8795/TPX-41, negative 15-volt power supply adjustment (para 3-15).

c. Blanker, Interference MX-8795/TPX-41, timing adjustment (para 3-16).

d. Coder, Control KY-97C/TPX-41, Adjustment and Alignment Procedures (TM 11-5895-201-35).

e. Control, Remote Switching C-1271A/ TPX-22, adjustment and alignment procedures (para 3-18).

f. Modulator, Pulse MD-638/TPX-41, P2 pulse timing adjustment (para 3-20).

g. Modulator, Pulse MD-638/TPX-41, P2 pulse width adjustment (para 3-21).

h. Modulator, Pulse MD-638/TPX-41, control pulse delay adjustment (para 3-21).

i. Receiver-Transmitter, Radio RT-264D/ UPX-6, adjustment and alignment procedures (TM 11-5895-245-35).

j. Antenna Group AN/GPA-119, synchro alignment (para 3-23).

k. Decoder, Video KY-593/TPX-44, adjustment and alignment procedures (TM 11-5940-309-35).

l. Control, Remote Switching C-7014/TPX-44, adjustment and alignment procedures (TM 11-5840-309-35).

m. Simulator, Radar Signal SM-472/TPX-41, adjustment and alignment procedures (TM 11-5840-326-35).

n. Interconnecting Box J-2945/TPX-41, adjustment and alignment procedures (para 3-27).

7-5. Repair Procedures

This paragraph references instructions for performing various repair operations on components of Interrogator Set AN/TPX-41. These instructions are contained in the direct support repair section of this manual. Specific repair operations are listed in a through *d* below with references to paragraphs that provide pertinent instructions for each type of repair operation.

a. Electronic component repair (para 3-29).

b. Mechanical parts repair (para 3-30).

c. Coaxial cable repair (para 3-31).

d. Multiconductor cable repair (para 3-32).

7-6. Removal and Replacement; Disassembly and Reassembly

This paragraph references complete disassembly and reassembly procedures for all major components of Interrogator Set AN/TPX-41. These instructions consist of step-by-step procedures keyed to accompanying illustrations that portray the units, assemblies, and parts of a major component in an exploded view. Before disassembling a major component, study the exploded view and the relationships between the various parts and subassemblies. During disassembly, give particular attention to the assemblage of complex mechanical assemblies. Thorough study will provide for ease of disassembly and serve as an aid during reassembly. Major components of the AN/TPX-41 are listed in a through *l* below, with references to the paragraphs covering disassembly and reassembly of

each. Where disassembly and reassembly instructions for a particular major component are contained in a separate manual, the applicable TM is referenced as necessary.

a. Blanker, Interference MX-8795/TPX-41 (para 3-34).

b. Coder-Control KY-97C/TPX (TM 11-5895-201-35).

c. Control, Remote Switching C-1271A/ TPX-22 (para 3-36).

d. Modulator, Pulse MD-638/TPX-41 (para 3-37).

e. Receiver-Transmitter RT-264D/UPX-6 (TM 11-5895-245-35).

f. Antenna Group AN/GPA-119 (para 3-39).

g. Pedestal, Antenna AB-1158/GPA-119, disassembly and assembly (para 5-7).

h. Antenna AS-1796/GPA-119 (paras 3-41 and 3-42).

i. Decoder, Video KY-593/TPX-44 (TM 11-5840-309-35).

j. Control, Remote Switching C-7014/TPX-44 (TM 11-5840-309-35).

k. Simulator, Radar Signal SM-472/TPX-44 (TM 11-5840-326-35).

l. Interconnecting Box J-2945/TPX-41 (para 3-46).

CHAPTER 8

DEPOT OVERHAUL STANDARDS

Section I. GENERAL

8-1. Description of Depot Overhaul Standards

Depot overhaul standards consist of all tests required to insure rebuilt or repaired equipment meets adequate performance standards prior to reissue or return to stock. The tests that comprise depot overhaul standards for Interrogator Set AN/TPX-41 are covered in section II of this chapter. These tests must be performed to evaluate equipment performance and determine serviceability after equipment overhaul and prior to reissue or return to stock. The tools, test equipment and test fixtures required to perform these tests consist of those allocated to depot maintenance as indicated in maintenance allocation charts (MAC) contained in TM 11-5895-479-12. Each test in this chapter is preceded by a list of test equipment and materials required to perform the test, required equipment conditions necessary to accomplish the test, references to test connection diagrams as applicable, and any special instructions required to perform the test. Instructions for connecting and operating the test equipment required for each test are contained in the respective test procedures. Perform the tests in the order presented and follow the procedural steps of each test in the order given.

8-2. Technical Manual Coverage of Depot Overhaul Standards

a through k below list the major components of Interrogator Set AN/TPX-41 and reference the technical manuals that contain detailed coverage of depot overhaul standards for each.

a. Blanker, Interrogator MX-8795/TPX-41(TM 11-5895-479-35).

b. Coder-Control KY-97C/TPX-41 (TM 115895-201-35).

c. Control, Remote Switching C-1271A/TPX22 (TM 11-5895-479-35).

d. Modulator, Pulse MD-638/TPX-41 (TM 115895-479-35).

e. Receiver-Transmitter, Radio RT-264D/UPX6 (TM 11-5895-245-35).

f. Antenna AS-1796/TPA-119 (TM 11-5895479-35).

g. Pedestal, Antenna AB-1158/TPA-119 (TM 11-5895-479-35).

h. Decoder, Video KY-593/TPX-44 (TM 115840-309-35).

i. Control, Remote Switching C-5014/TPX-44 (TM 11-5840-309-35).

j. Simulator, Radar Signal SM-472/TPX-44 (TM 11-5840-326-35).

k. Interconnecting Box J-2945/TPX-41 (TM 11-5895-479-35).

8-3. Modification Work Orders

Perform all applicable modification work orders pertaining to this equipment before making specified tests. DA Pam 310-7 lists all available MWO's.

Section II. TEST PROCEDURES

8-4. General

This section covers depot overhaul standard testing for Interrogator Set AN/TPX-41. Specific tests that must be performed to insure equipment performance complies with depot overhaul standards are listed in a through aa below with references to the paragraphs containing the detailed test procedures. Where depot overhaul standards for a particular major component are covered in a separate manual, the applicable TM is referenced as necessary. Paragraphs 8-5 through 8-10 contain depot overhaul standard test procedures that require the use of tools, test equipment, and facilities available only to depot level maintenance.

a. Blanker, Interference MX-8795/TPX-41, physical tests and inspection (para 6-3).

b. Blanker, Interference MX-8795/TPX-41, positive power supply regulation test (para 6-4).

c. Blanker, Interference MX-8795/TPX-41, negative power supply regulation test (para 6-5).

d. Blanker, Interference MX-8795/TPX-41, dc voltage test (para 6-6).

e. Blanker, Interference MX-8795/TPX-41, trigger test (para 6-7).

f. Blanker, Interference MX-8795/TPX-41, trigger/gate generator test (para 6-8).

g. Blanker, Interference MX-8795/TPX-41, synchronizer-multiplier test (para 6-9).

h. Blanker, Interference MX-8795/TPX-41, processor test (para 6-10).

i. Blanker, Interference MX-8795/TPX-41, video test (para 6-11).

j. Coder-control KY-97C/TPX, depot overhaul standards (TM 11-5895-201-35).

k. Control, Remote Switching C-1271A/ TPX-22, physical test and inspection (para 6-13).

l. Modulator, Pulse MD-638/TPX-41, physical test and inspection (para 6-14).

m. Modulator, Pulse MD-638/TPX-41, power supply test (para 6-15).

n. Modulator, Pulse MD-638/TPX-41, pulse generator processor output test (para 6-16).

o. Modulator, Pulse MD-638/TPX-41, pulse generator processor test (para 6-17).

p. Modulator, Pulse MD-638/TPX-41, insertion loss test (para 8-5).

q. Receiver-Transmitter, Radio RT-264D/ UPX-6, depot overhaul standards (TM 11-5895-245-35).

r. Antenna AS-1796/GPA-119, physical test and inspection (para 6-19).

s. Antenna AS-1796/GPA-119, vswr test (para 6-20).

t. Antenna AS-1796/GPA-119, pattern test (para 8-7).

u. Antenna AS-1796/GPA-119, gain test (para 8-8).

v. Antenna AS-1796/GPA-119, RF switch S1001 test (para 8-10).

w. Pedestal, Antenna AB-1158/GPA-119, rotary coupler E20001 vswr test (para 6-21).

x. Decoder, Video KY-593/TPX-44, depot overhauls standards (TM 11-5840-309-35).

y. Control, Remote Switching C-7014/TPX-44, depot overhaul standards (TM 11-5840-309-35).

z. Simulator, Radar Signal SM-472/TPX-44, depot overhaul standards (TM 11-5840-309-35).

aa. Interconnecting Box J-2945/TPX-41, physical test and inspection (para 6-25).

8-5. Modulator, Pulse MD-638/TPX-41, Insertion Loss Test

a. Test Equipment.

(1) Signal Generator SG-299/U.
(2) Frequency Meter FR-146/U.
(3) Indicator, Standing Wave Ratio AN/UPM-108.
(4) Sweep oscillator 691A, Hewlett-Packard.
(5) Detector mount 627AM and element 631C, polytechnic research and development.
(6) Attenuator 50-10, (Weinschel (2 required).
(7) Low-pass filter 360B, Hewlett-Packard.

b. Test Connections and Conditions. Connect test equipment as shown in figure 8-1. Leave MD-638/TPX-41 out of circuit by interconnection of attenuators 50-10.

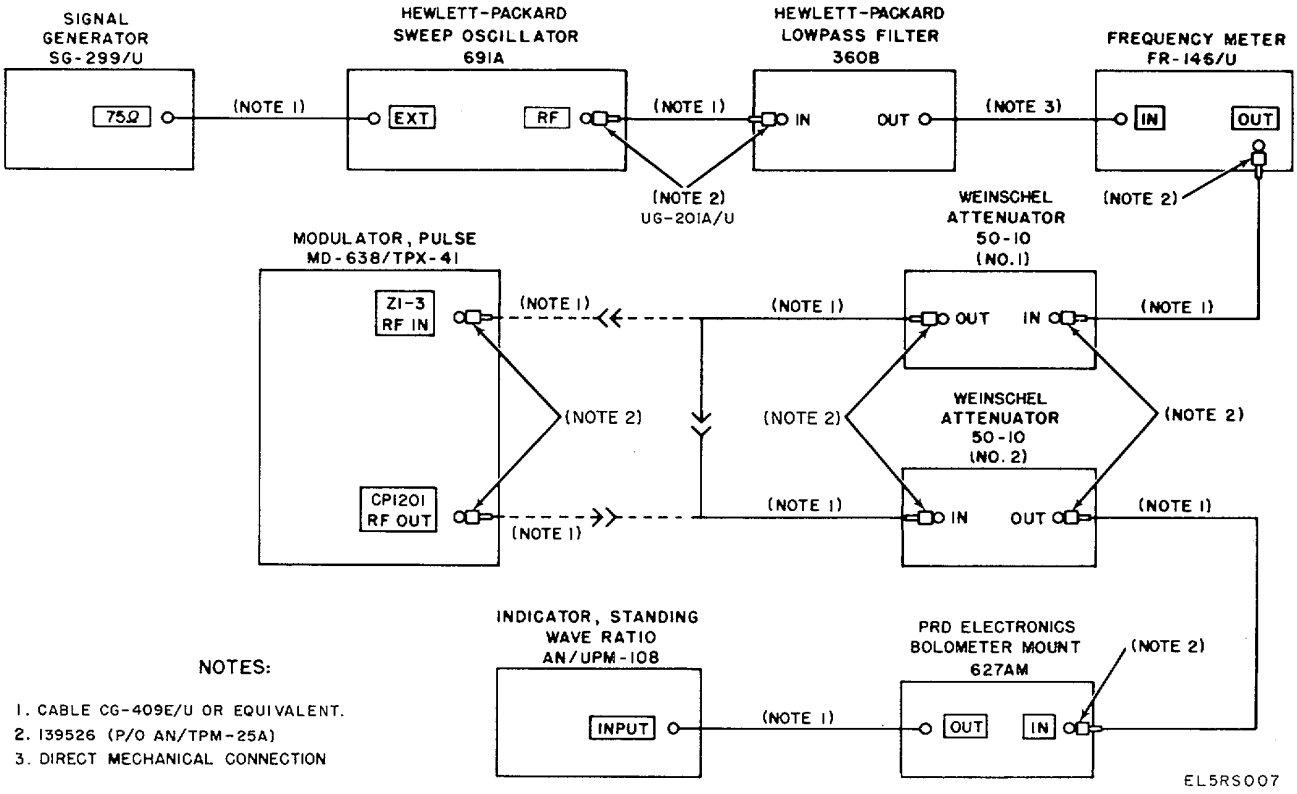


Figure 8-1. Modulator, Pulse MD-638/TPX-41, insertion loss test connections.

c. Procedure.

(1) On MD-638/TPX-41, place POWER switch S1301 to ON.
(2) Apply 117-volt, ac power to: SG-299/U, AN/UPM-108, and HP-691A. Allow 5 minutes for test equipment stabilization.
(3) On HP-691A, set controls as follows:
LINE: RF
SWEEP SELECTOR: cw
POWER LEVEL: fully cw
START /CW: 1.03
FUNCTION: START STOP
AMPL. MOD: EXT AM
(4) On SG-299/U, set controls as follows:
POWER: ON
RANGE: X100
FREQUENCY: 10
ATTENUATION: 20 db

(5) On AN/UPM-108, set controls as follows:

POWER: ON
BOLO BIAS CURRENT: LOW
INPUT SELECTOR: BOLO 200 OHMS
RANGE: 40 db
METER SCALE: NORMAL

(6) On FR-146/U, rotate FREQUENCY control to 1030 MHz.

(7) On HP-691A, adjust POWER LEVEL control to obtain midrange indication on AN/ UPM-108.

NOTE

On AN/UPM-108, adjust VERNIER control as required to maintain midrange indication during this step.

(8) On HP-691A, adjust START/CW control until meter indicates dip on AN/UPM-108. Observe frequency is 1030 +2 MHz.

(9) On AN/UPM-108, adjust VERNIER control for maximum scale meter deflection. Observe indication is zero db.

(10) On FR-146/U, rotate FREQUENCY control off 1030 MHz.

(11) On MD-638/TPX-41, check for proper alignment and tightness of cable connectors on diplexer Z1201.

(12) On attenuator 50-10, remove connection between 50-10 (No. 1 and No. 2); and on MID-638/TPX-41, connect 50-10 (No. 1) to RF IN connector Z1201-3, and 50-10 (No. 2) to RF OUT connector CP1201.

(13) On AN/UPM-108, observe insertion loss of MD-638/TPX-41 at 1030 MHz is less than 1.25 db maximum.

(14) Repeat step (1) above.

(15) On HP-691A, place START/CW control to 1.09.

(16) On FR-146/U, rotate FREQUENCY control to 1090 MHz.

(17) On HP-691A, adjust POWER LEVEL control to obtain midrange indication on AN/ UPM-108.

NOTE

On AN/UPM-108, adjust VERNIER control as required to maintain midrange indication during this step.

(18) On HP-691A, adjust START/CW control until meter on AN/UPM-108 indicates a dip at 1090 +2 MHz.

(19) On AN/UPM-108, adjust VERNIER control for maximum scale meter deflection. Observe indication is zero db.

(20) On FR-146/U, rotate FREQUENCY control off 1090 MHz.

(21) On MD-638/TPX-41, check for proper alignment and tightness of cable connectors on diplexer Z1201.

(22) On 50-10 (No. 1 and No. 2), remove connections; and on MD-638/TPX-41, connect 50-10 (No. 1) to RF IN connector Z1201-3, and 50-10 (No. 2) to RF OUT connector CP1201.

(23) On AN/UPM-108, observe that insertion loss of MD-638/TPX-41 at 1090 MHz is less than 1.25 db maximum.

(24) Remove ac power from equipment and return MD-638/TPX-41 to service.

8-6. Antenna System Test Range

a. General. The test procedures contained in paragraphs 8-7 and 8-8 are performed on Antenna AS-1796/GPA-119 at a test range.

Special facilities and permanent test mount apparatus required to perform antenna range tests are described in b below. These facilities and devices are required in addition to test equipment described in each test procedure.

b. Tower and Test Mount Requirements. Test procedures for antenna measurements require the use of a transmitting tower and a receiving tower. The transmitting tower contains an L-band radar transmitter, and L-band transmitting antenna reflector and feed assembly, and a universal bearing

mount with the capability of remote, three-axis adjustment. The receiving tower contains an azimuth-over elevation positioner, Scientific- Atlanta model 5303-1; a positioner control unit, Scientific-Atlanta model 4112; and cables, Scientific-Atlanta number 5051-12 necessary for pattern measurements. A description of the transmitting and test mount equipment follows:

(1) The distance between the transmitting tower and receiving tower should not be less than 200 feet. This distance will accommodate antennas up to 10 feet in length.

(2) The vertical size of the transmitting antenna used determines the minimum height of both towers. The minimum height of the towers is calculated by dividing 100 by the vertical dimension (in feet) of the transmitting antenna. For example, if the vertical dimension of the transmitting antenna is 5 feet, the towers should be at least 20 feet in height.

(3) The area between and around the towers must be free of interfering objects such as buildings, telephone or powerlines, or fences which could reflect microwave signals. The test site should avoid strong sources of radio frequency interference.

(4) Transmitter power and transmitter antenna gain must be sufficient to provide adequate one-way signal to investigate the side lobe structure of the antenna under test. An L-band transmitter with an average power of 5 watts or more is required.

(5) The azimuth-over elevation positioner, SA model 5303-1 supports and simulates the scanning action of the AS-1796/GPA-119 during antenna measurements. It must be long and strong enough for solid antenna support. It must be capable of rotating at least 180 degrees right and left in the horizontal plane and at least 30 degrees (from level) in the vertical plane. It must have an easily readable horizontal and vertical protractor to indicate position, accurate to 0.1 degree. It must have handwheel for adjustment (in both planes), and appropriate gears to permit maximal rotation. Positioner control unit, SA model 4112 remotely actuates drive motors for horizontal and vertical slew, and synchros for azimuth position data to operate the associated Recorder Set, Radiation Pattern, Radio Frequency AN/GPM-45. All gears should be spring-loaded to eliminate backlash and to provide rotation accuracy within 0.001 inch.

(6) The AS-1796/GPA-119 with RF switch S1101 removed must be securely fastened to the azimuth-over elevation positioner (SA model 5303-1) with the centerline directly above the azimuth rotational center.

8-7. Antenna AS-1796/GPA-119, Pattern Test

a. Test Equipment.

(1) Transmitting equipment. Power oscillator, Airborne Instrument Labs, model 124C.

(2) Receiving equipment.

Azimuth-over elevation positioner, Scientific-Atlanta model 5303-1.

Dc block, Sage model 505.

Positioner control unit, Scientific-Atlanta model 4112

Frequency Meter FR--146/U.

Dummy Load, Electrical DA-265/U.

Detector mount, PRD model 627AM, and element, PRD model 631C.

Cables, Scientific-Atlanta number 5051-12;

Indicator, Standing Wave Ratio AN/ UPM-108 Adapter, Connector UG-201A/U.

Recorder Set, Radiation Pattern, Radio Frequency AN/GPM-45.

Cable, Radio Frequency CG-409E/U.

b. Test Connections and Conditions.

(1) On SA 5303-1, assemble Antenna AS1796/GPA-119 on adapter with long dimension in the horizontal direction.

(2) Connect receiving equipment test equipment on receiving tower as shown in figure 8-2.

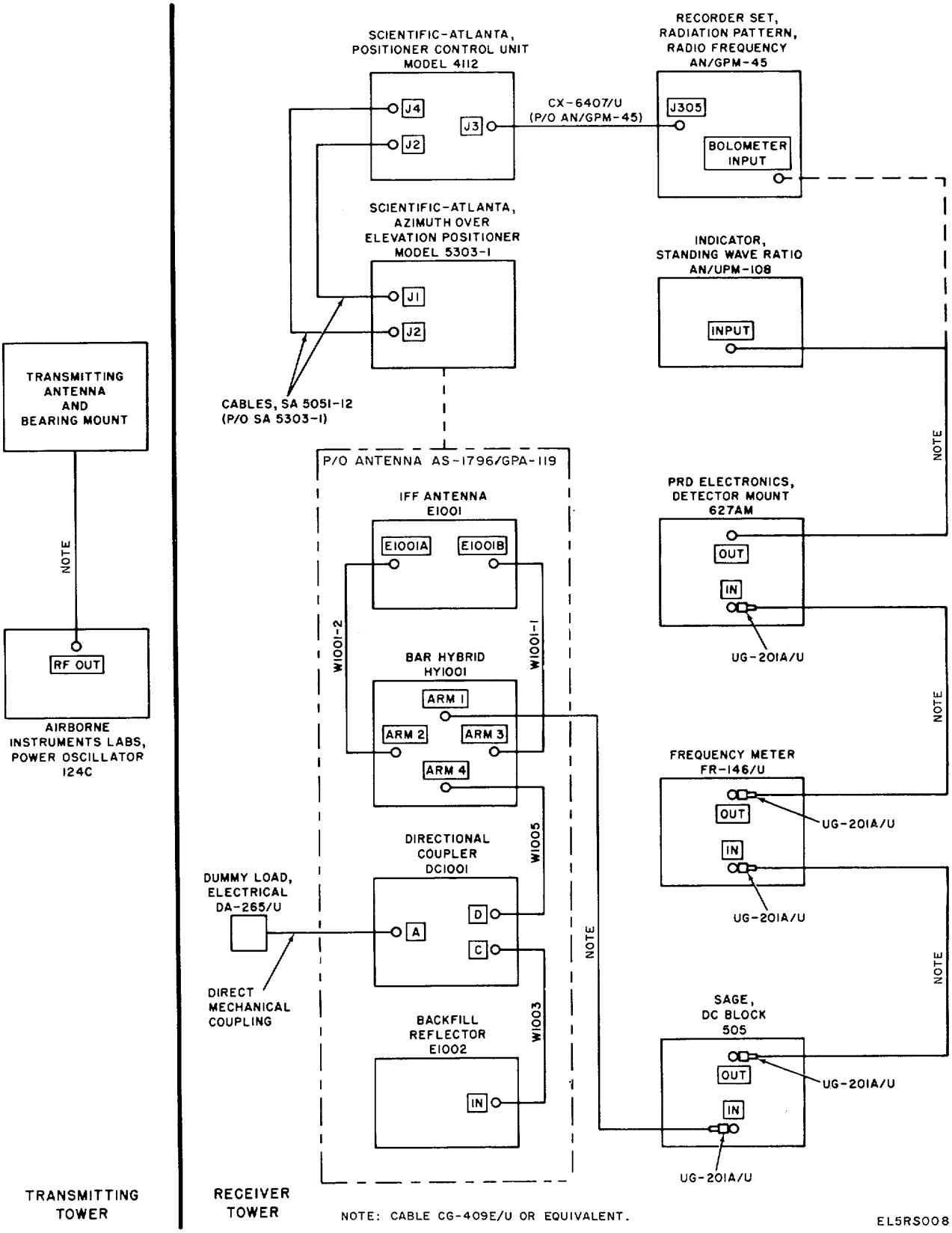


Figure 8-2. Antenna AS-1796/GPA, sum pattern test connections.

CAUTION

At receiving tower, on AN/UPM-108, place INPUT SELECTOR to XTAL, BOLO BIAS switch to LOW.

(3) At receiving tower, apply 117 vac power to test equipment, place all power switches to on, and allow 5 minutes to stabilize equipment.

(4) At receiving tower, on AN/UPM-108, place INPUT SELECTOR switch to BOLO 200 OHMS, RANGE switch to 40 db (setting may be changed to obtain stable usable signal).

(5) On transmitting tower, assemble test equipment for transmission of L-band energy as shown in figure 8-2.

(6) At transmitting tower, apply 117 vac power to test equipment, and allow 5 minutes for stabilization.

(7) transmitting tower, on AIL 124C, place FILAMENT POWER switch to ON and observe that filament power indicator lights.

(8) At transmitting tower, on AIL 124C when PLATE POWER indicator lights, place PLATE POWER switch to ON.

(9) At transmitting tower, on AIL 124C place PULSE POLARITY switch to NEG, and MODULATION SELECTOR switch to 1000 CYCLES.

(10) At transmitting tower, rotate transmitting antenna dipole to position of vertical polarization by rotating transmitting antenna bearing mount.

(11) At receiving tower, prepare AS-1796/ GPA-119 for test by adjusting SA 5303-1 in both azimuth and elevation planes (horizontal and vertical) for maximum received energy at 1030 MHz as indicated on AN/UPM-103.

(12) At transmitting tower, on AIL 124C, rotate OSCILLATOR TUNING control until dip indication is observed on AN/UPM-108.

(13) At transmitting tower, on transmitting antenna, perform boresighting adjustments by rotating bearing mount through 360 degrees of rotation.

(14) At receiving tower, on AN/UPM-108, as transmitting antenna dish and dipole are rotated, observe two electrical maximums of equal amplitude. Also, observe rotational angles of two maximums as indicated on transmitting antenna bearing mount protractor.

(15) At receiving tower, repeat step (14) above to verify that angles indicated are 180 +2 degrees apart.

(16) At receiving tower, if maximums are unequal in amplitude, or if angles are not 180 +2 degrees apart, perform necessary adjustments of transmitting antenna bearing mount followed by repetition of steps (13) and (14) above after each and every adjustment until boresighting of step (14) above is achieved.

(17) At transmitting tower, on transmitting antenna, rotate bearing mount to position of vertical polarization.

(18) At receiving tower, on FR-146/U, rotate FREQUENCY control to 1030 MHz.

(19) At receiving tower, on AN/UPM-108, set controls as follows:

INPUT SELECTOR: BOLO 200 OHMS
RANGE: 40 db
BOLO BIAS CURRENT: LOW

(20) At transmitting tower, on AIL 124C, rotate OSCILLATOR TUNING control until dip indication is observed on AN/UPM-108.

(21) At transmitting tower, on AIL 124C, depress OSCILLATOR TUNING control (tunes cathode only) for maximum deflection on RELATIVE POWER meter.

(22) At transmitting tower, on AIL 124C, adjust COUPLING control for ample gain, range, and signal stability as indicated on AN/UPM-108 (value of coupling should not exceed scale on RELATIVE POWER meter of AIL 124C).

(23) At transmitting tower, on AIL 124C, observe OSCILLATOR GRID meter needle does not move into red area.

(24) At transmitting tower, on AIL 124C, adjust MODULATION GAIN control to increase reading on OSCILLATOR GRID meter if below normal level indication.

(25) At receiving tower, on FR-146/U, readjust for maximum dip observed on AN/UPM-108. If frequency at observed dip is not 1030 MHz, reset FR-146/U for 1030 MHz and repeat step (22) above.

(26) At receiving tower, disconnect AN/ UPM-108 and connect the 627 AM detector mount to the AN/GPM-45 recorder set (fig. 8-2).

c Azimuth Pattern Test Procedure.

(1) At receiving tower, on AN/GPM-45, place AC POWER switch to ON.

(2) At receiving tower, on AN/GPM-45, set C RYSTAL-CURRENT-BOLO-METER switch to CURRENT, and adjust BOLO CURRENT ADJUST for bias current meter indication of 4.5 ma.

(3) At receiving tower, on AN/GPM-45, place CRYSTAL-CURRENT-BOLOMETER switch to BOLOMETER.

(4) At receiving tower, on AN/GPM-45, place PEN MOTOR switch to ON.

(5) At receiving tower, on AN/GPM-45, place CHART MOTOR switch to ON.

(6) At receiving tower, on AN/GPM-45, adjust GAIN and ATTENUATOR DB controls until chart pen rests at full scale (O db).

(7) At receiving tower, on AN/GPM-45, place DEGREES/CYCLE control to 360 degrees.

(8) At receiving tower, on AN/GPM-45, adjust CHART ZERO control until pen is exactly on zero degree line of chart.

(9) At receiving tower, on AN/GPM-45, place CHART DRIVE switch to AZIMUTH, and MANUAL CHART CONTROL to OFF.

(10) At receiving tower, on SA 4112, rotate SPEED CONTROL ccw until 180 degrees is indicated on chart.

(11) At receiving tower, refer to paragraph 48, and on AN/GPN-45, fill pen with red ink.

(12) At receiving tower, on AN/GPN-45, place LIFT-WRITE switch to WRITE.

(13) At receiving tower, on SA 4112, rotate SPEED CONTROL cw until 360 degrees is indicated. In this position, azimuth sum pattern is traced by pen on chart paper.

(14) At receiving tower, on AN/GPM-45, place LIFT-WRITE switch to LIFT.

(15) Verify that sum channel pattern is acceptable by studying the charted indication on the AN/GPM-45 and checking for the following (fig. 8-4):

(a) Azimuth beam width of main lobe is no more than 8 degrees at -3 db points.

(b) Maximum side lobes are at or below the -23 db level. If sum pattern is acceptable, proceed with the following steps. If pattern is not acceptable, repeat steps (1) through (14) above.

NOTE

At receiving tower, on AN/GPM-45, do not readjust controls or manually move chart paper while performing this procedure to obtain a difference channel overlay pattern, unless instructed to do so.

(16) At receiving tower, on AN/GPM-45, place PEN MOTOR switch to OFF, and **CRYSTALCURRENT-BOLOMETER** switch to CRYSTAL**.**
This removes protective bolometer bias during disconnection of test cable.

(17) At receiving tower, on AS-1796/GPA119 remove DA-265/U from connector DC1001-A (IN) on directional coupler DC1001.Remove CG-409E/U, interconnected to dc block 505, from connector ARM 1 on bar hybrid HY1001 (fig. 8-2).

(18) At receiving tower, connect CG-409E/ U between dc block 505 and connector DC1001-A (IN) on DC1001. Connect DA-265/U to ARM 1 on HY1001 (fig. 8-3).

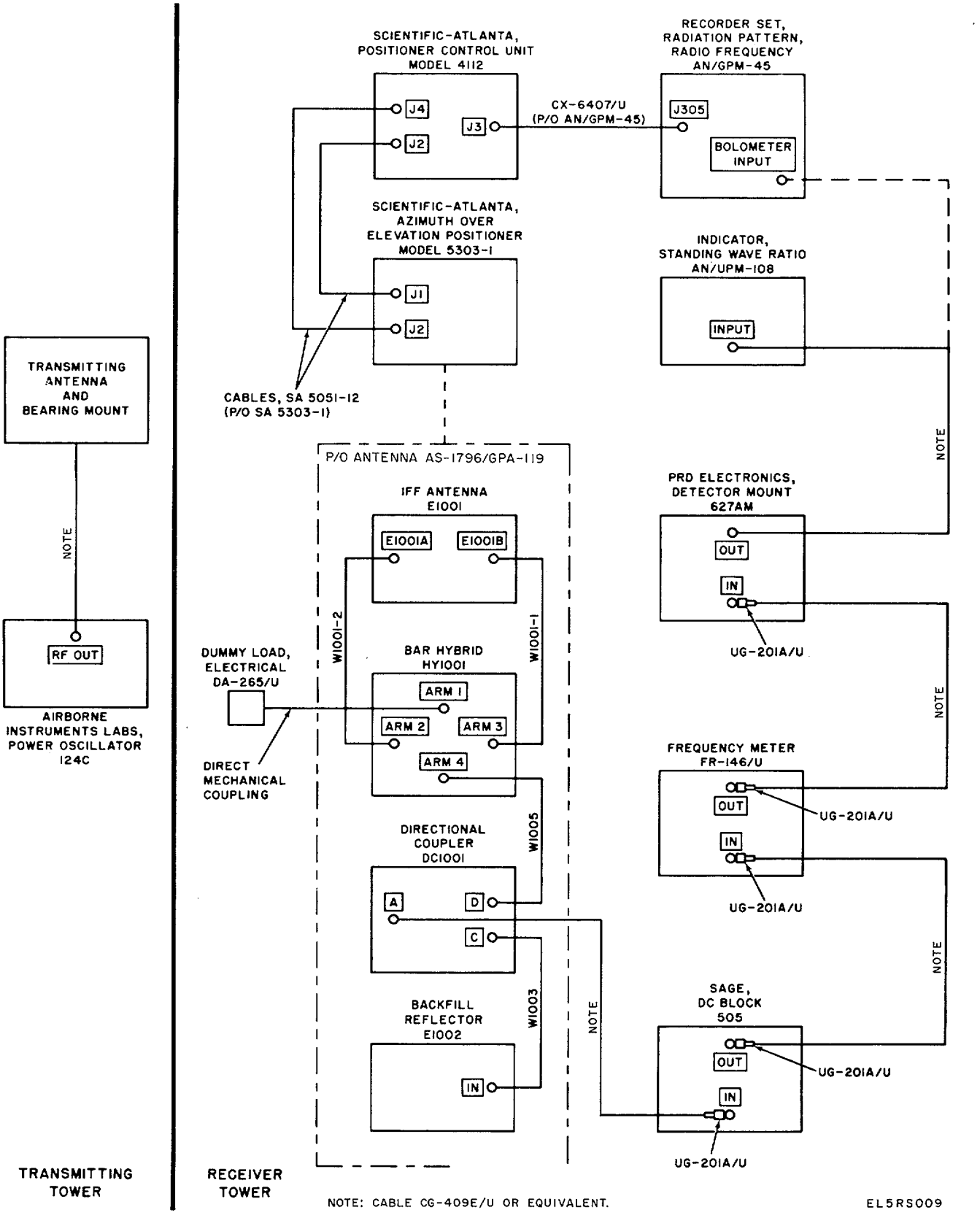


Figure 8-3. Antenna AS-1796/GPA-119, difference pattern test connections.

(19) At receiving tower, on AN/GPM-45, place PEN MOTOR switch to ON, and CRYSTALCURRENT-BOLOMETER switch to BOLOMETER.

(20) At receiving tower, on SA 4112 rotate SPEED CONTROL until zero degrees is indicated on chart, and then return the azimuth positioner 180 degrees ccw. This pattern begins at same angular position as that in step (13) above.

(21) At receiving tower, on AN/GPM-45, change pen ink to black (or opposite color used in step (11) above). On AN/GPM-45, place LIFT-WRITE switch to WRITE.

(22) At receiving tower, on SA 4112, rotate SPEED CONTROL cw to 360 degrees to obtain the azimuth difference pattern which overlays the sum pattern.

(23) Verify that difference channel pattern is acceptable by studying the charted indication on the AN/GPM-45 and checking for the following (fig. 8-4):

(a) Difference pattern null-depth at zero degrees is at least 25 db below sum pattern reading at zero degrees.

(b) Difference pattern db-level exceeds sum pattern db-level by at least 4 db in all areas except the null interference regions (33 to 50 degrees either side of zero degrees).

If difference pattern is acceptable, proceed with step (24) below. If pattern is not acceptable, repeat steps (1) through (23) above until it is determined that pattern recordings are accurately plotted and meet performance standards.

(24) At receiving tower, on AN/GPM-45, place CRYSTAL-CURRENT-BOLOMETER switch to CRYSTAL, and LIFT-WRITE switch to LIFT. Remove and save used portion of chart paper.

d. Elevation Pattern Test Procedure.

(1) At receiving tower, on AS-1796/ GPA-119 remove CG-409E/U (dc block 505) from connector DC1001-A on DC1001 (fig. 8-2). Remove DA-265/U from ARM 1 on HY1001 (fig. 8-2).

(2) At receiving tower, on SA 5303-1, place AS-1796/GPA-119 in vertical position (elevation pattern measurement).

(3) At transmitting tower, rotate transmitting antenna bearing mount to horizontal polarization position.

(4) At receiving tower, on AS-1796/ GPA-119 install CG-409E/U between DC Block 505 and connector ARM 1 on HY1001 (fig. 8-2). Install DA-265/U on connector DC1001-A (IN) on DC1001 (fig. 8-2).

(5) At receiving tower, on SA 4112, rotate SPEED CONTROL until zero degrees is indicated on chart scale at AN/GPM-45.

(6) At receiving tower, on AN/GPN-45, place CRYSTAL-CURRENT-BOLOMETER switch to BOLOMETER.

(7) At receiving tower, on SA 5303-1, adjust for maximum pen deflection, and adjust GAIN control for exactly zero db as indicated on chart paper of AN/GPM-45.

(8) At receiving tower, on AN/GPM-45, place DEGREE/CYCLE control to 360 degrees.

(9) At receiving tower, on AN/GPM-45, adjust CHART ZERO control until pen is exactly on zero degree line of chart.

(10) At receiving tower, on SA 4112, rotate SPEED CONTROL ccw to 180 degrees.

(11) At receiving tower, on AN/GPM-45, place LIFT-WRITE switch to WRITE.

(12) At receiving tower, on SA 4112, rotate SPEED CONTROL cw 180 degrees to obtain elevation sum pattern.

(13) At receiving tower, observe that plotted pattern is accurate and meets performance standards (45 degrees, maximum beam width at 3 db points). If not acceptable, repeat steps (5) through (13) before proceeding. For typical elevation pattern, see figure 8-5.

(14) At receiving tower, on AN/GPM-45, place LIFT-WRITE switch to LIFT.

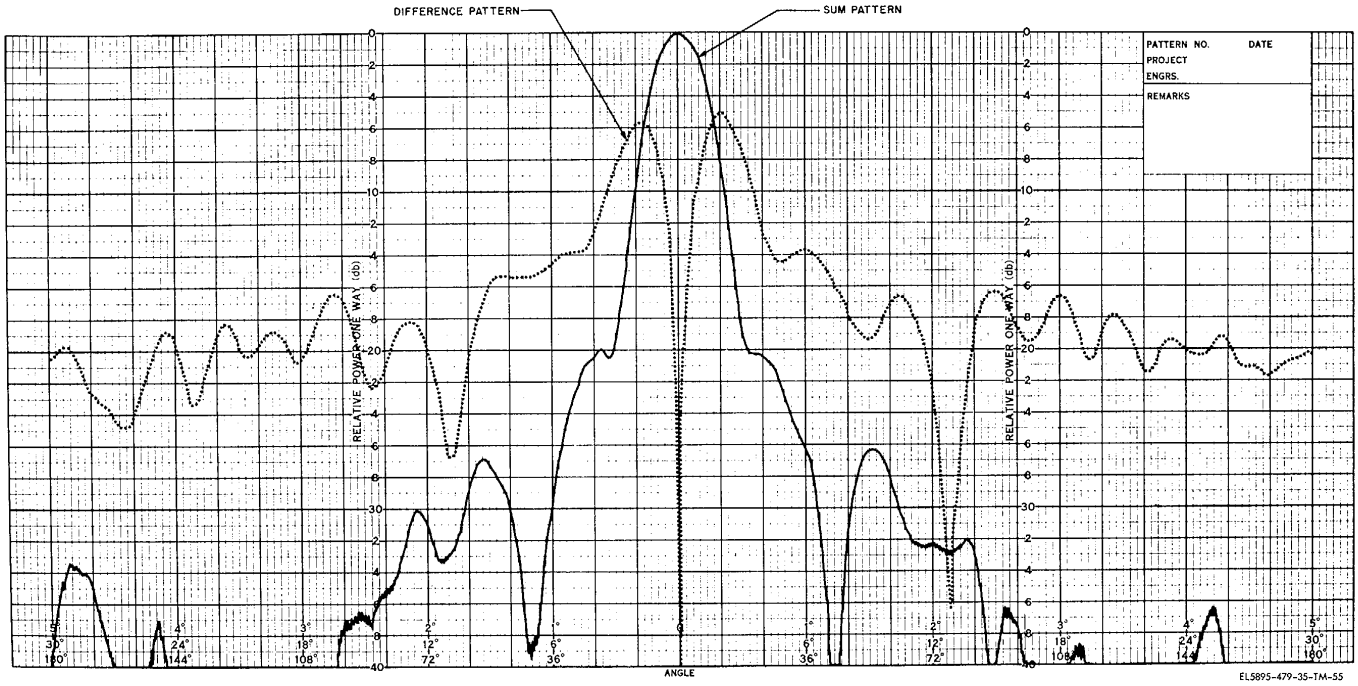


Figure 8-4. Antenna AS-1 796/GPA--119, typical azimuth sum and difference pattern.

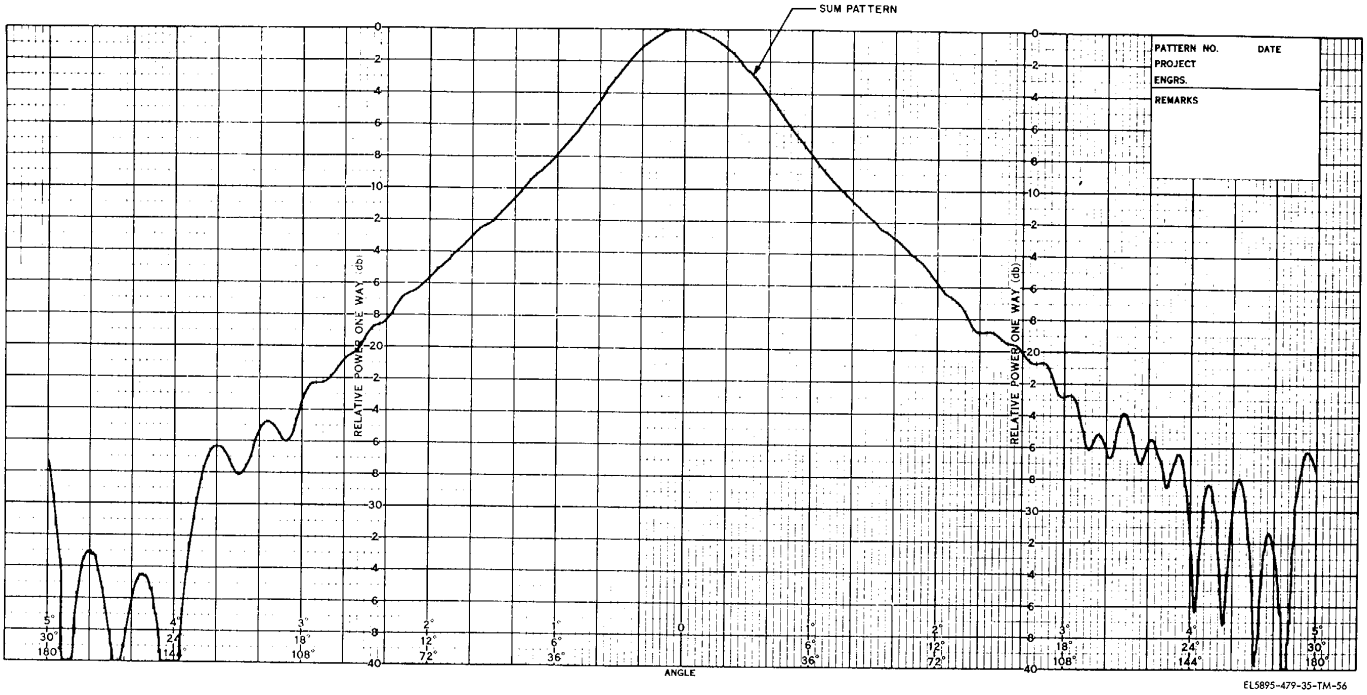


Figure 8-5. Antenna AS-1796/GPA-119 typical elevation sum and difference pattern.

(15) At receiving tower, on AN/GPM-45, place CRYSTAL-CURRENT-BOLOMETER switch to CRYSTAL.

(16) Disconnect all test equipment.

8-8. Antenna AS-1796/GPA-119 Gain Test

a. Test Equipment.

(1) Transmitting equipment. Power oscillator, model 124C.

(2) Receiving Equipment.

Dc block, model 505.

Frequency meter FR-146/U.

Detector mount PRD 627 AM, and element PRD 631C.

Indicator, Standing Wave Ratio AN/ UPM-108.

Standard gain horn, model 12-0.9.

Coax to waveguide adapter, model 11-0.9.

Dummy Load, Electrical DA-265/U.

Azimuth over elevation positioner, Scientific-Atlanta model 5303-1.

Positioner control unit, Scientific-Atlanta model 4112.

Cable, Scientific-Atlanta number 5051-12.

Cable, Radio Frequency CG-409E/U.

Adapter, Connector UG-201A/U.

b. Test Connections and conditions.

(1) At receiving tower, on SA 5303-1, assemble AS-1796/GPA-119 on adapter and attach with long dimension in the vertical direction.

(2) At receiving tower, connect test equipment as shown in figure 8-6.

(3) At receiving tower, apply 117 vac power to test equipment and allow 5 minutes to stabilize.

(4) At receiving tower, on AN/UPM-108, place INPUT SELECTOR switch to BOLO 200 OHMS, RANGE switch to 40 db, BOLO BIAS CURRENT switch to LOW, and LINE POWER switch to ON.

(5) At transmitting tower, assemble test equipment for transmission of L-band energy as shown in figure 8-6.

(6) At transmitting tower, apply 117 vac power to test equipment and allow 5 minutes to stabilize.

(7) At transmitting tower, on AIL 124C, place FILAMENT POWER switch to ON and observe that filament power indicator lamp lights.

(8) At transmitting tower, on AIL 124C, when plate power indicator lamp lights, place PLATE POWER switch to ON.

(9) At transmitting tower, on AIL 124C, place PULSE POLARITY switch to NEG, and MODULATION SELECTOR switch to 1000 Hz.

(10) At transmitting tower, rotate transmitting antenna to position of horizontal polarization by rotating transmitting antenna bearing mount (fig. 8-6).

(11) At receiving tower, on AS-1905/TPX, adjust by rotating SA 5303 in both azimuth and elevation planes (horizontal and vertical) for maximum received energy as indicated on AN/ UPM-108.

(12) At transmitting tower, on AIL 124C, rotate OSCILLATOR TUNING control until dip indication is observed on AN/UPM-108 at receiving tower.

(13) At transmitting tower, perform boresighting adjustments of transmitting antenna by rotating bearing mount through 360 degrees of rotation. Rotation is performed about axis of antenna radiation.

(14) At transmitting tower, as transmitting antenna rotates, observe two electrical maximums of equal amplitude as indicated on AN/UPM-108 at receiving tower. Also observe rotational angles corresponding to two maximums as indicated on bearing mount protractor. Repeat several times to verify that angles indicated are 180 +2 degrees apart.

(15) At transmitting tower, if maximums are unequal in amplitude, or if angles are not 180 +6 degrees apart, perform line adjustments of bearing mount followed by repetition of steps (13) and (14) above after each and every adjustment until boresighting of step (14) is achieved.

(16) At transmitting tower, on transmitting test antenna, adjust bearing mount to position of horizontal polarization.

(17) At receiving tower, on FR-146/U, rotate FREQUENCY control to 1030 +2 MHz.

(18) At receiving tower, on AN/UPM-108, set controls as follows:

SELECTOR: BOLO 200 OHMS.
RANGE: 40 db.
BOLO BIAS CURRENT: LOW (19)

(19) At transmitting tower, on AIL 124C, rotate OSCILLATOR TUNING PLATE and CATHODE control until dip indication is observed on AN/UPM-108 at receiving tower.

(20) At receiving tower, on FR-146/U, adjust FREQUENCY control for 1130 MHz.

(21) At transmitting tower, on AIL 124C, press OSCILLATOR TUNING control (tunes cathode only) and adjust for maximum deflection on RELATIVE POWER meter.

(22) At transmitting tower, on AIL 124C, adjust COUPLING control for ample gain range and signal stability as indicated on AN/UPM-108 at receiving tower (value of coupling should not exceed scale on RELATIVE POWER meter of AIL 124C).

(23) At transmitting tower, on AIL 124C, observe OSCILLATOR GRID meter needle does not swing into red area.

(24) At transmitting tower, on AIL 124C, adjust MODULATION GAIN control to increase reading on OSCILLATOR GRID meter if below normal level indication.

(25) At receiving tower, on FR-146/U, readjust FREQUENCY control for maximum dip 8-14 observed on AN/UPM-108. If frequency at observed dip is not 1030 MHz, reset FR-146/U for 1030 MHz and repeat step (19) above.

(26) At receiving tower, on SA 4112, adjust SA 5303-1 in azimuth and elevation until maximum indication of received energy is observed on AN/UPM-108.

c. Procedure.

(1) On AN/UPM-108, rotate VERNIER GAIN control for scale meter indication of 0 to 5 db.

NOTE

Do not change VERNIER GAIN control setting while performing following steps.

(2) At receiving tower, on AN/UPM-108, place INPUT SELECTOR switch to XTAL 200 ohms.

(3) At receiving tower, on AS-1796/ GPA-119, remove CT-1409E/U between dc block 505 and connector ARM 1 on bar hybrid HY1001 (fig. 8-6). Install CG-409E/U between dc block 505 and coax-to-waveguide adapter SA11-0.9 (fig. 8-6).

(4) At receiving tower, place SA-11-0.9 and SA-12-0.9 assembly directly above center of AS-1905/TPX. Point assembly toward transmitting test antenna on transmitting test tower and observe indication at position of maximum received signal on AN/UPM-108 with INPUT SELECTOR placed to BOLO 200 ohms.

(5) At receiving tower, on AN/UPM-108, record meter indication in db. Typical meter indication is 4.1 db.

(6) At receiving tower, calculate relative gain of AS-1796/GPA-119 as follows:

(a) Gain (G) = Computed db (calculated difference between steps (27) and (31) above), plus gain factor of SA-12-0.9 at 1030 MHz, plus calculated RF loss introduced by bar hybrid HY1001 and matched cable W1001-2.

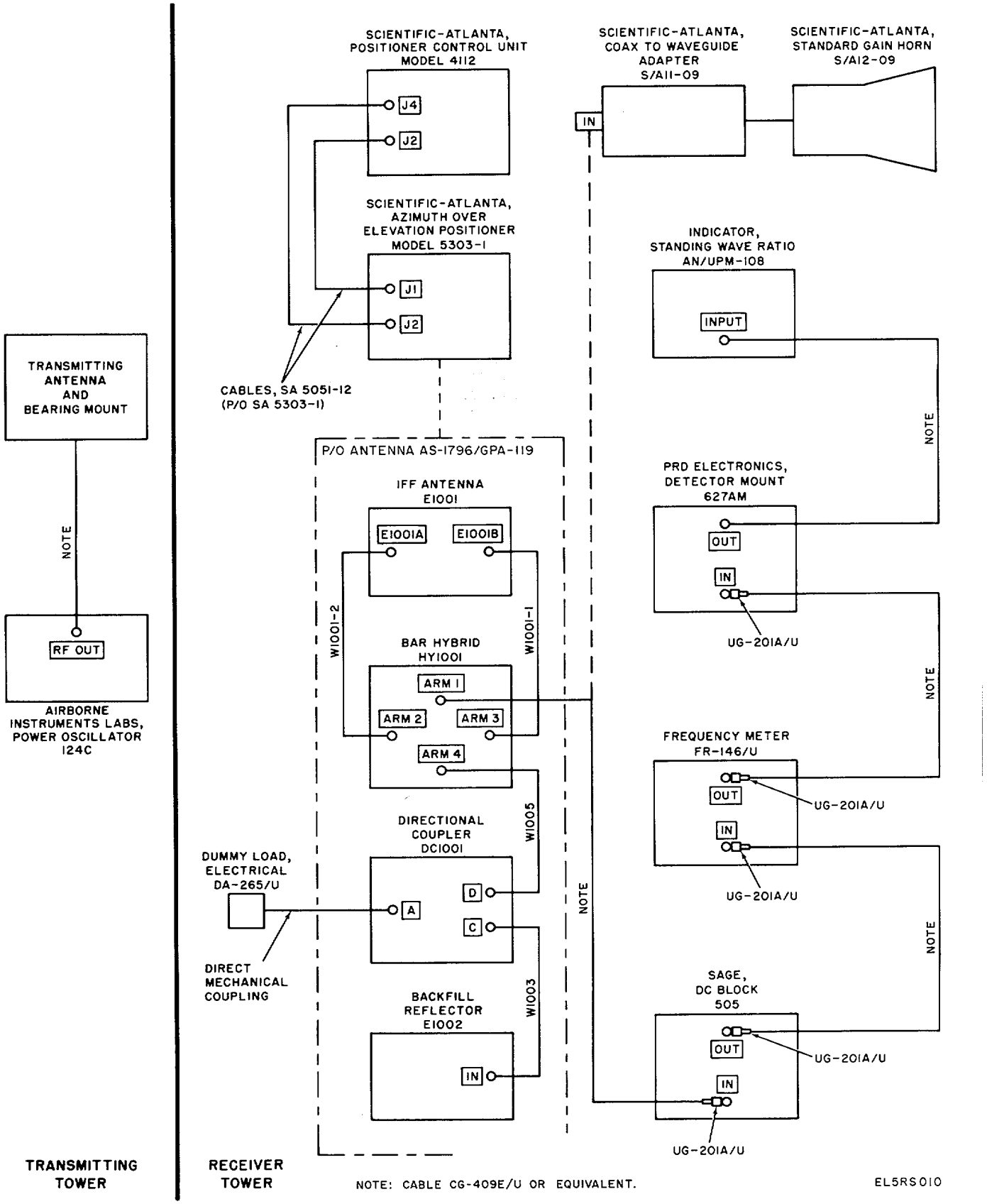


Figure 8-6. Antenna AS-1786/GPA-119, gain test connections.

(9) Remove AS-1905/TPX from adapter and test mount.

8-9. RF Switch Test Generator

a. General. Depot maintenance testing of RF switch S1001 requires fabrication of a test generator for use with the required items of test equipment. Fabrication of the test generator shall be completed by the depot, using the parts contained in the chart below. Assemble and wire the components of the test generator, following instructions contained in figure FO-22.

(b) Example: G =9 db + 13.94 db + 1.1 db + 15.94 db.

(c) Gain (G) = 15 db minimum.

(7) Observe that AS-1796/GPA-119 meets performance standard (15 db minimum gain).

(8) Remove power, disconnect test cables, and remove test equipment). b. Material.

b. Material.

Manufacturer's part No.	Description	Circuit designation	Federal supply code	Quantity
G38003S6	Transformer	T1	90095	1
G280040S1	Transformer	T2	01961	1
G390045S1	Silicon controlled rectifier	CR2, 3	24930	1
	Semiconductor device, diode 1N270.	CR1	81349	1
CP09AKE103K3	Capacitor, fixed, paper di-electric: 0.01-µf, 10%.	C1,2	81349	2
CP09AlKE153K3	Capacitor, fixed, paper di-electric: 0.01-µf, 10%.	C3	81349	1
	Capacitor, fixed, electrolytic: 2.2-µf, 10%.	C4	56289	2
PBO1FA03..	Binding post: red	E1	81349	1
PBO1FA04	Binding post: black	E4,5	81349	2
275 (green)	Binding post: green, 2,000 vdc, 30 amp.	E2,3	71002	2
7661	Switch: 4 PST	S1	15605	1
	Resistor, fixed, composition: 470-ohm, 5%,1/2 W	R1	81349	1
	Resistor, fixed, composition: 1-ohm, 5%, 1/4W. Resistor, fixed, composition: 47-ohm, 5%,1/4W.	R2	81349	1
	Connector, receptacle electrical UG-1094/U.	P1	81349	2
GS11-112	Mounting post		24930	2
32AA9	Phenolic board		00534	1
T94	Terminal		08145	50
C22	Wire: white, 22 gage		81349	2 ft
	Cable, radio frequency		81349	2 ft
A-150_	Chassis: 5 x 7 x 3 inch		00675	1
MS-16108-3A,	Test jack: black	TP1,2	96906	2
MS-16108-5A	Test jack: green	TP3,5	96906	2
MS-16108-2A	Test jack: red	TP4	96906	1
MS-16108-7A _	Test jack: blue	TP6,7,8	96906	3

8-10. Antenna AS-1796/GPA-119, RF Switch S1001 Test

a. Test Equipment and Materials.

Oscilloscope AN/USM-140B.
Pulse Generator AN/PPM-1A (2 required).
Multimeter TS-352/U.
Frequency Meter FR-146/U.
Power Supply PP-3135/U.
Indicator, Standing Wave Ratio AN/UPM108 (2 required).
Connector UG-274B (3 required).
Sweep oscillator, Hewlett-Packard model 691A.
Directional coupler, L-band, 10 db, Nardar model 3042-10 (2 required).
Adapter Connector UG-29B/U.
Dummy Load Electrical DA-265/U (2 required).
Cable Radio Frequency CG-409E/U.
Video detector, Sage model 1020J.
Detector mount, Polytechnic Research and Development model 627AM with element 631C.
Attenuator, 10 db, Weinschel model 50-10 (2 required).
Connector, Adapter UG-201A/U.
Crystal detector, Hewlett-Packard model 420B.
Attenuator, variable, Polytechnic Research and Development model L1110.
Power supply, Power Designs model 5015A (2 required).
ITT Gilfillan frequency diplexer, GIB 115327.
Resistor, 200-ohms, 1/4-watt.
Test Generator.

b. Test Connections and Conditions.

(1) Insure that the test generator is fabricated as shown in figure FO-22. Label test points, connectors, switch positions, and terminals as indicated.

(2) Arrange the test equipment as shown in figure 8-7, leaving RF switch S1001 out of the test circuit, and AC ON RESET switch on the PD5015A power supply positioned to OFF. Apply 117 vac power to the test equipment and allow 5 minutes for stabilization.

(3) On FR-146/U, rotate FREQUENCY control to 1030 MHz.

(4) On AN/UPM-108 (No. 1 and No. 2), set controls as follows:
LINE POWER: ON
INPUT SELECTOR: BOLO 200 ohms (No. 1); XTAL 200 ohms (No. 2)
RANGE (db) 40 db
BOLO BIAS CURRENT: LOW

(5) On HP691A, set controls as follows:
LINE: RF
SWEEP SELECTOR: CW
START/C'W: 1.03
POWER LEVEL: 10
FUNCTIONS: press START STOP
AMPLITUDE MOD: press INT SQ WAVE.

(6) On PRD LI110, adjust control to obtain midrance indication on 40 db scale of AN/UPM108 (No. 1).

(7) On HP691A, adjust MANUAL SWEEP control until meter indicates a dip on AN/UPM108 (No. 2). Adjust VERNIER GAIN control as necessary on AN/UPM-108.

(8) On AN/UPM-108 (No. 1), adjust VERNIER GAIN control for full scale meter needle deflection (O db) on 40 db scale.

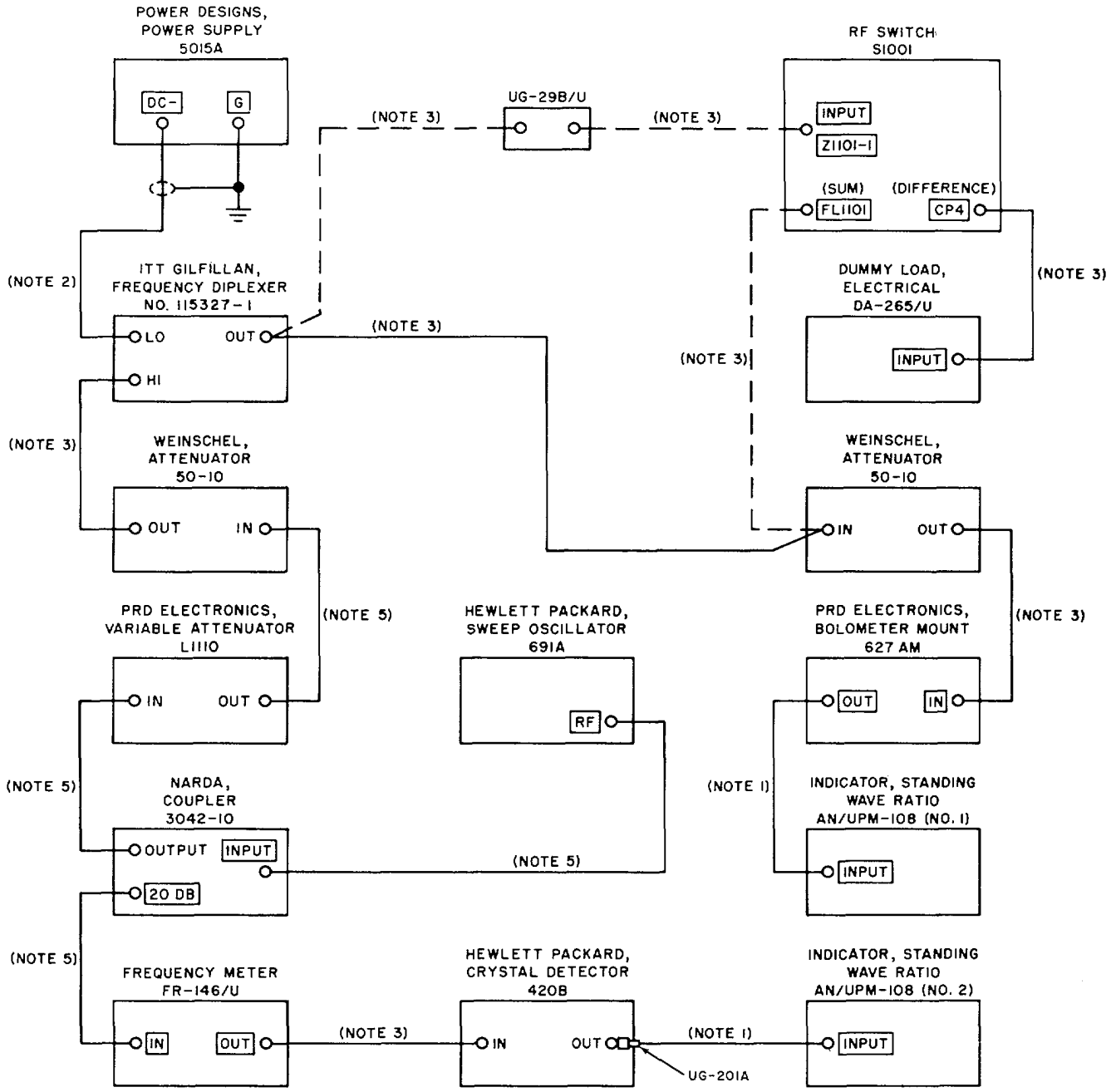
(9) On AN/UPM-108 (No. 1), place INPUT SELECTOR switch to XTAL 200 ohms.

NOTE

Do not change test equipment settings while performing following procedures unless instructed to do so.

c. RF Measurement Procedure.

(1) Connect RF switch S1001 in test circuit between ITTG frequency diplexer No. 115327 and Weinschel attenuator 50-10 (fig. 8-7).



NOTES:

1 CABLE CG-409E/U OR EQUIVALENT.
2 JUMPER CABLE FABRICATED LOCALLY.
3 DIRECT MECHANICAL CONNECTION.
4 ADAPTER UG-201A/U.
5 RG-214/U CABLE, TERMINATED EACH END WITH UG-21D/U CONNECTORS, FABRICATED LOCALLY.

Figure 8-7. Antenna AS-1796/GPA-119, RF switch S1001 insertion loss test connections.

(2) On the PD5015A, place AC ON RESET switch to ON. Adjust VOLTAGE control to -20 volts dc.

(3) On AN/UPM-108 (No. 1), place INPUT SELECTOR switch to BOLO 200 ohms.

4) On AN/UPM-108 (No. 1), observe that insertion loss of RF switch S1001 (between connector Z1101-1 (INPUT) on diplexer Z1101 and connector FL1101-OUT (SUM) on filter FL1101) is 3.8 db maximum.

(5) On PD 5015A, place AC ON RESET switch to OFF.

(6) On AN/UPM-108 (No. 1), place INPUT SELECTOR switch to XTAL 200 ohms.

(7) Remove S1001 from test circuit. Reconnect ITTG frequency diplexer No. 115327 and Weinschel attenuator 50-10.

(8) On AN/UPM-108 (No. 1), place INPUT SELECTOR switch to BOLO 200 ohms).

(9) On FS-146/U, rotate FREQUENCY control to 1090 MHz.

(10) On HP691A, adjust MANUAL SWEEP control until meter indicates a dip on AN/UPM108 (No. 2).

(11) On AN/UPM-108 (No. 1), adjust VERNIER GAIN control for full scale meter deflection (O db) on 40 db scale.

(12) On AN/UPM-108 (No. 1), place INPUT SELECTOR switch to XTAL 200 ohms.

NOTE

Do not change test equipment settings while performing following procedures unless instructed to do so.

(13) Connect RF switch S1001 in test circuit between ITTG frequency diplexer No. 115327 and Weinschel attenuator 50-10 (fig. 8-7).

(14) On PD5015A, place AC ON RESET switch to ON. Check for -20-volt dc output.

(15) On AN/UPM-108 (No. 1), place INPUT SELECTOR to BOLO 200 ohms. Observe that insertion loss of RF switch S1001 (between connector Z1101-1 (INPUT) on diplexer Z1101 and connector FL1101-OUT (SUM) on filter FL1101) is 3.8 db maximum, as indicated on AN/UPM-108 (No. 1)).

(16) On AN/UPM-108 (No. 1), place INPUT SELECTOR to XTAL 200 ohms.

(17) Disconnect and remove all test equipment (fig. 8-7).

d. RF Switching Test Procedure.

(1) Complete test circuit connections shown in figure 8-8. Check that power supply voltage controls are set fully ccw for 0-volt output.

(2) On FR-146/U, rotate FREQUENCY control to 1030 MHz.

(3) On PD5015A (No. 2), place AC ON RESET switch to ON, and adjust VOLTAGE control to -10 volts dc.

(4) On PD5015A (No. 1), place AC ON RESET switch to ON, and adjust VOLTAGE control to -1.5 volt dc.

(5) On PP-3135, place AC POWER switch to ON, METER RANGE switch to 0-500 VOLTS, HIGH VOLTAGE switch to ON, and HV CONTROL to 250 volts dc.

(6) On HP691A, set controls as follows:

LINE: RF
START CW: 1.03
FUNCTION: press START STOP
SWEEP SELECTOR: CW
POWER LEVEL: 10
AMPLITUDE MOD: press INT SQ WAVE

(7) On AN/USM-140B, set controls as follows:

POWER: ON
ASTIGMATISM: midposition
FOCUS: midposition
INTENSITY: midposition
SCALE LIGHT: fully cw
CHANNEL A VERTICAL AMPLIFIER
POSITION: midposition
POLARITY: +UP
HORIZONTAL POSITION: midposition

HORIZONTAL DISPLAY INTERNAL
SWEEP MAGNIFIER: X1
EXTERNAL VERNIER: CALIBRATE
AC-DC: DC
SWEEP TIME: (MICROSECONDS/ CM): 0.5
VERNIER: CAL
TRIGGER SLOPE: as desired
TRIGGER LEVEL: as desired
SWEEP MODE: PRESET
TRIGGER SOURCE: EXT AC
CHANNEL A-CHANNEL B: CHAN-NEL A
SENSITIVITY: (VOLTS/CM): 10
VERNIER: DC

(8) On AN/UPM-108 set controls as follows:

LINE POWER: ON
INPUT SELECTOR: XTAL 200 ohms
METER SCALE: NORMAL
RANGE: 40 db
BOLO BIAS CURRENT: LOW

(9) On AN/PPM-1A (No. 1), set controls as follows:

POWER: ON
PULSE RATE: 300
ATTENUATION: 0
SYNC SELECTOR: X1
POLARITY: +
PULSE LENGTH:5 MICROSECONDS
AMPLITUDE: 10

(10) On AN/PPM-1A (No. 2), set controls as follows:

POWER: ON
ATTENUATION: 0
SYNC SELECTOR: +
POLARITY: +
PULSE LENGTH:5 /sec
AMPLITUDE: 10

(11) On TS-352/U, place FUNCTION switch to DIRECT.

(12) With 117 vac power applied to test equipment, allow 5 minutes for stabilization.

(13) On TS-352B/U, connect black test lead between OHM-DC ±AC connector and TP1 (GRD) on test generator (fig. FO-22).

(14) On TS-352B/U, connect red test lead between 500 V connector on 20,000 OHMS PER VOLT DC and test point TP4 (+250V) on test generator (fig. FO-22).

(15) Check all connections of cables and tightness of connections in test circuit.

NOTE

Use care during adjustment of critical voltages in the following steps.

(16) On PP-3135/U, adjust HV CONTROL for 250-volt indication on TS-352B/U.

(17) On TS-352B/U, remove red lead from test circuit, connect red test lead to 50V range connector on 20,000 OHMS PER VOLT DC, and place FUNCTION switch to 20,000 ohms/VDC REV.

(18) On TS-352B/U, connect red test lead to TP3 (-20v) on test generator (fig. FO-22).

(19) On PD 5015A (No. 2), adjust VOLTAGE control for -20-volt indication on TS352B/U.

(20) On TS-352B/U, remove red lead from test circuit and connect to 2.5V range connector.

(21) On TS-352B/U, connect red test lead to TP5 (-1.5v) on test generator (fig. FO-22).

(22) On PD5015A (No. 1), adjust VOLTAGE control for -1.5-volt indication on TS-352B/U.

(23) On AN/USM-140B, move CHANNEL A INPUT cable assembly CG-409A/U to UG274B/UT connector on test generator, test point TP6.

(24) On AN/PPM-1A (No. 1), adjust controls for 10 volt peak amplitude, 0.5 µsec pulse duration at 300 pps.

(25) On AN/USM-140B, move CHANNEL A INPUT CT-409E/U to UG-274B/U on test generator, test point TP7.

(26) On AN/PPM-1A (No. 2), adjust for same pulse characteristics as for AN/PPM-1A (No. 1) (step (24) above), and adjust PULSE POSITION

control for 1.5 μsec delay from AN/PPM-1A (No. 1) pulse position adjustment.

(27) On AN/USM-140B, move CHANNEL A INPUT CG-409E/U to UG-274B/U with 200-ohm load attached (fig. 8-8). Check that DC POWER switch at test generator is ON.

(28) On HP691A, adjust POWER LEVEL control until meter on AN/UPM-108 indicates full scale deflection (maximum RF output).

(29) On FR-146/U, rotate FREQUENCY control to 1030 MHz.

(30) On AN/UPM-108, adjust VERNIER GAIN control for midrange meter indication on 40 db scale.

(31) On HP691A, rotate START/CW control for meter dip indication on AN/UPM-108. On HP691A, remove INT SQ WAVE modulation.

(32) On AN/USM-140B, observe and record peak pulse amplitude of positive pulse.

(33) On AN/PPM-1A (No. 1) PULSE OUT connector, disconnect CG-409E/U from test point TP6 at test generator (fig. 8-8).

(34) On AN/USM-140B, observe that pulse is no longer displayed, and that base level does not shift.

(35) On HP691A, place LINE switch to STANDBY.

(36) Disconnect cable from connector FL1101-OUT (SUM) on filter FL1101, and remove DA-265/U from connector CP1104 (DIFFERENCE) on filter FL1102 at RF switch S1101.

(37) Connect cable to connector CP-1104 (DIFFERENCE) on FL1102, and connect DA-265/U to connector FL1101-OUT (SUM) on FL1101.

(38) On HP691A, place LINE switch to RF, and allow 5 minutes to stabilize at maximum RF output of 1030 MHz.

(39) On AN/PPM-1A (No. 1) PULSE OUT connector, reconnect CG-409E/U to test point TP6 on test generator (fig. 8-8).

(40) On AN/USM-140B, observe that negative pulse does not differ in amplitude from pulse observed in step (32) above by more than +10 percent.

(41) On AN/PPM-1A (No. 1) PULSE OUT connector, disconnect CG-409E/U from test point TP6 on test generator.

(42) On AN/USM-140B, observe that pulse is no longer displayed, and that base level does not shift.

(43) Remove power from equipment, and restore RF switch S1101 to service.

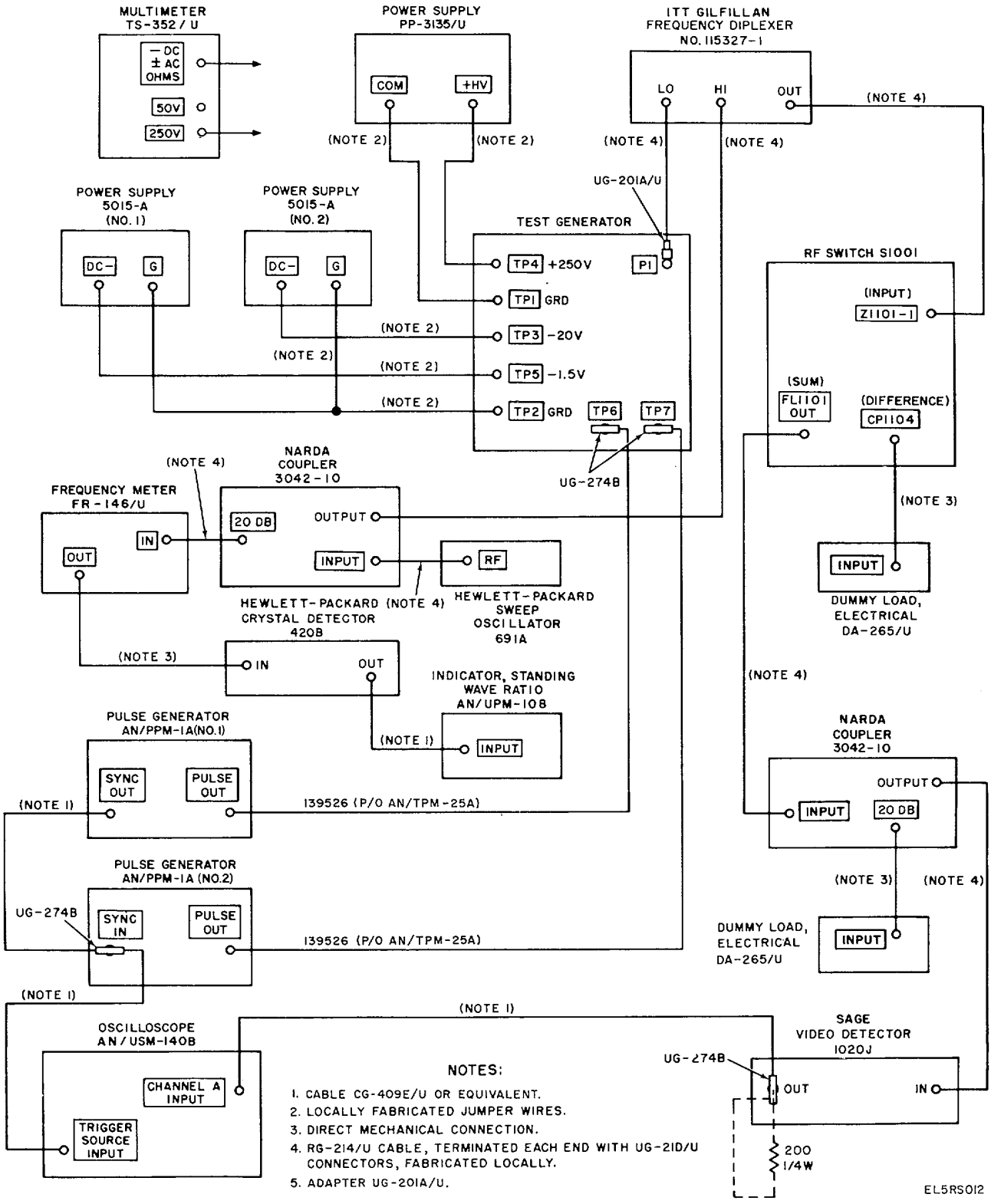


Figure 8-8. Antenna AS-1796/GPA-ll9, RF switch S1001 switching test connections.

APPENDIX

REFERENCES

Following is a list of applicable references that are available to the direct and general support and depot maintenance repairman of Interrogator Set AN/TPX-41.

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	U.S. Army Equipment Index of Modification Work Orders.
SC 5180-91-CL-R07	Tool Kit, Electronic Equipment TK-105/G.
TB 9-6625-042-35	Calibration Procedure for: Frequency Meter FR-146/U, Microlab/FXRN410(), H-P Model 536A, and FEL Model WDA-940.
TB SIG 222	Solder and Soldering.
TB SIG 355-1	Depot Inspection Standard for Repaired Signal Equipment.
TB SIG 355-2	Depot Inspection Standard for Refinishing Repaired Signal Equipment.
TB SIG 355-3	Depot Inspection Standard for Moisture and Fungus Resistant Treatment.
TM 55-1500-323-25	Installation Practices for Aircraft Electric and Electronic Wiring.
TM 11-1175	Radar Test Set AN/UPM-6A and Radar Test Set AN/UPM-6B.
TM 11-6625-237-14	Pulse Generator AN/PPM-1.
TM 11-5109	Coaxial Slotted Line IM-92/U.
TM 11-6625-258-14	Signal Generator SG-299/U, SG-299 A/U, SG-299 B/U, and SG-299 C/U.
TM 11-5840-293-12	Organizational Maintenance Manual: Radar Set AN/FPN-40 (With IFF Capability).
TM 11-5840-293-35	DS, GS and Depot Maintenance Manual: Radar Set AN/FPN-40 (With IFF Capability).
TM 11-5840-309-35	DS, GS, and Depot Maintenance Manual: Decoder, Video KY-593/TPX-44 and Control, Remote Switching C-7014/TPX-44.
TM 11-5840-309-35P	DS, GS, and Depot Maintenance Repair Parts and Special Tool Lists: Decoder, Video KY-593/TPX-44.
TM 11-5840-326-35	DS, GS, and Depot Maintenance Manual: Simulator, Radar Signal SM-472/TPX-44.
TM 11-5840-326-35P	DS, GS, and Depot Maintenance Repair Parts and Special Tool Lists: Simulator, Radar Signal SM-472/TPX-44.
TM 11-5840-345-20	Organizational Maintenance Manual: Landing Control Central AN/FSQ ( ).
TM 11-5840-345-34	Direct Support and General Support Maintenance Manual: Landing Control Central AN/TSQ( ).
TM 11-5840-346-20	Organizational Maintenance Manual: Multiplexer TD-991/G and Demultiplexer TD 992/G.
TM 11-5840-346-35	DS, GS, and Depot Maintenance Manual: Multiplexer TD-991/G and Demultiplexer TD 992/G.
TM 11-5895-201-35	DS, GS, and Depot Maintenance Manual: Coder-Control Interrogator Sets KY-97/TPX, KY-97A/TPX, KY-97B/TPX, KY-97C/TPX, and KY592/TPX-44.
TM 11-5895-479-12	Operator and Organizational Maintenance Manual: Interrogator Set AN/ TPX-41.

TM 11-5895-479-34P	Repair Parts and Special Tools List: Interrogator Set AN/TPX-41.
TM 11-5950-205-14P	Operator's Organizational, Field, and Depot Maintenance Repair Parts and Special Tool Lists and Maintenance Allocation Chart: Transformer, Variable, Power CN-16/U, CN-16A/U, CN-16B/U.
TM 11-6625-200-15	Operator and Organizational Maintenance Manual: Multimeters ME-26A and ME-26B/U, ME-26C/U, and ME-26D/U.
TM 11-6625-274-12	Operator's and Organizational Maintenance Manual: Test Sets, Electron Tube TV-7/U, TV-7A/U, TV-7B/U, and TV-7D/U.
TM 11-5540	Light Assembly, Electrical MX-1292/PAQ.
TM 11-6625-283-12	Operator and Organizational Maintenance Manual: Signal Generators TS-452B/U and TS-452 C/U.
TM 11-6625-299-15	Operator, Organizational, Field and Depot Maintenance Manual: Signal Generators AN/URM-64 and AN/URM-64A.
TM 11-6625-316-12	Operator and Organizational Maintenance Manual: Test Sets, Electron Tube TV-2/U, TV-2A/U, TV-2B/U, and TV-2C/U.
TM 11-6625-320-12	Operator, and Organizational Maintenance Manual: Voltmeter, Meter ME30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U, and ME30E/U.
TM 11-6625-335-12	Operator's and Organizational Maintenance Manual: Indicators, Standing Wave Ratio AN/UPM-108 and AN/UPM-108A.
TM 11-6625-354-12	Operator's and Organizational Maintenance Manual: Recorder Set, Radiation Pattern, Radio Frequency AN/GPM-45.
TM 11-6625-359-10	Operator's Manual: Spectrum Analyzer Set AN/UPM-84 (Polarad) TM 11-6625-366-15 Organizational, DS, GS, and Depot Maintenance Manual: Multimeter TS-352B/U.
TM 11-6625-368-10	Operator's Manual: Pulse Generator Sets AN/UPM-15 and AN/UPM-15A.
TM 11-6625-403-14	Operator, Organizational, and Field Maintenance Manual: Radar Test Set AN/UPM-98.
TM 11-6625-433-15	Organizational, DS, GS, and Depot Maintenance Manual Including Repair Parts and Special Tool Lists: Wattmeters AN/URM-98 and AN/URM 98A.
TM 11-6625-508-10	Operator's Manual: Signal Generators AN/USM-44 and AN/USM-44A.
TM 11-6625-535-15-1	Organizational, DS, GS, and Depot Maintenance Manual: Oscilloscopes AN/USM-140B, AN/USM-140C, AN/USM-141A, and AN/USM-141B.
TM 11-6625-537-15	Operator Organizational, Field, and Depot Maintenance Manual: Voltmeter, Electronic ME-202/U.
TM 11-6625-542-15	Operator, Organizational, Field and Depot Maintenance Manual: Electronic Marker Generator AN/USM-108.
TM 11-6625-700-25	Organizational, DS, GS, and Depot Maintenance Manual: Digital Readout Electronic Counter AN/USM-207.
TM 11-6625-2610-12	Operator's and Organizational Maintenance Manual for Radar Test Set AN/TPM-25A,

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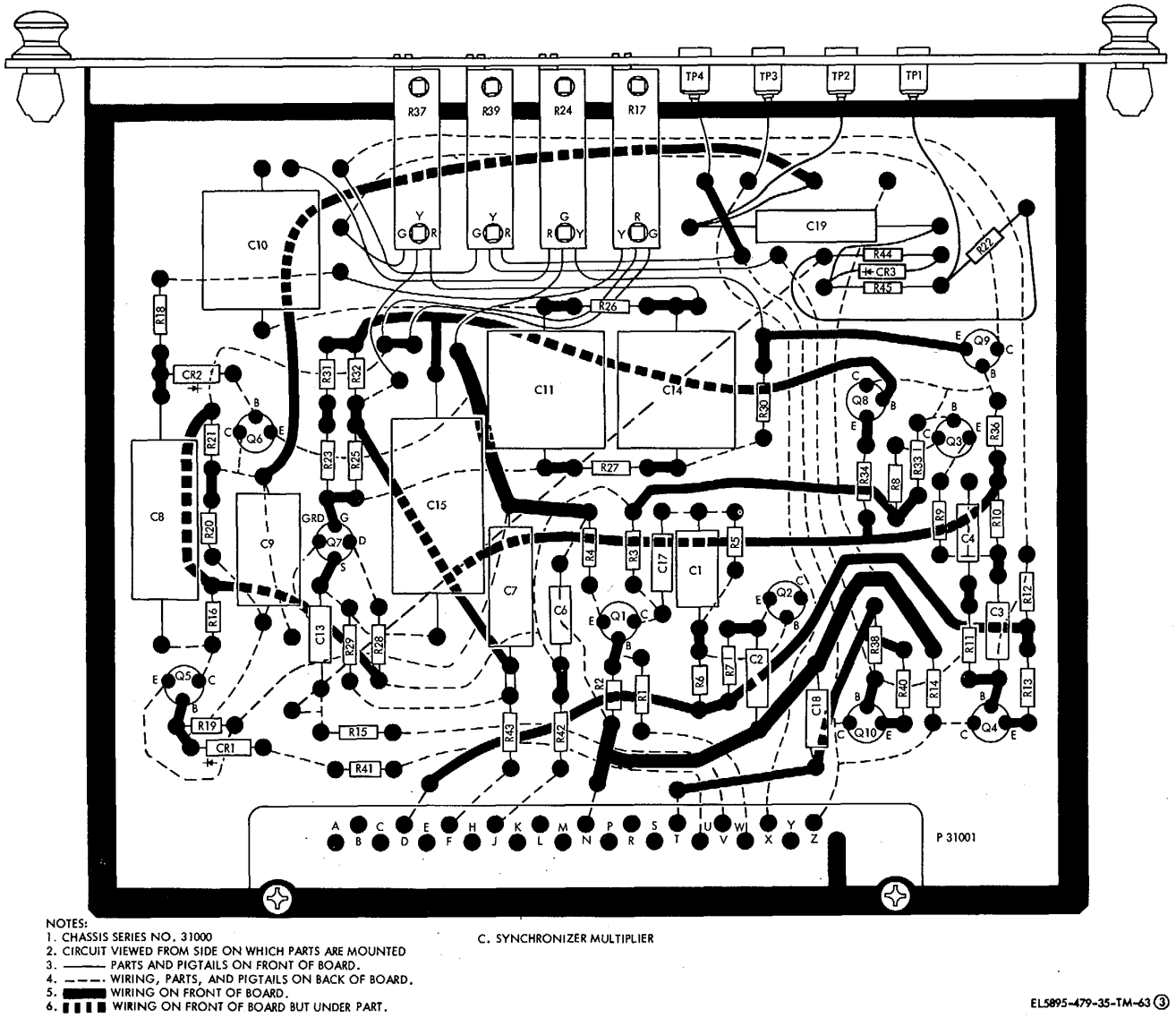
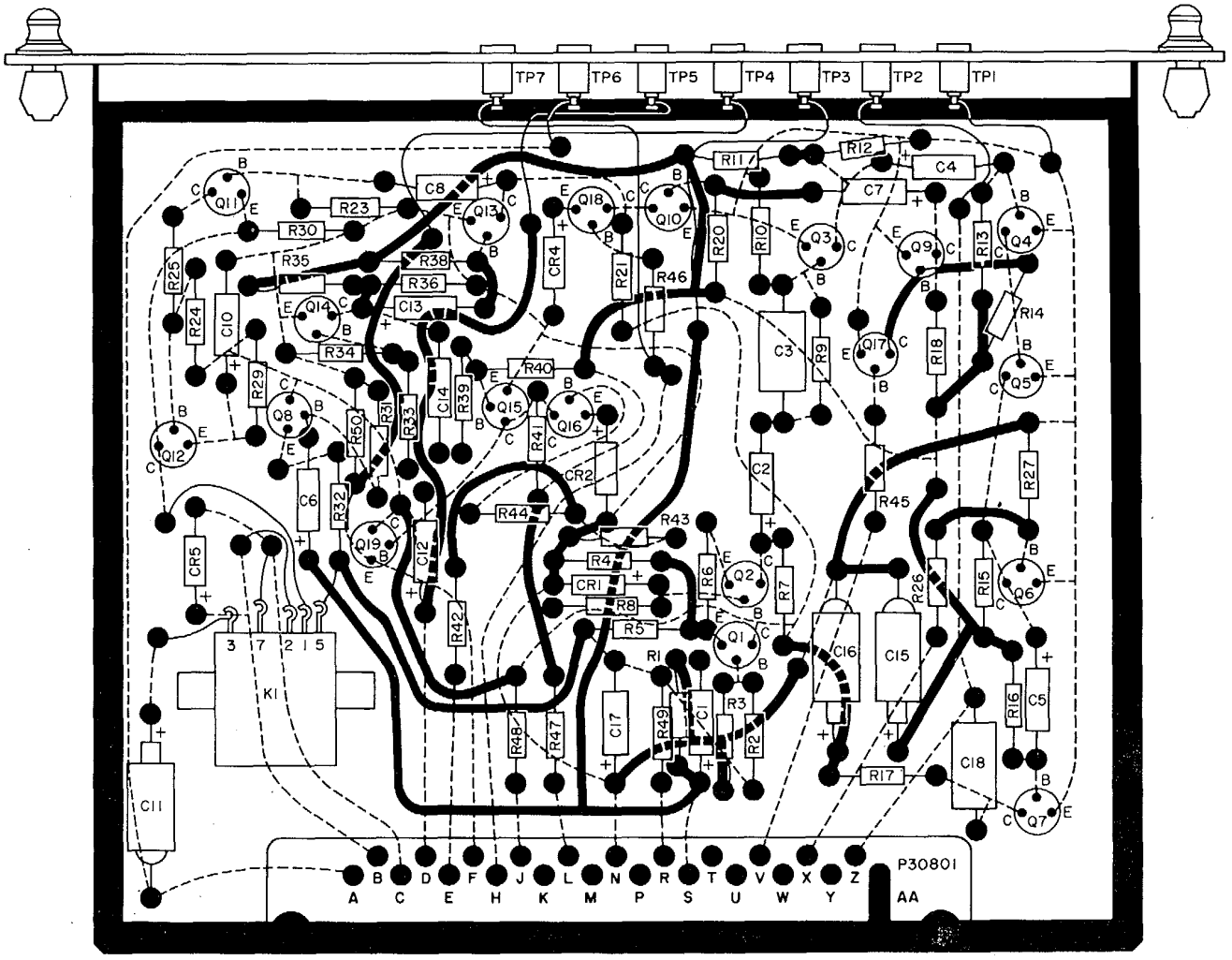


Figure FO-4 (3). Blanker, Interference MX-8 795/TPX-41, wiring diagram (sheet 3 of 4).



D. PROCESSOR

NOTES:

1. CIRCUIT VIEWED FROM SIDE ON WHICH PARTS ARE MOUNTED.
2. —— PARTS AND PIGTAILS ON FRONT OF BOARD.
3. – – – WIRING, PARTS, AND PIGTAILS ON BACK OF BOARD.
4. ■■■ WIRING ON FRONT OF BOARD.
5. ■■■ WIRING ON FRONT OF BOARD BUT UNDER PART.

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Figure FO-4 (4). Blanker, Interference MX-8 795/TPX-41, wiring diagram (sheet 4 of 4)

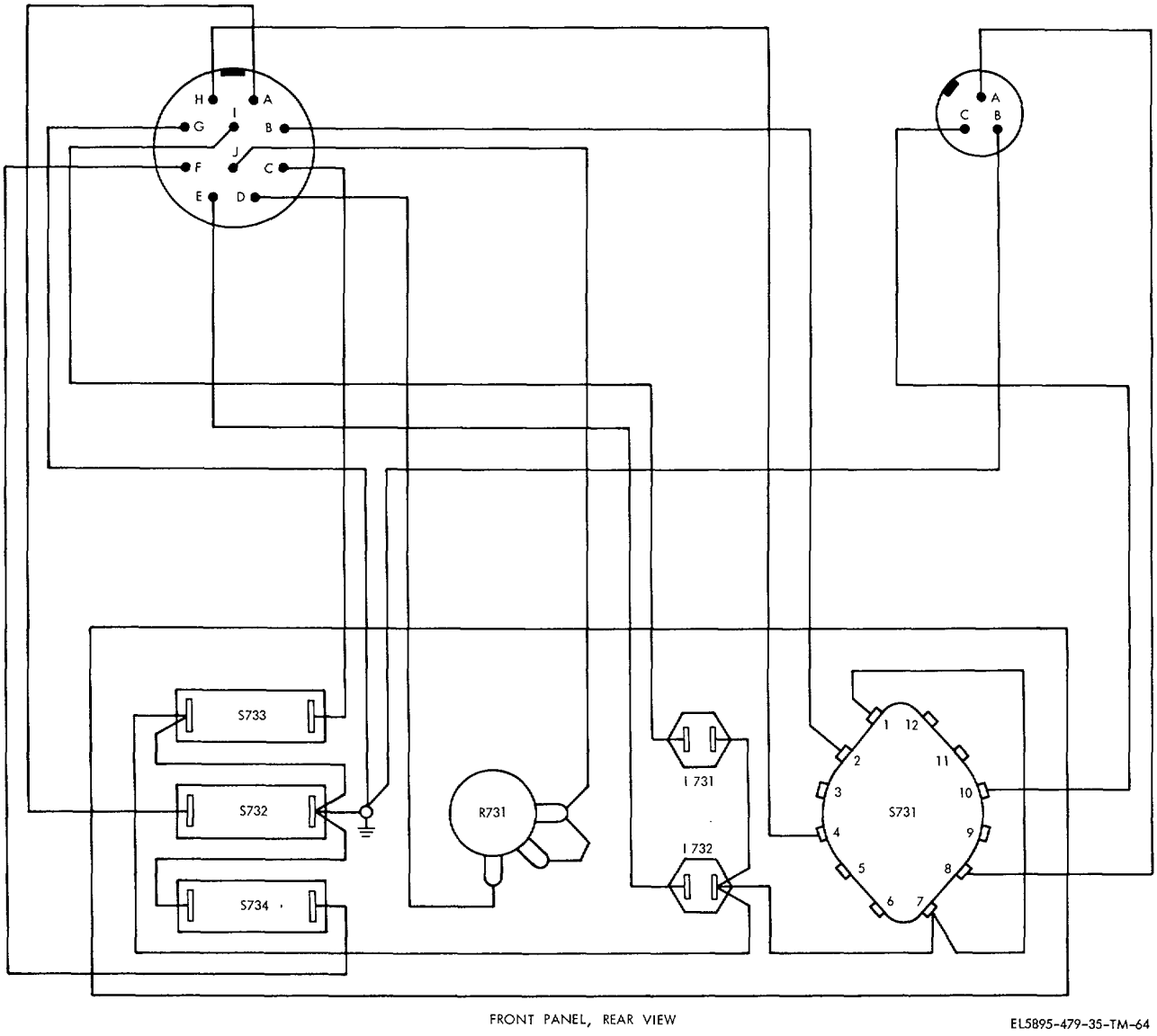
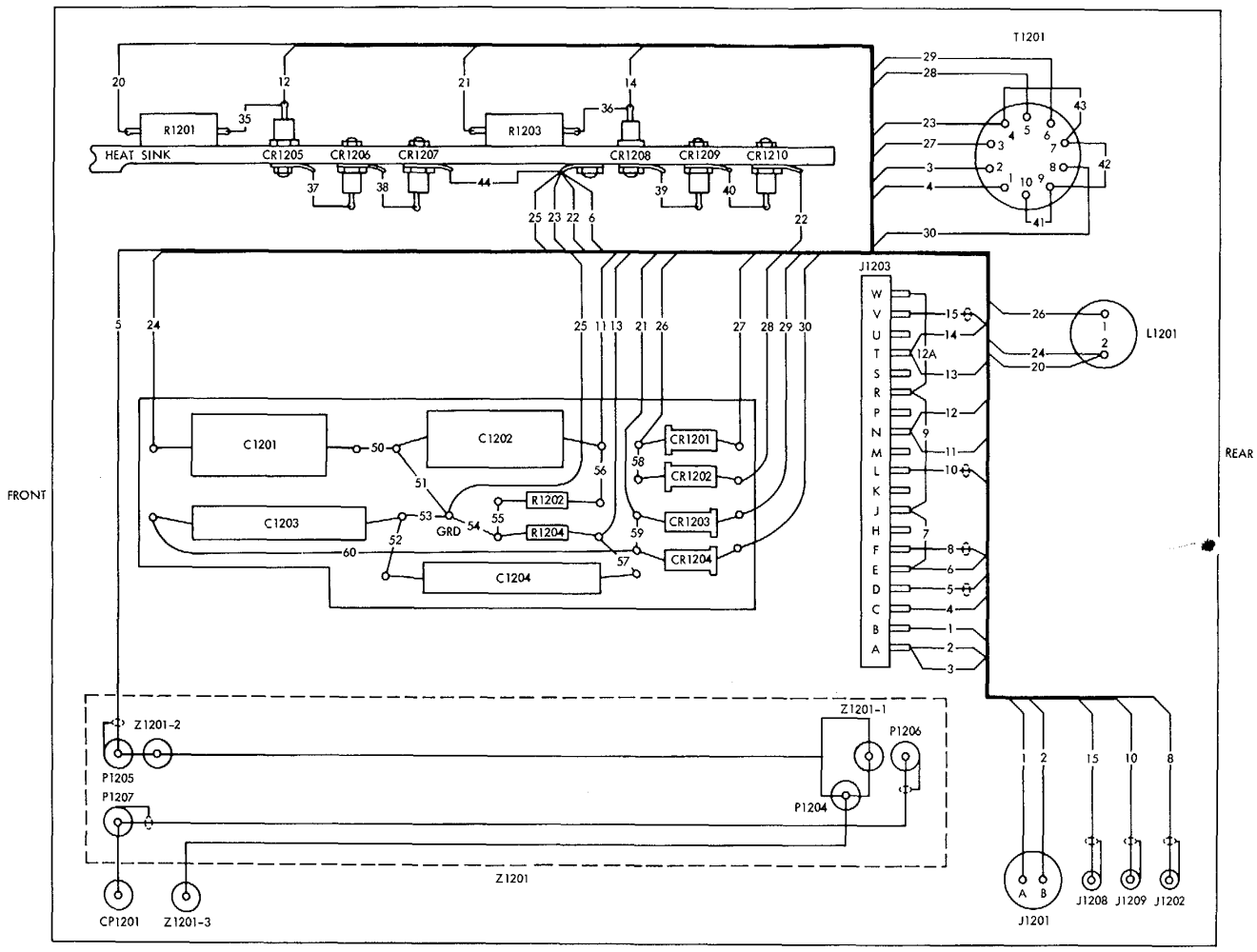


Figure FO-5. Control, Remote Switching C-1271A/TPX-22, wiring diagram.



NOTES:

1. THE ANGLE AT WHICH A SPECIFIC WIRE ENTERS A CABLE INDICATES THE DIRECTION TO FOLLOW IN FINDING THE OTHER END OF THE WIRE.
2. THE BASE LINE DOES NOT REPRESENT THE HARNESS.

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Figure FO-6 (1) . Modulator, Pulse MD-638/TPX-41, wiring diagram (sheet 1 of 2)

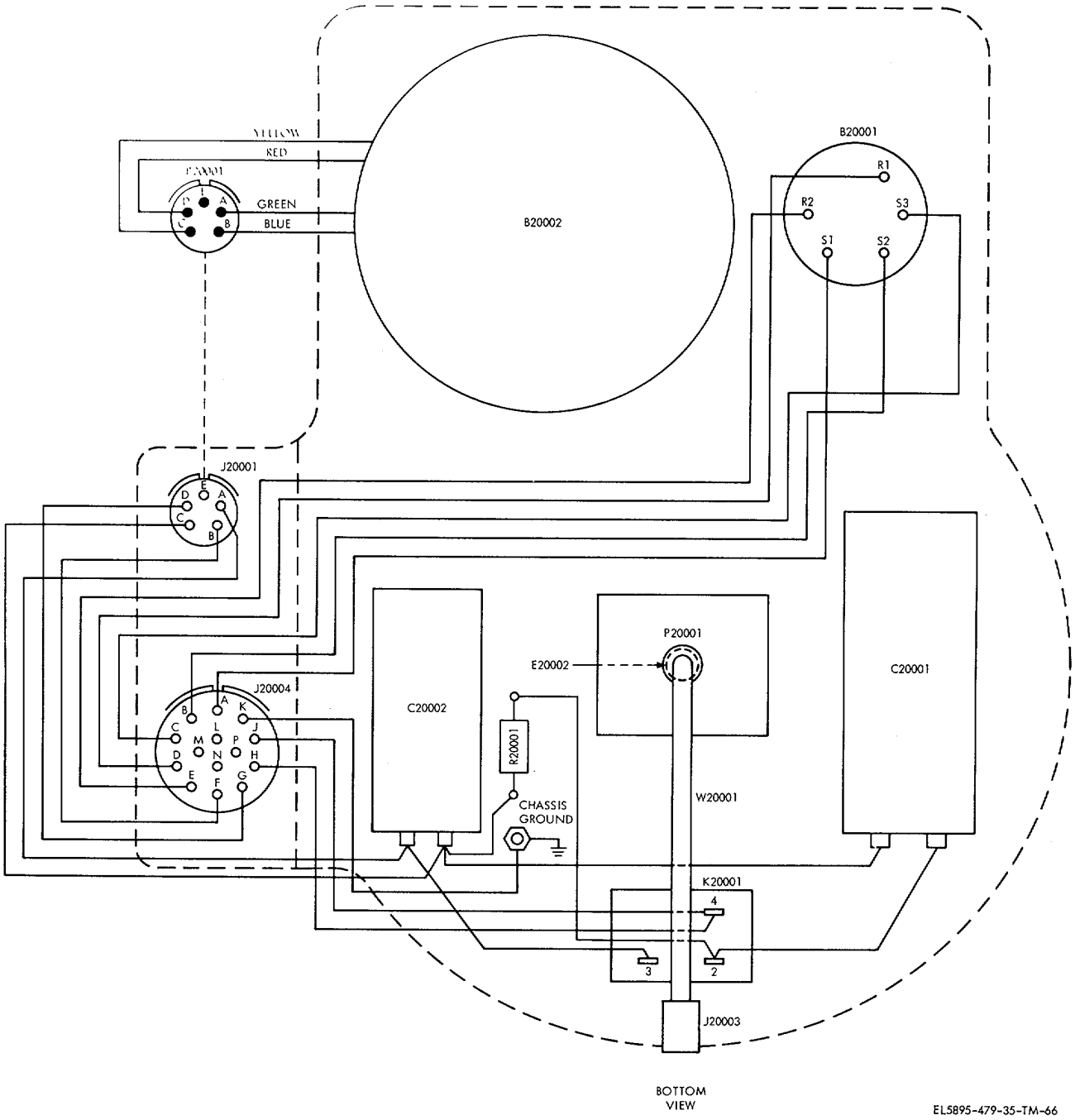


Figure FO-7. Pedestal, Antenna AB- 1158/GPA- 119, wiring diagram.

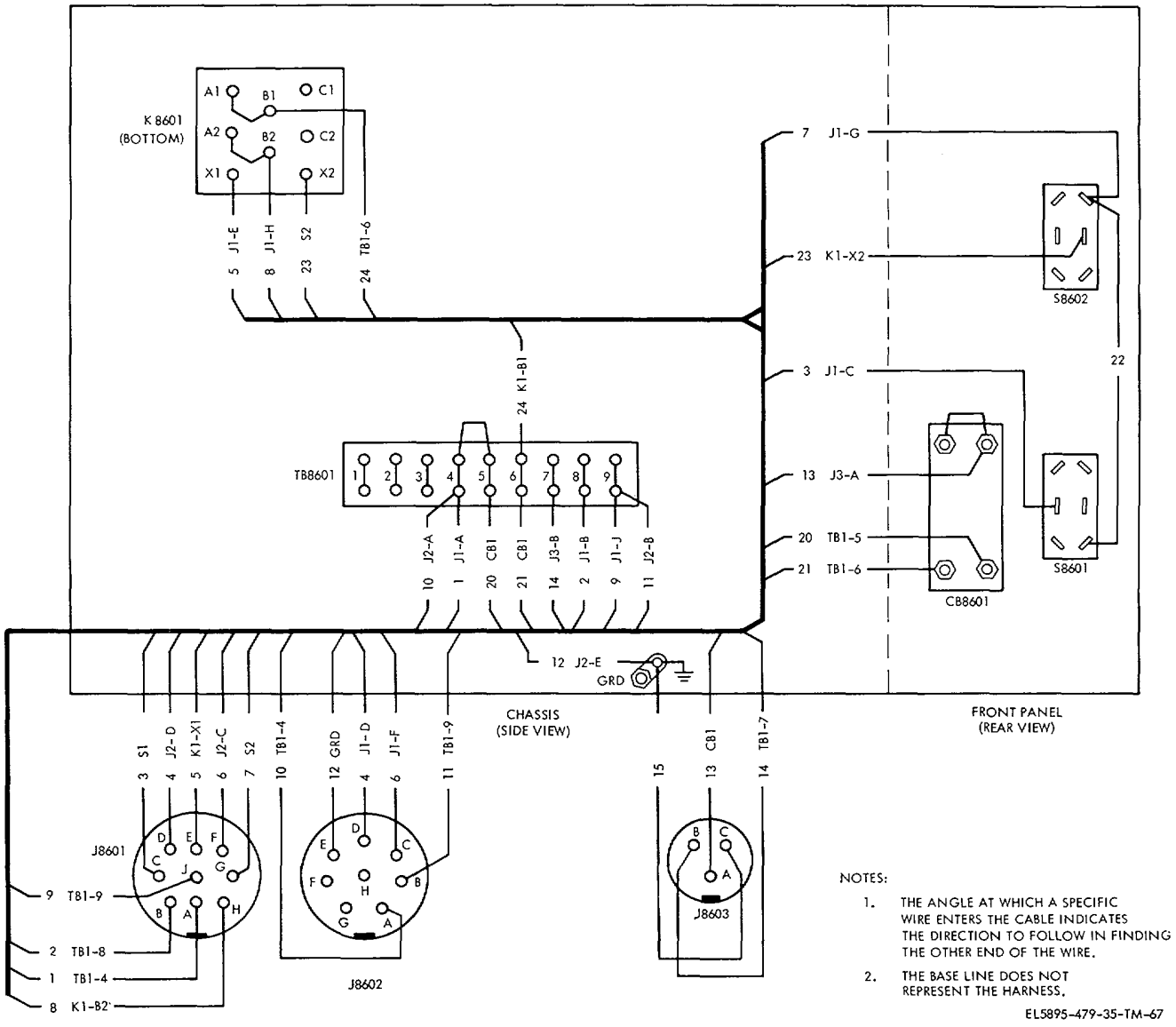


Figure FO-8. Interconnecting Box J-2945/TPX-41, wiring diagram.

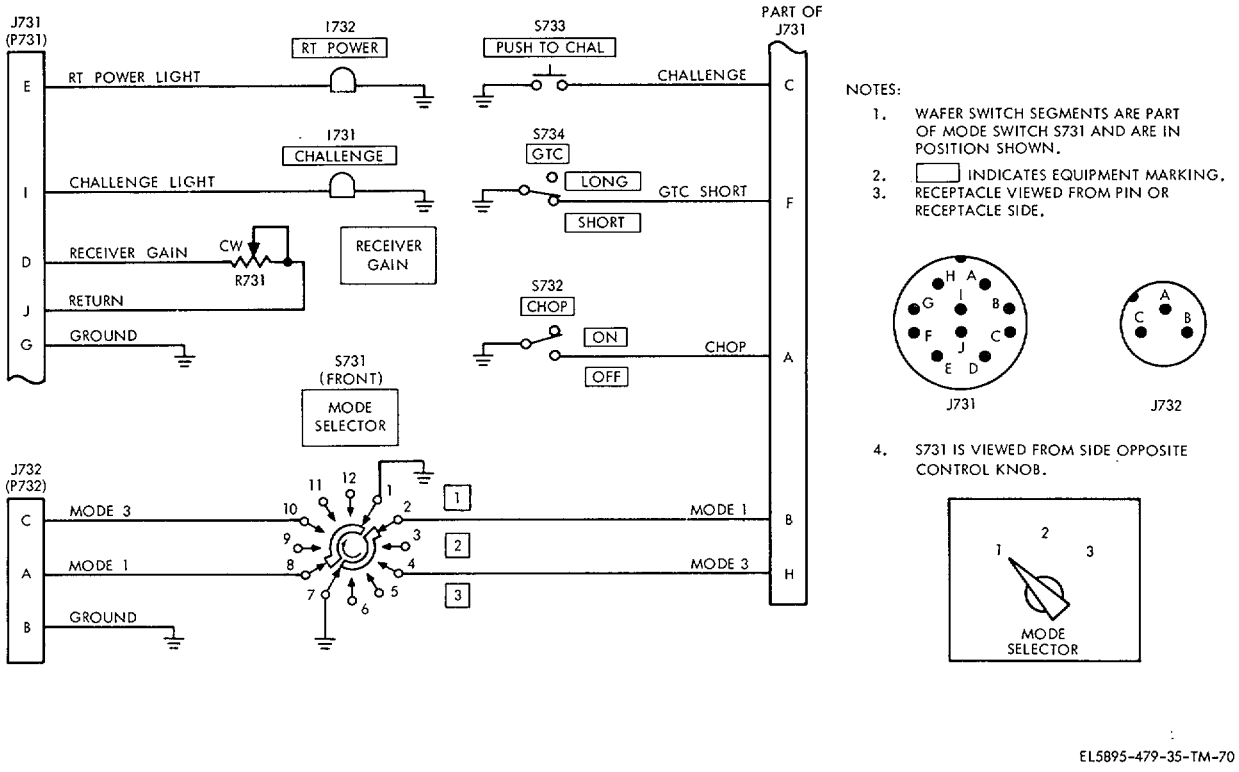


Figure FO-11. Control, Remote Switching C--1271A/TPX-22, schematic diagram.

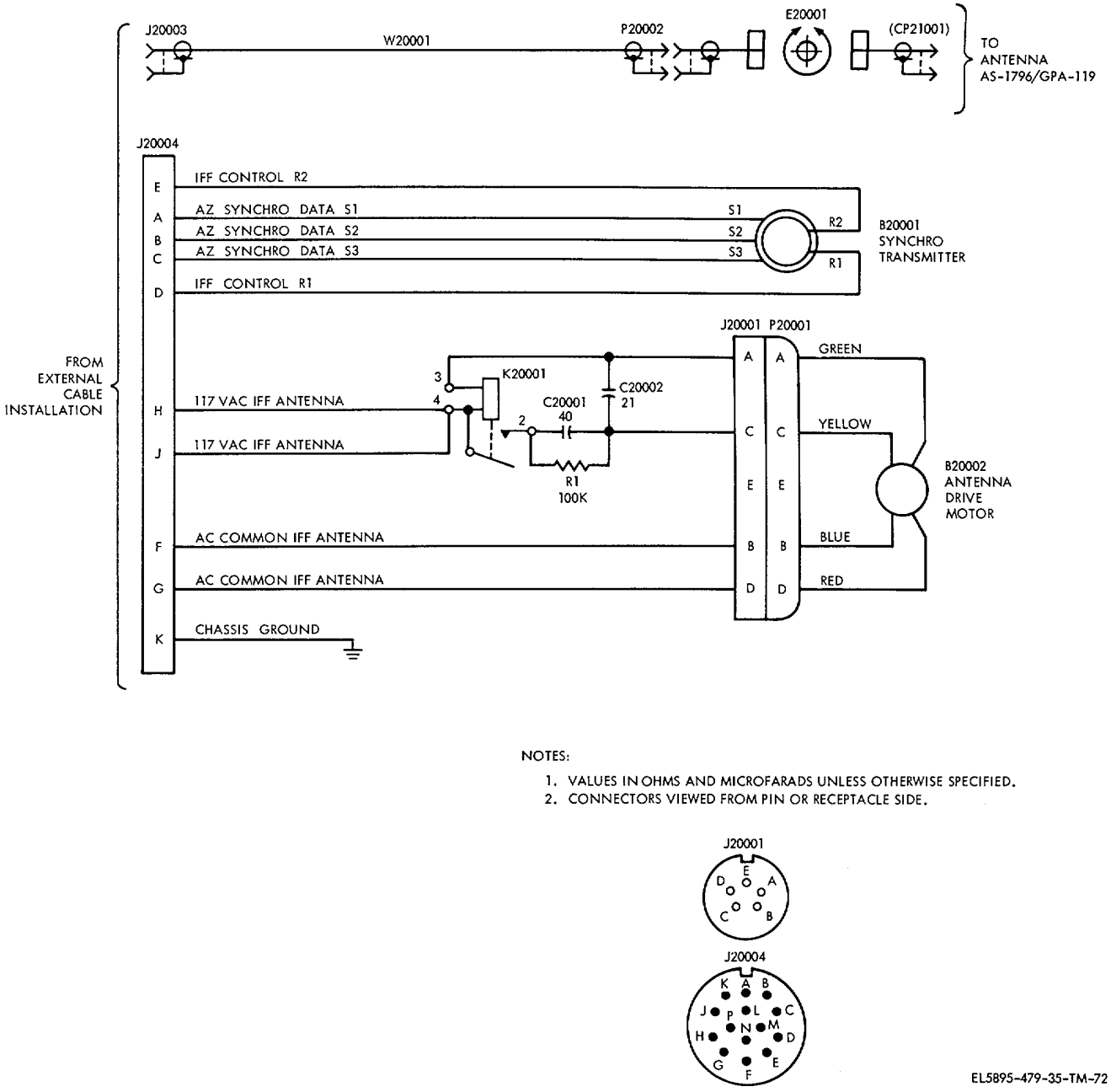


Figure FO-13. Pedestal, Antenna AB--1158/GPA--119, schematic diagram.

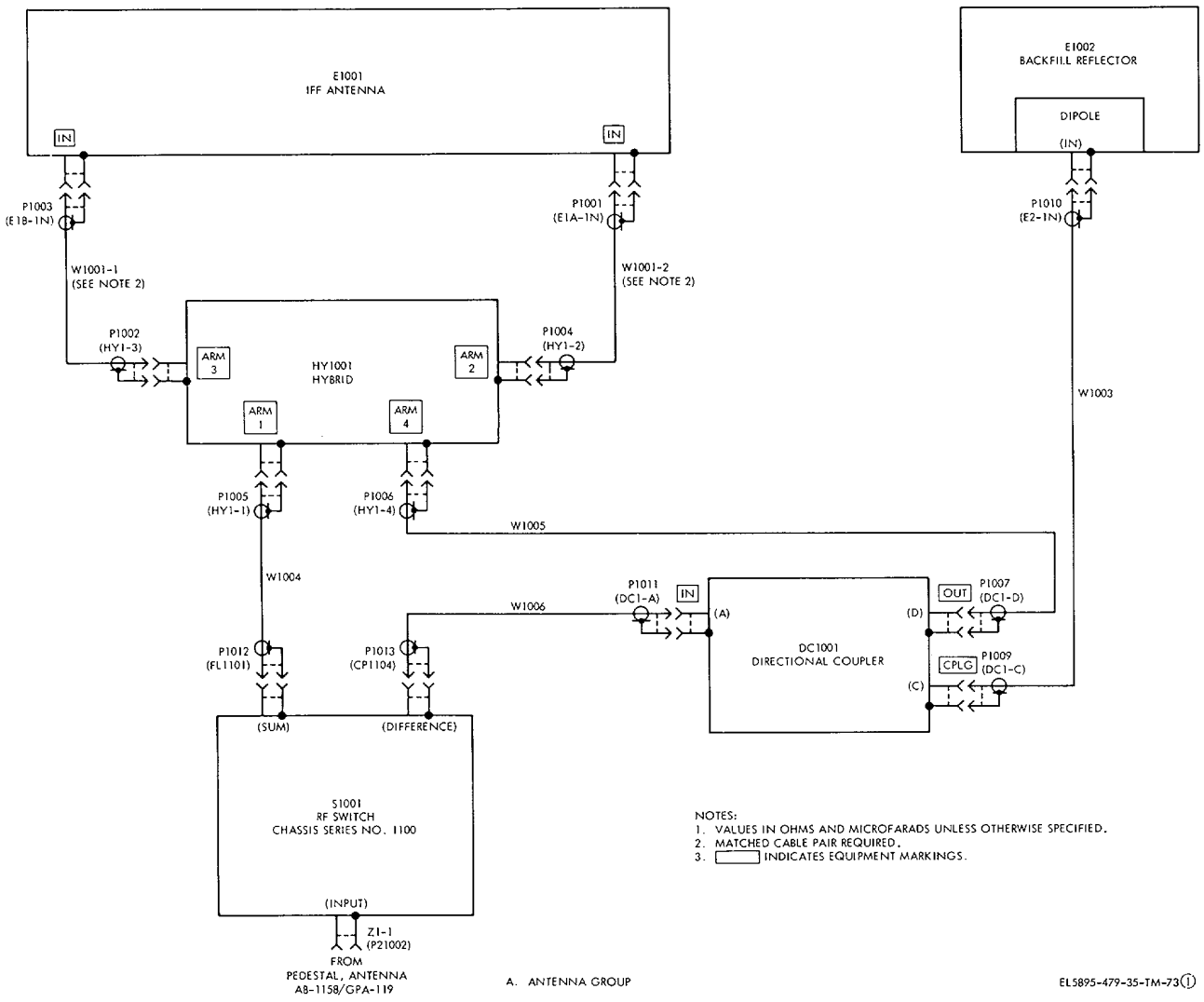


Figure FO-14 (1). Antenna AS-1 796/GPA-119, schematic diagram (sheet I of 2).

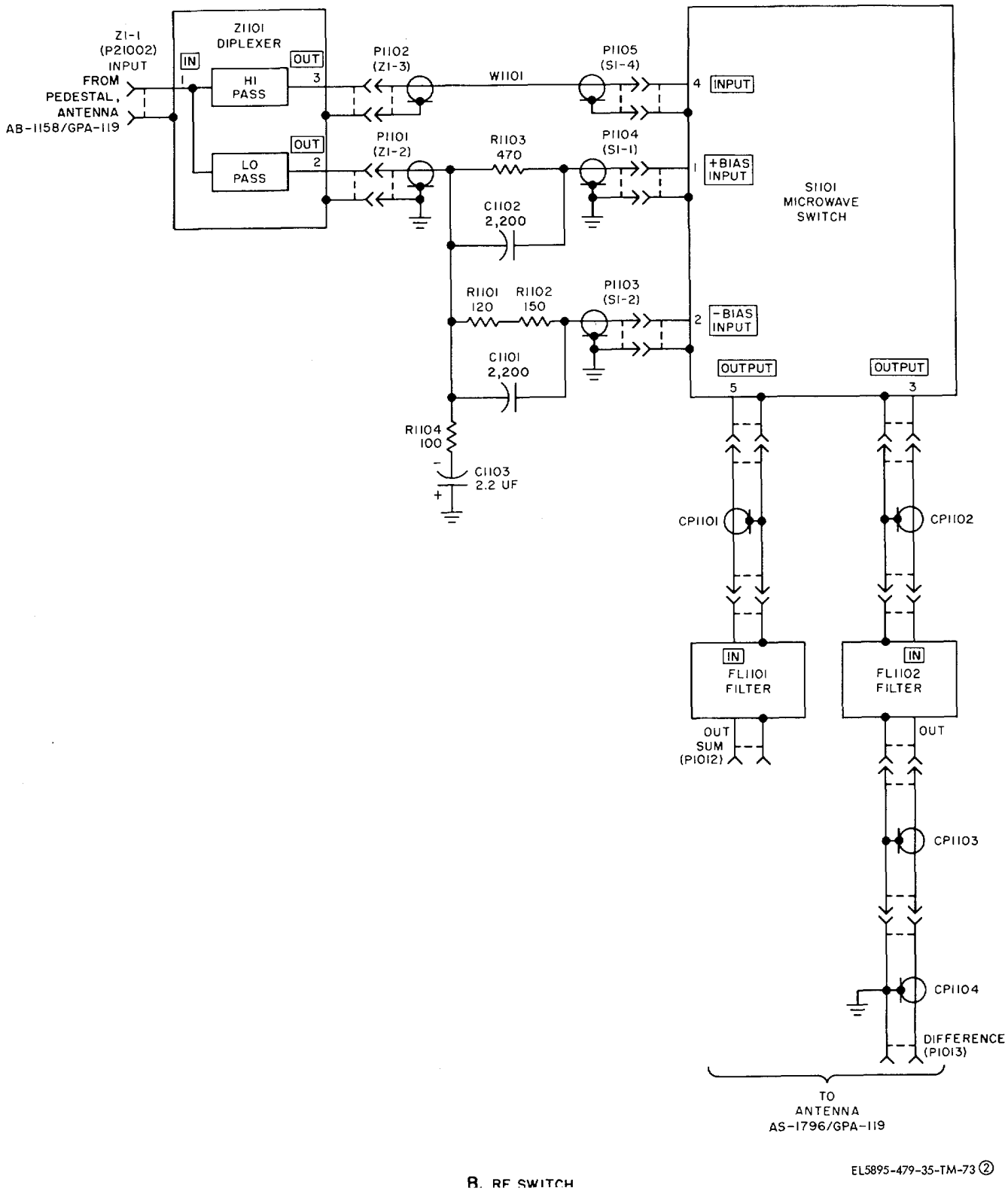


Figure FO-14 (2). Antenna AS-1 796/GPA- 119, schematic diagram (sheet 2 of 2).

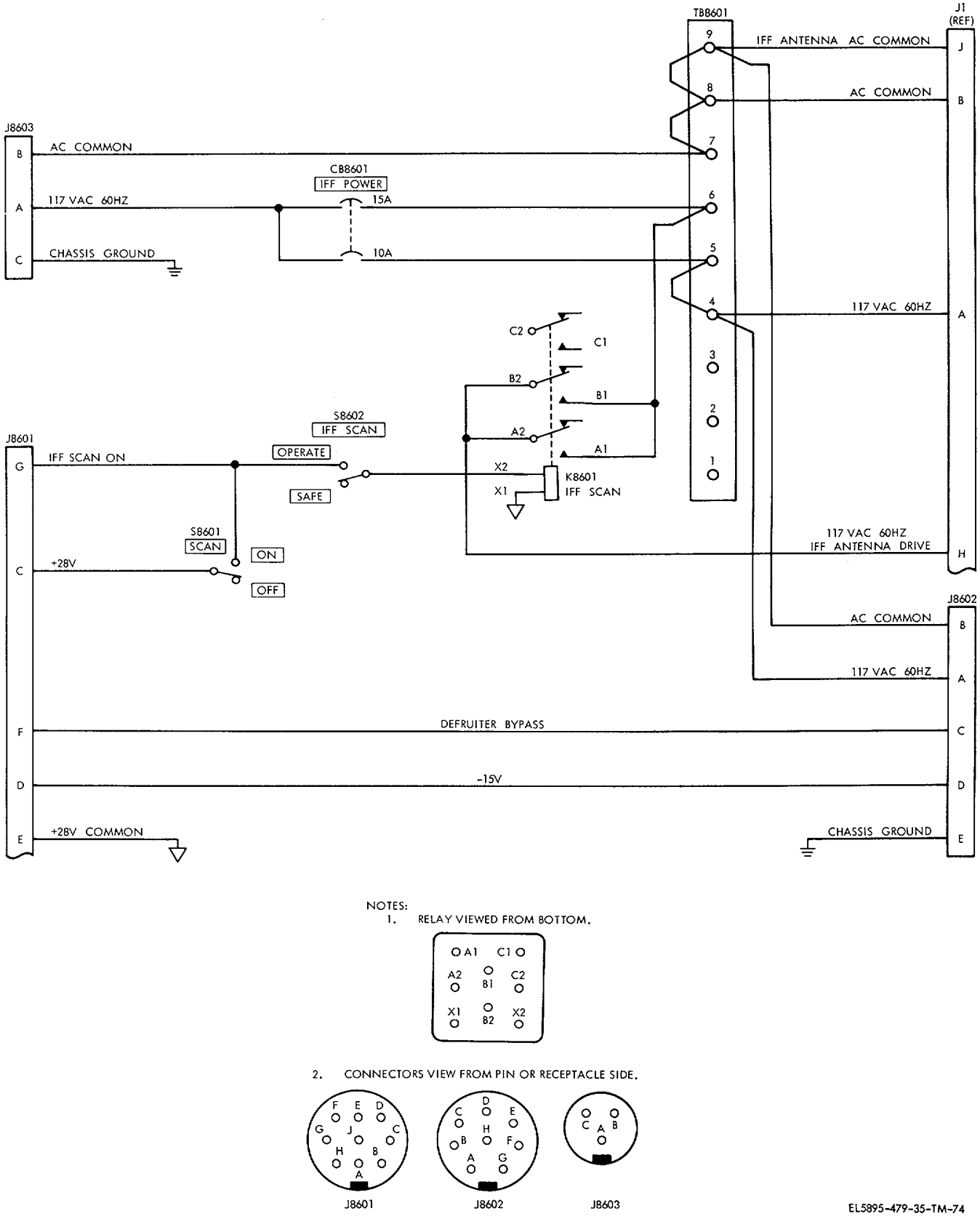


Figure FO-15. Interconnecting Box J-2945/TPX-41, schematic diagram.

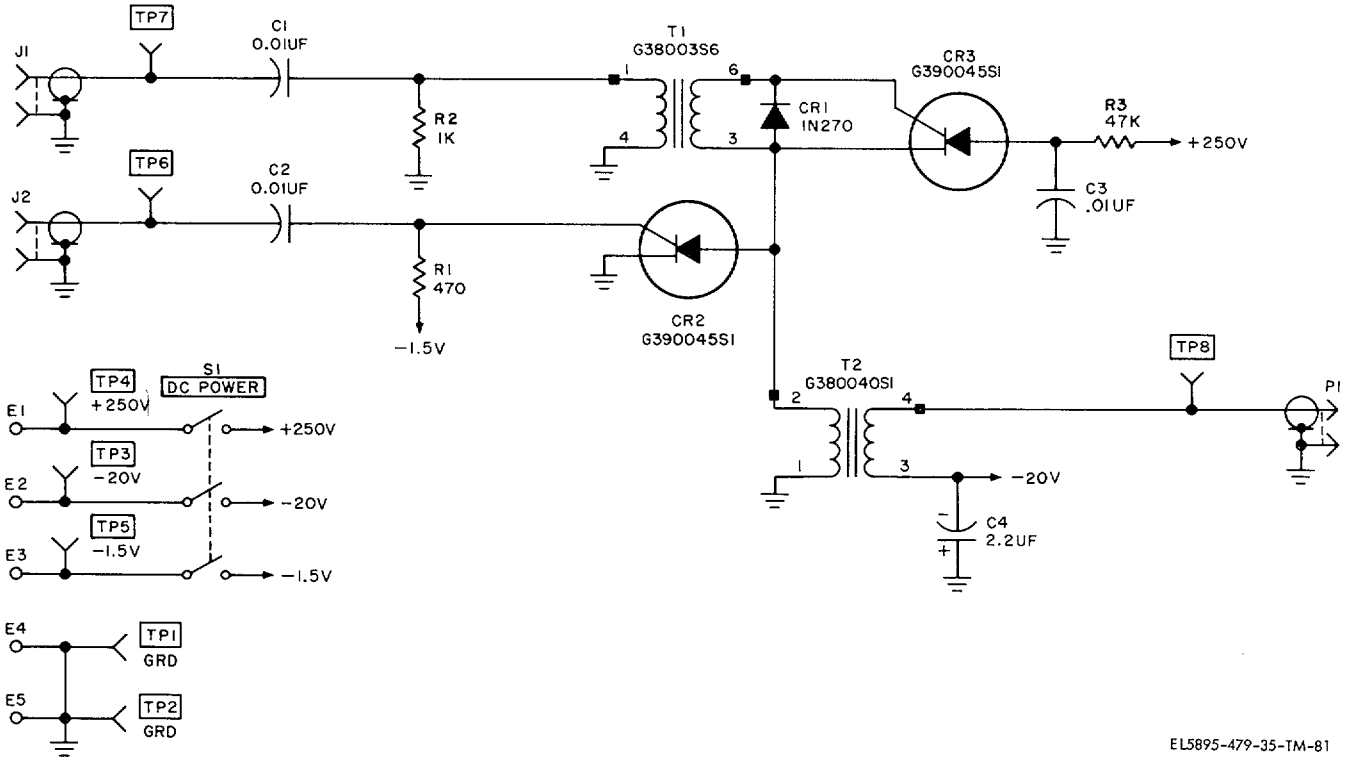
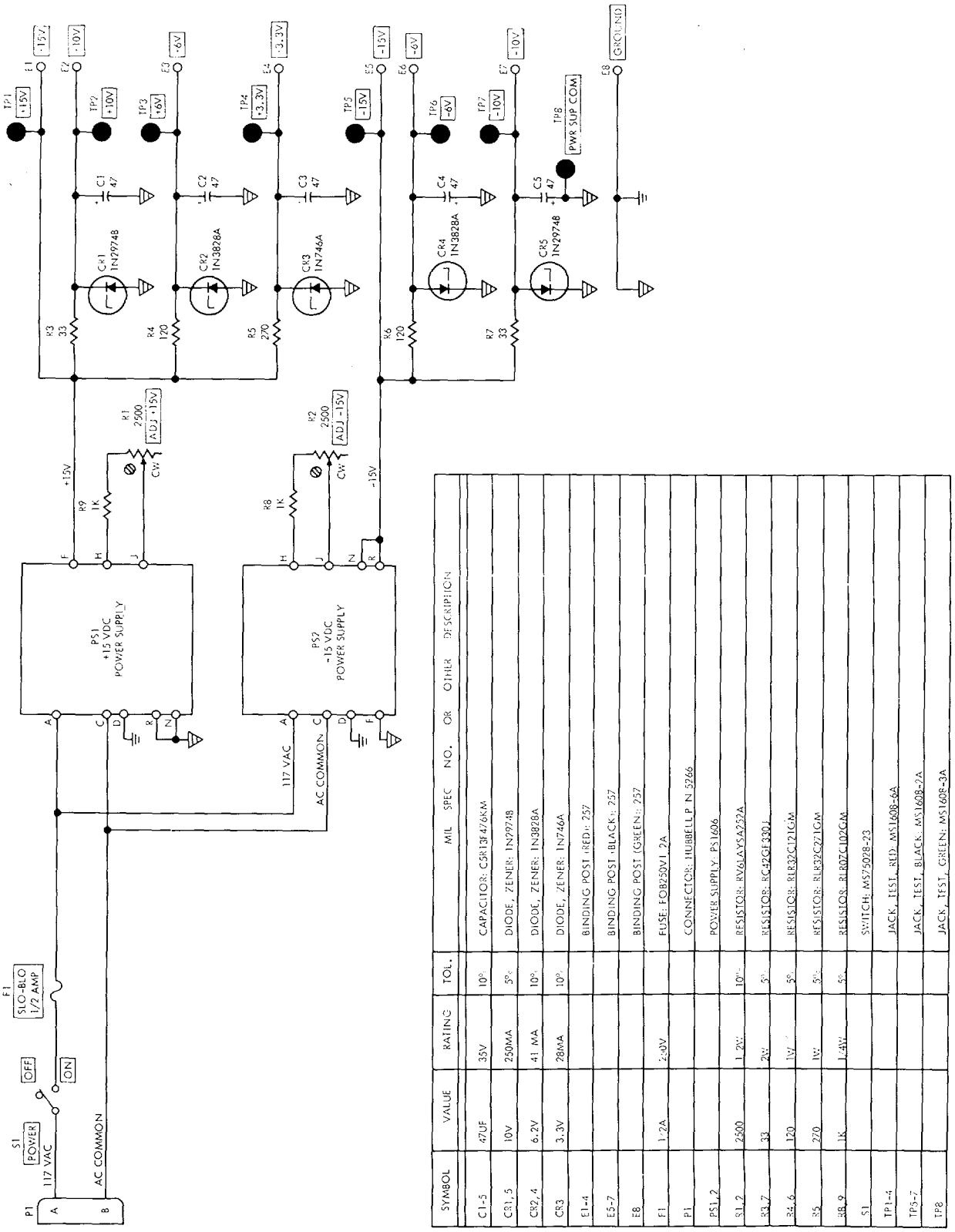


Figure FO-22. Antenna AS-1 796/GPA-1 119, RF switch test generator schematic diagram.



SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO. OR OTHER DESCRIPTION
C1-5	47UF	35V	10%	CAPACITOR: CSR13F476KM
CR1,5	10V	250MA	5%	DIODE, ZENER: 1N29748
CR2,4	6.2V	41 MA	10%	DIODE, ZENER: 1N3828A
CR3	3.3V	28MA	10%	DIODE, ZENER: 1N746A
E1-4				BINDING POST (RED): 257
E5-7				BINDING POST (BLACK): 257
E8				BINDING POST (GREEN): 257
F1	1/2A	250V		FUSE: FOB250V1/2A
P1				CONNECTOR: HUBBELL P N 5266
PS1,2				POWER SUPPLY: PS1606
R1,2	2500	1 2W	10%	RESISTOR: RV6LAY5A252A
R3,7	33	2W	5%	RESISTOR: RC42GF330J
R4,6	120	1W	5%	RESISTOR: RLR32C121GM
R5	270	1W	5%	RESISTOR: RLR32C271GM
R8,9	1K	1/4W	5%	RESISTOR: RLR07C102GM
S1				SWITCH: MS75028-23
TP1-4				JACK, TEST, RED: MS1608-6A
TP5-7				JACK, TEST, BLACK: MS1608-2A
TP8				JACK, TEST, GREEN: MS1608-3A

Figure FO-23. Bench test power supply.

By Order of the Secretary of the Army:

W. C. WESTMORELAND,
General, United States Army,
Chief of Staff.

Official:
VERNE L. BOWERS,
Major General, United States Army,
The Adjutant General.

Distribution:

Active Army:

CNGB (1)
Dir of Trans (1)
COE (1)
TSG (1)
CofSptS (1)
ACSC-E (2)
USAMB (10)
USAARENBD (2)
USASA (2)
USACDC (2)
USACDCCEA (1)
USACDCCEA Ft Huachuca (1)
CONARC (2)
USAMC (1)
USAMICOM (2)
USATECOM (2)
USAMUCOM (2)
ARADCOM (2)
ARADCOM Rgn (1)
USAECOM (2)
OS Maj Comd (2)
USACDCEC (10)
USASTRATCOM (2)
USAESC (70)
Armies (1)
USASESS (5)
Svc Colleges (1)
Fort Huachuca (5)
Fort Carson (7)
WSMR (2)
USAERDAA (2)
USAERDAW (2)
USACRREL (2)
Army Dep (1) except
LBAD (14)
SAAD (30)
TOAD (14)
LEAD (7)
ATAD (10)
NAAD (3)
SVAD (3)
Gen Dep (1)
Sig Sec Gen Dep (5)
Sig Dep (10)
Sig FLDMS (1)
1st Cav Div (2)
Ft Richardson (USAECOM Ofc) (2)
AAF (1)
USARV (5)
USAAVNS (2)
Units org under fol TOE:
(1 copy each)
11-158
29-134
29-136

NG: None

USAR: None

For explanation of abbreviations used, see AR 310-50.

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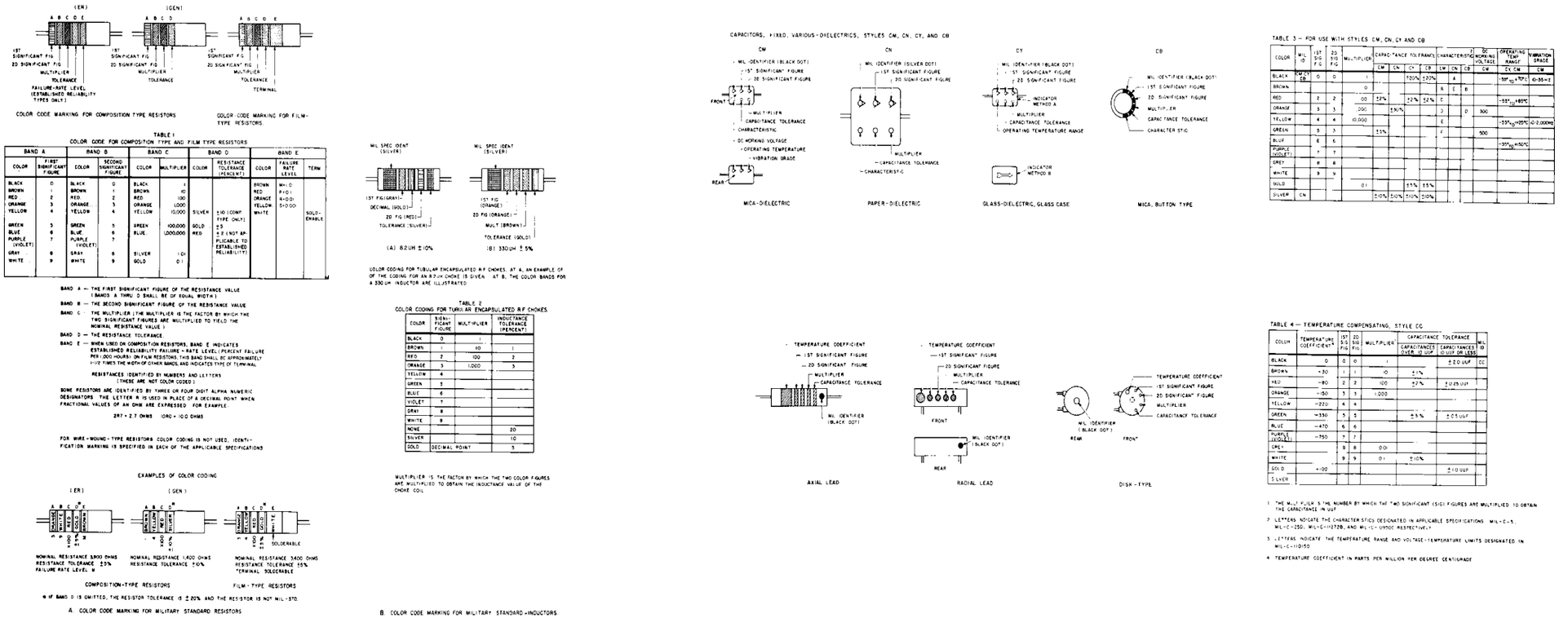


Figure FO-1. Military standard resistor, inductor, and capacitor color coding.

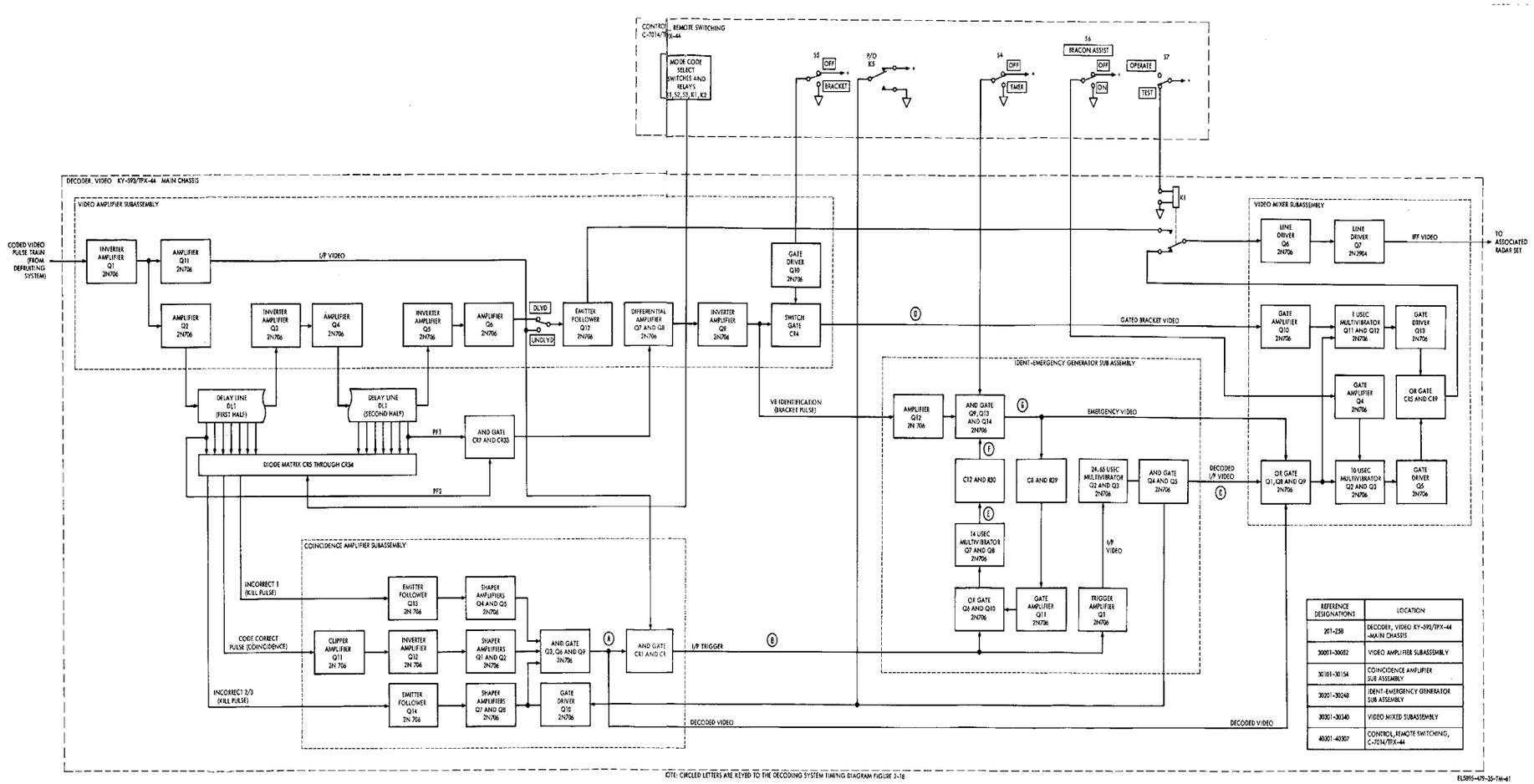


Figure FO-2. Decoding system, block diagram.

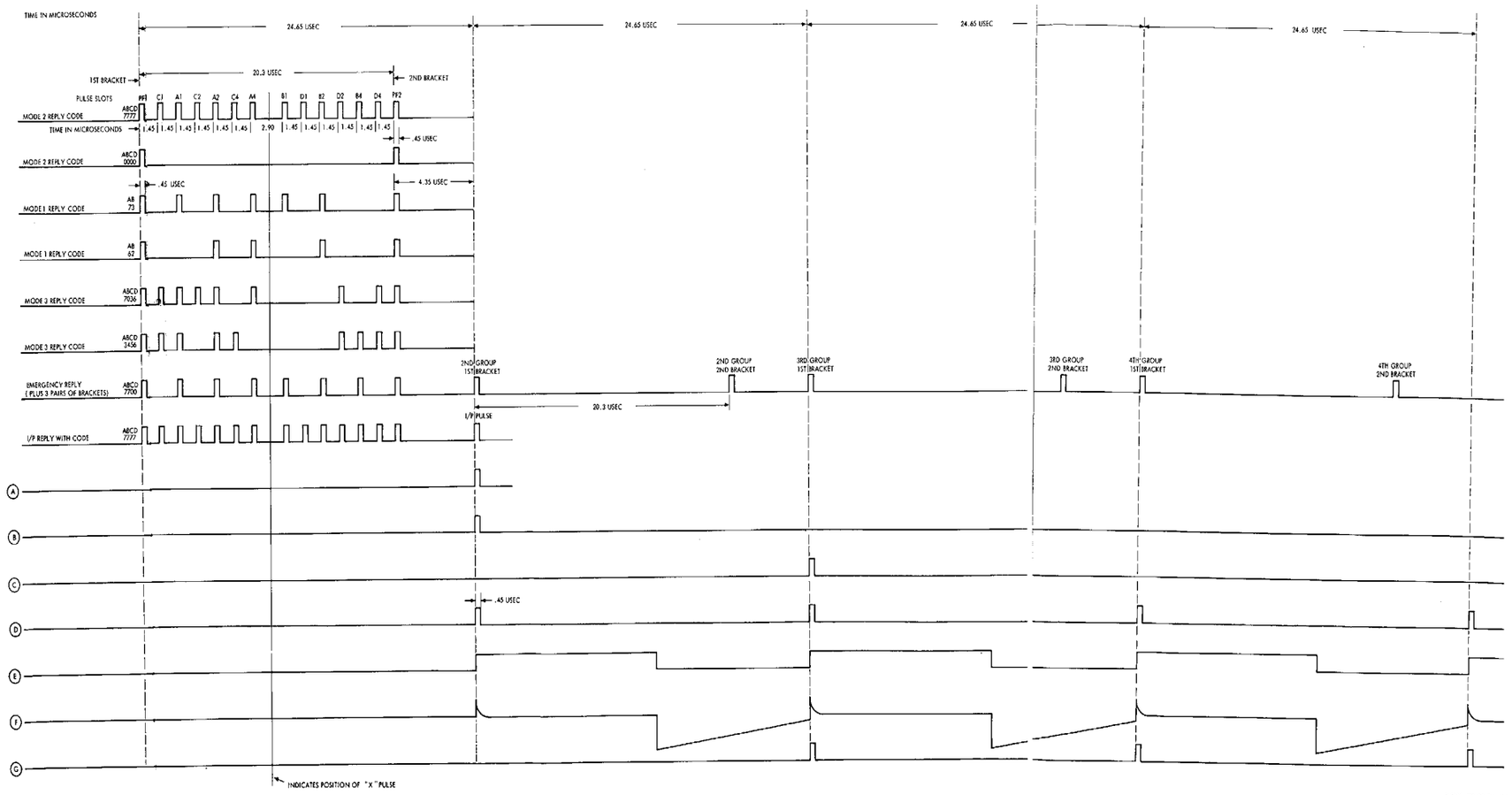


Figure FO-3. Decoding system, timing diagram.

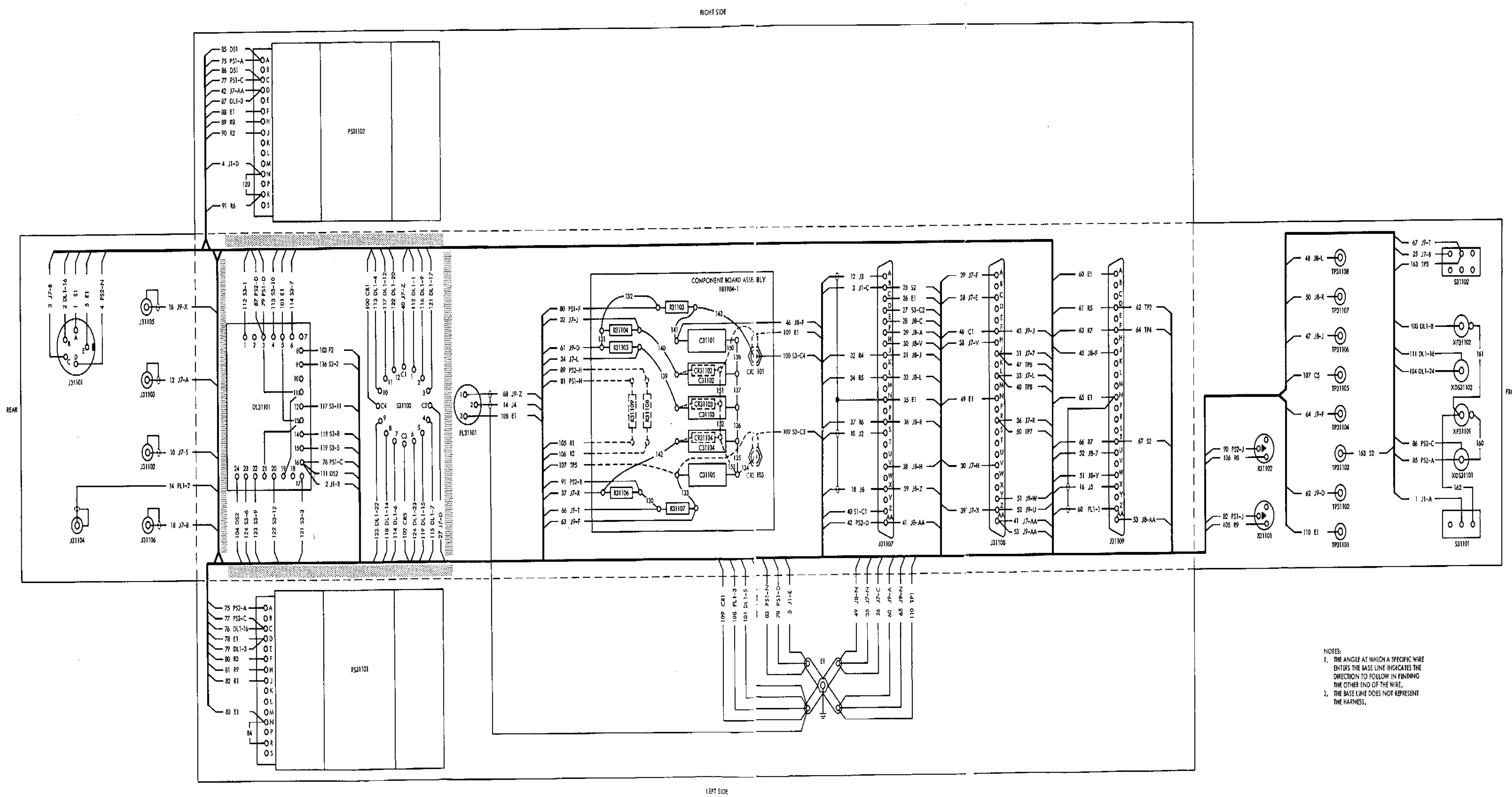


Figure FO-4 (1). Blanker, Interference MX-8795/TPX-41, wiring diagram (sheet 1 of 4).

Change 1

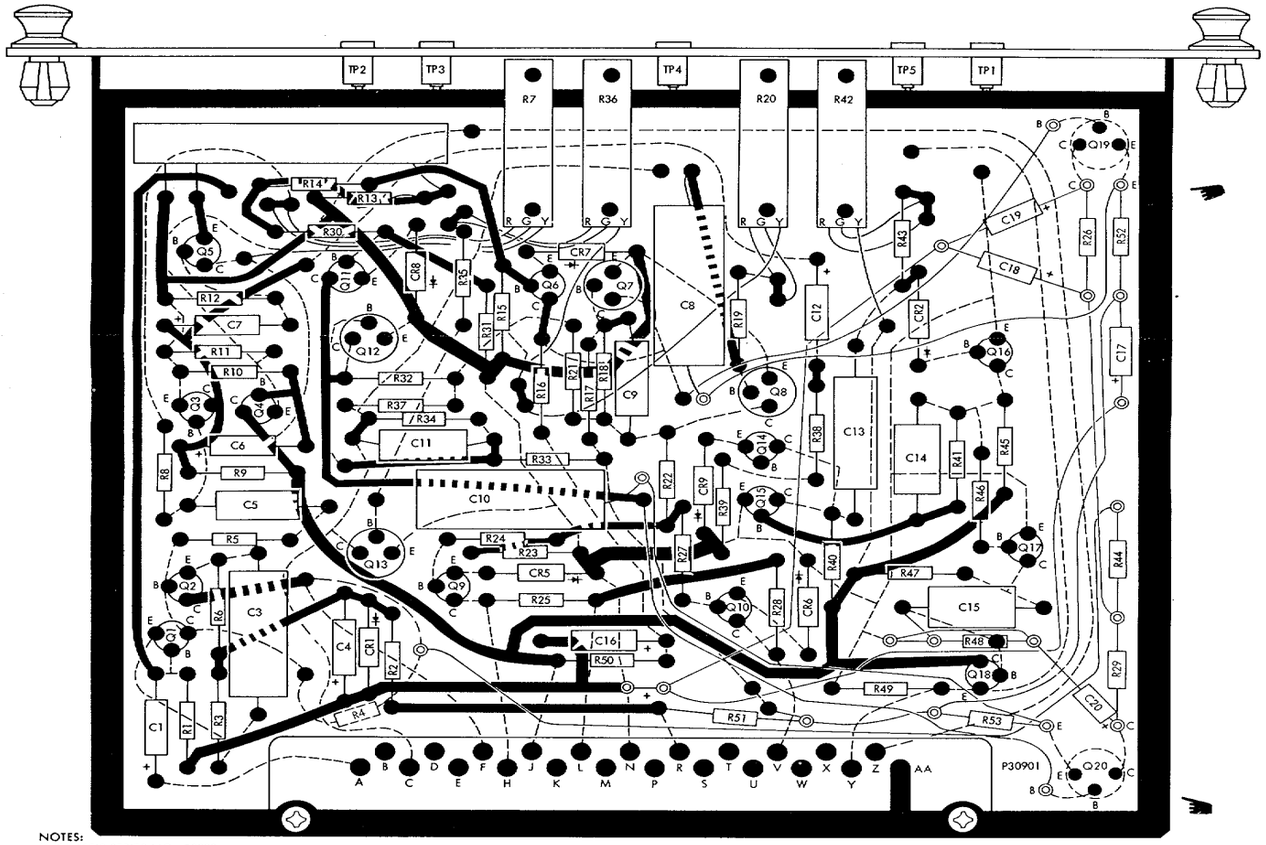


Figure FO-4 (2). Blanker, Interference MX-8795/TPX-41, wiring diagram (sheet 2 of 4).

Change 1

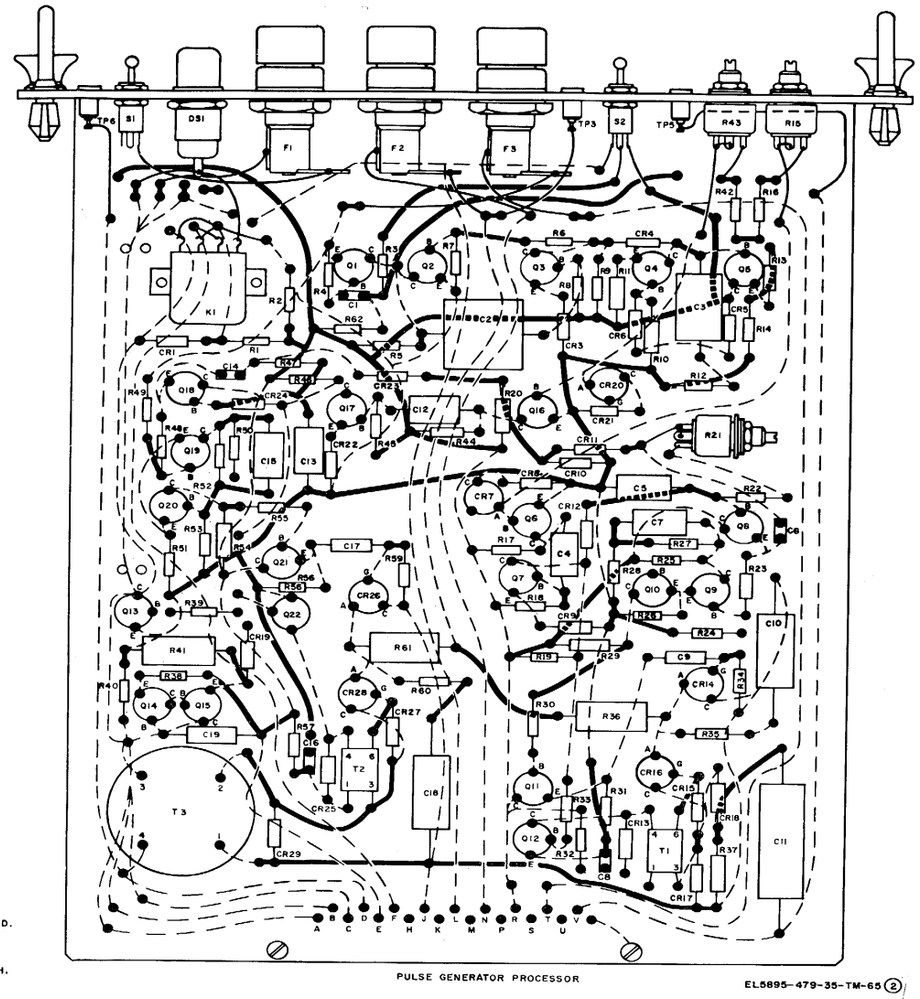


Figure FO-6 (2). Modulator, Pulse MD-638/TPX-41, wiring diagram (sheet 2 of 2)

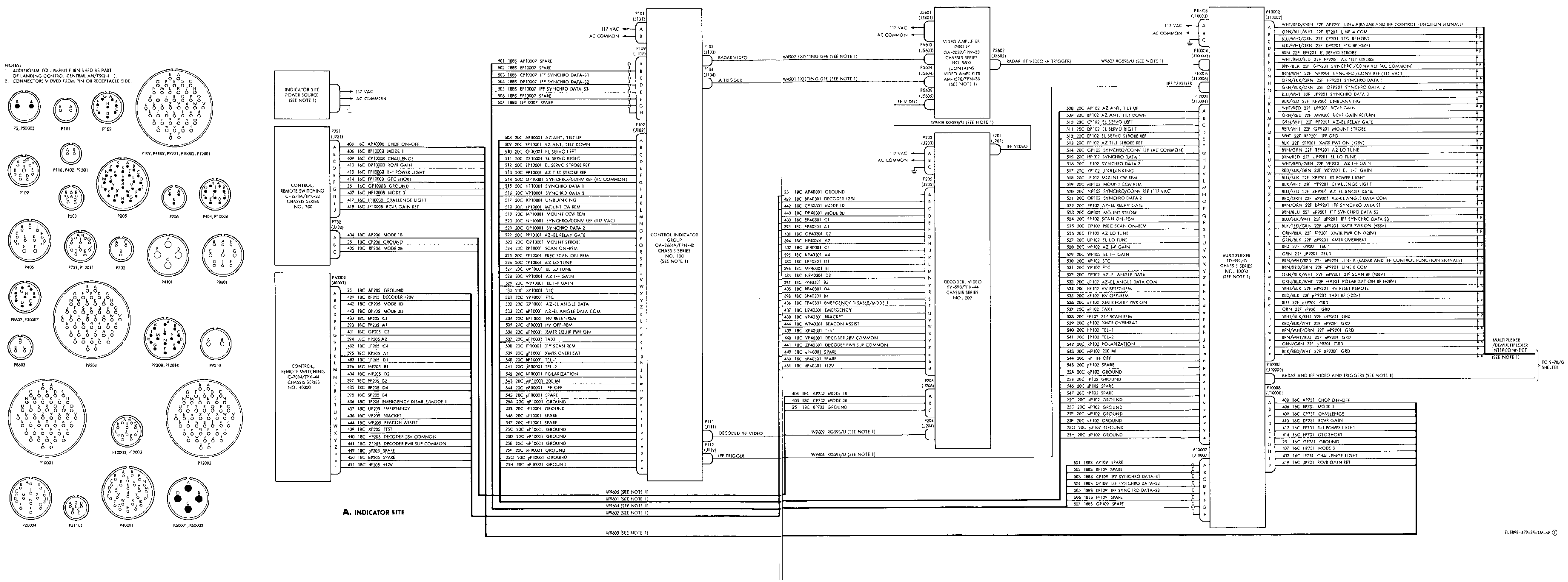


Figure FO-9 (1). Interrogator Set AN/TPX-41, interconnecting diagram (sheet 1 of 2)

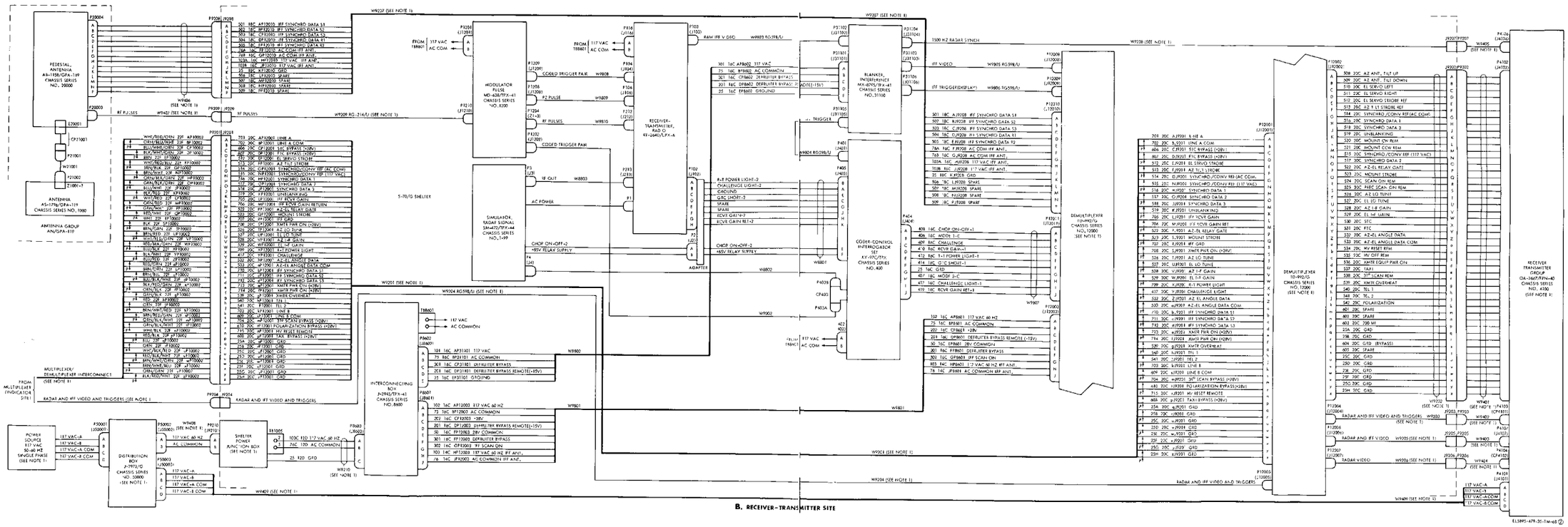


Figure FO-9 (2). Interrogator Set AN/TPX-41 interconnecting diagram (sheet 2 of 2)

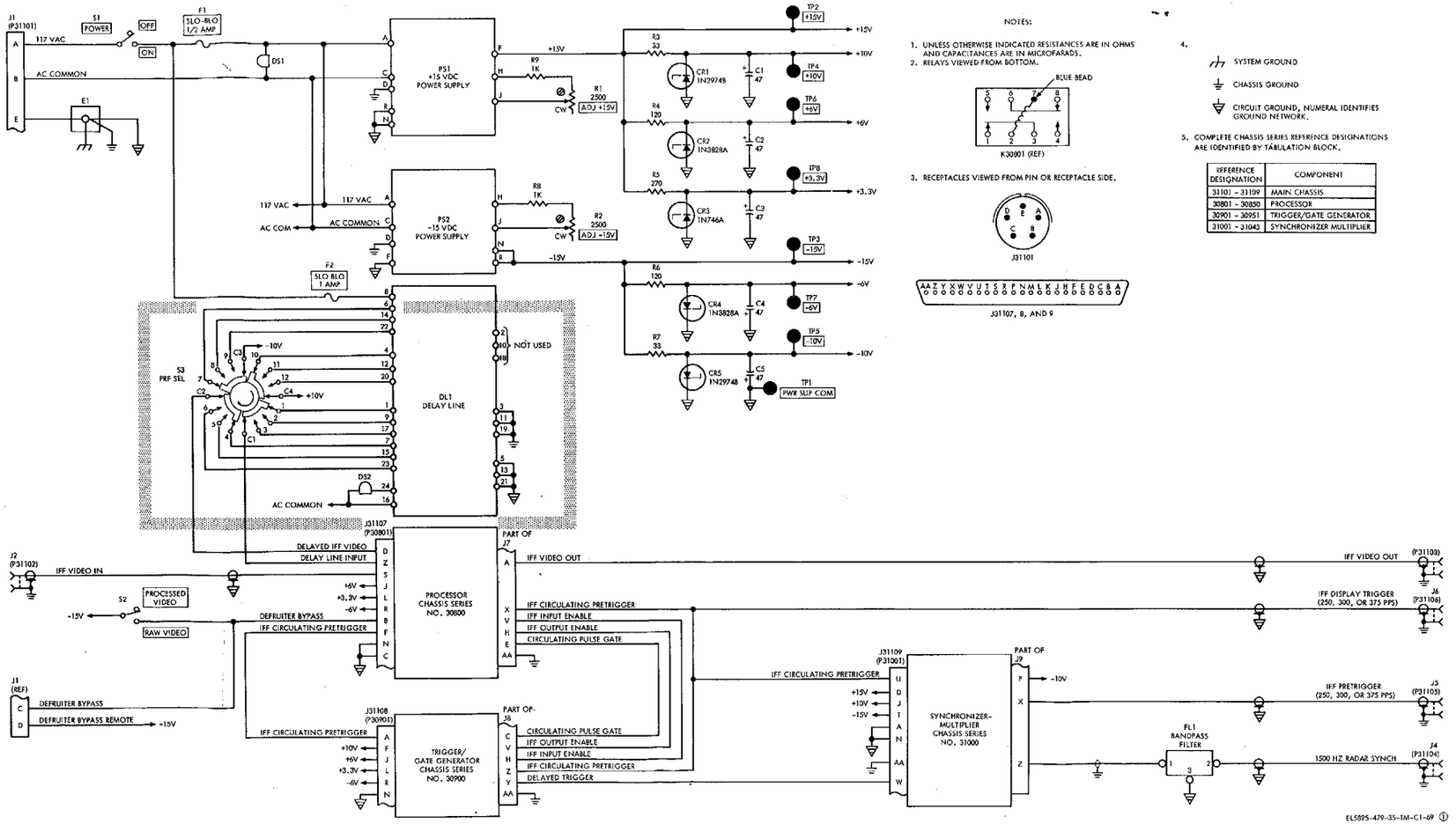


Figure FO-10 (1). Blanker, Interference MS-8795/TPX-41, schematic diagram (sheet 1 of 4) **CHANGE 1**

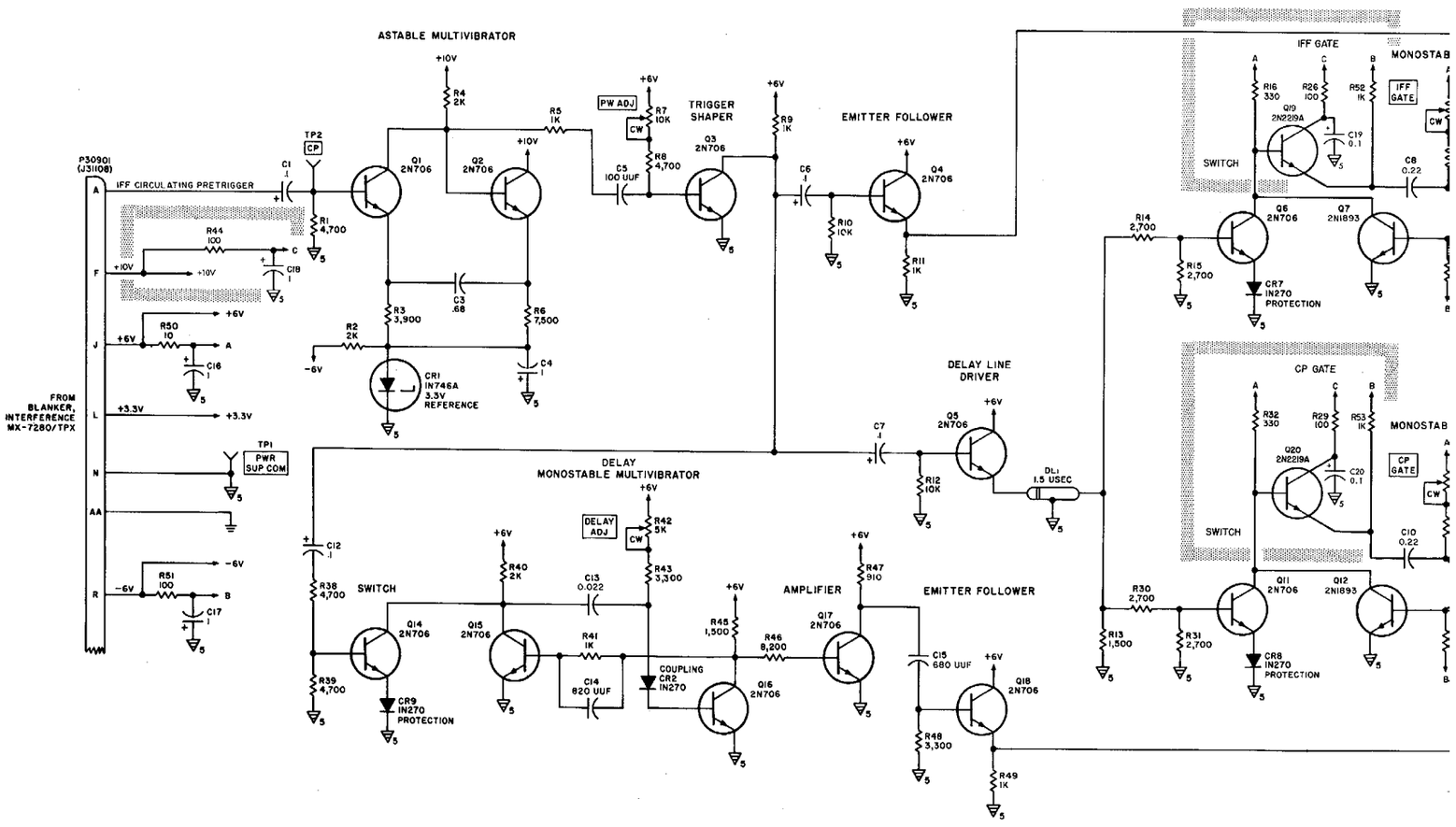


Figure FO-10 (2). Blanker, Interference MX-879/TPX-41, schematic diagram (sheet 2 of 4) **CHANGE 1**

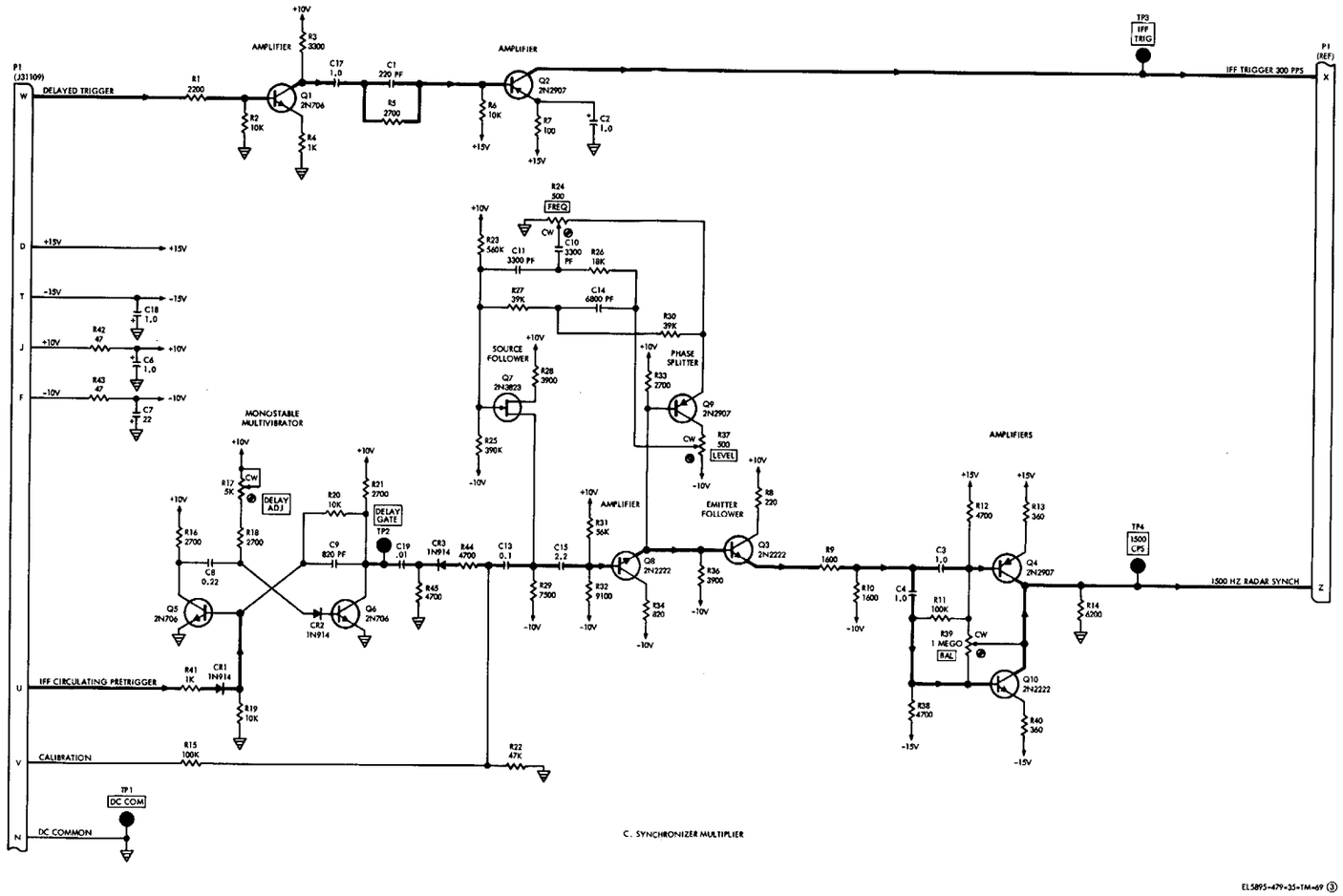


Figure FO-10 (3). Blanker, Interference MX-8795/PX-41, schematic diagram (sheet 3 of 4).

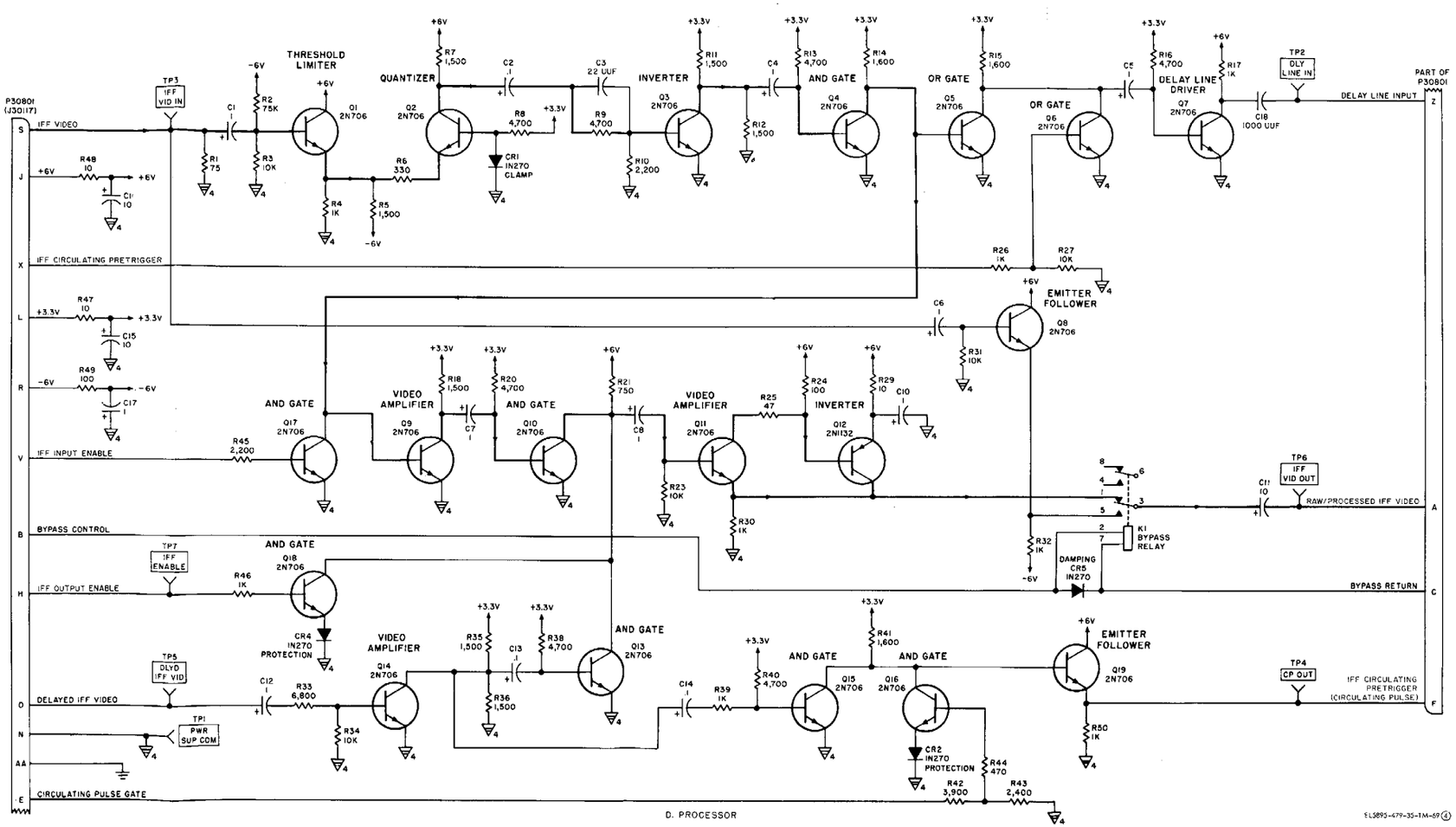


Figure FO-10 (4). Blanker, Interference MX-8795/TPX-41, schematic diagram (sheet 4 of 4).

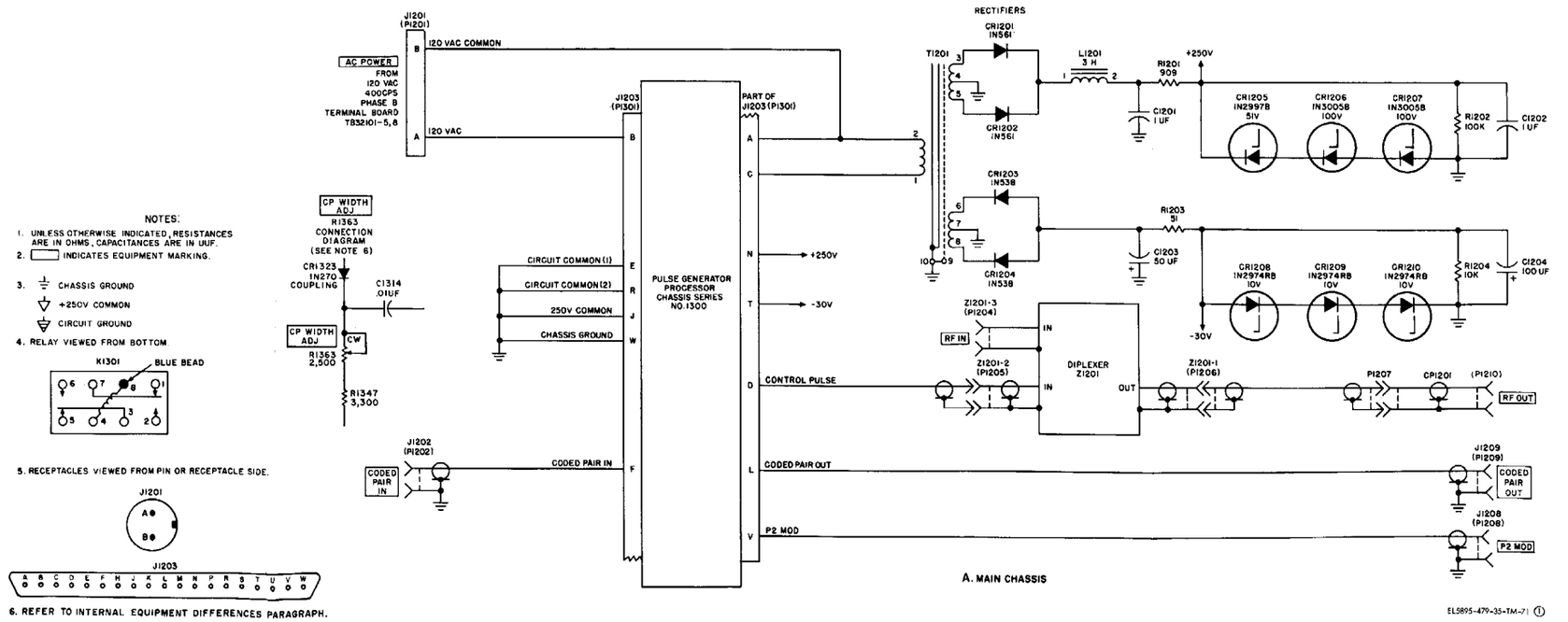


Figure FO-12 (1). Modulator, Pulse MD-638/TPX-41, schematic diagram (sheet 1 of 2).

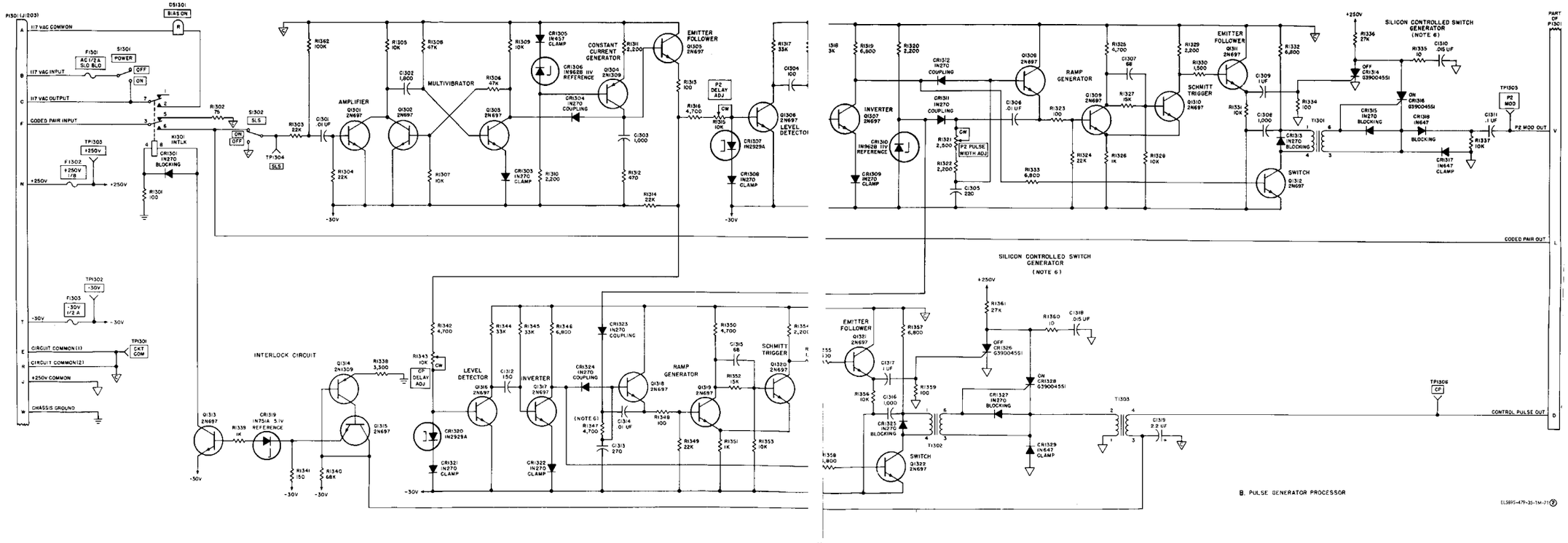
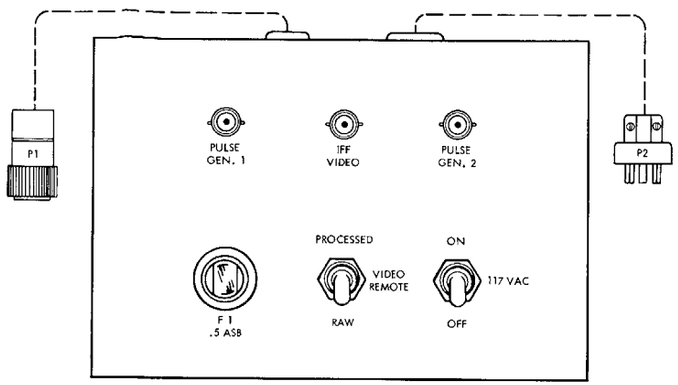
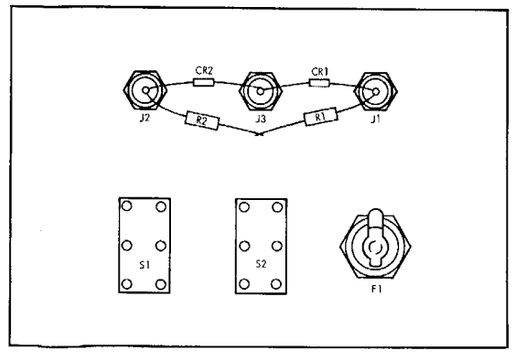
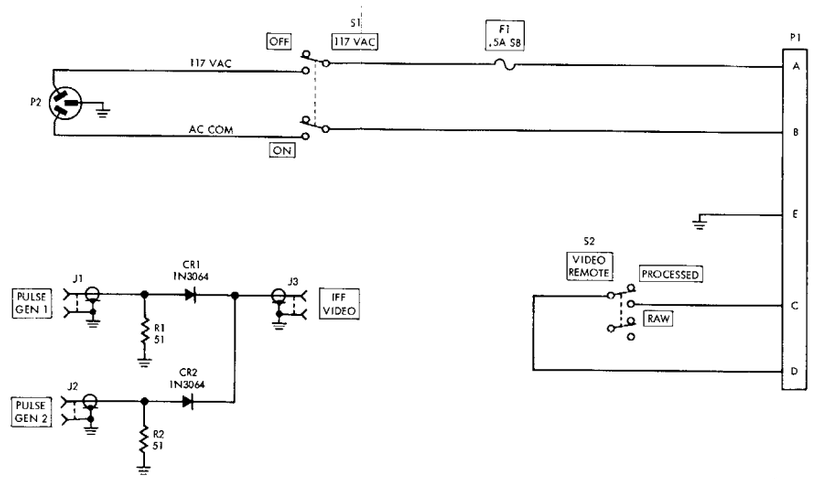


Figure FO-12 (2). Modulator, Pulse MD-638/TPX-41, schematic diagram (sheet 2 of 2).

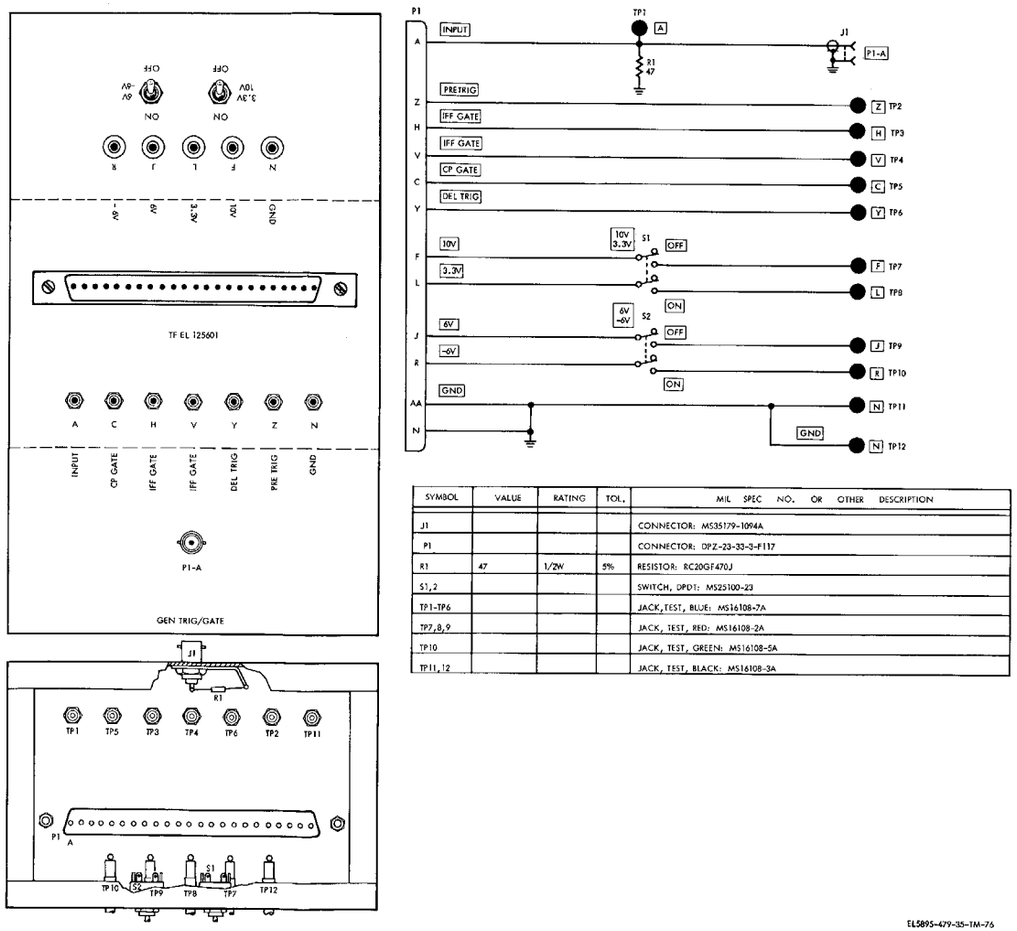






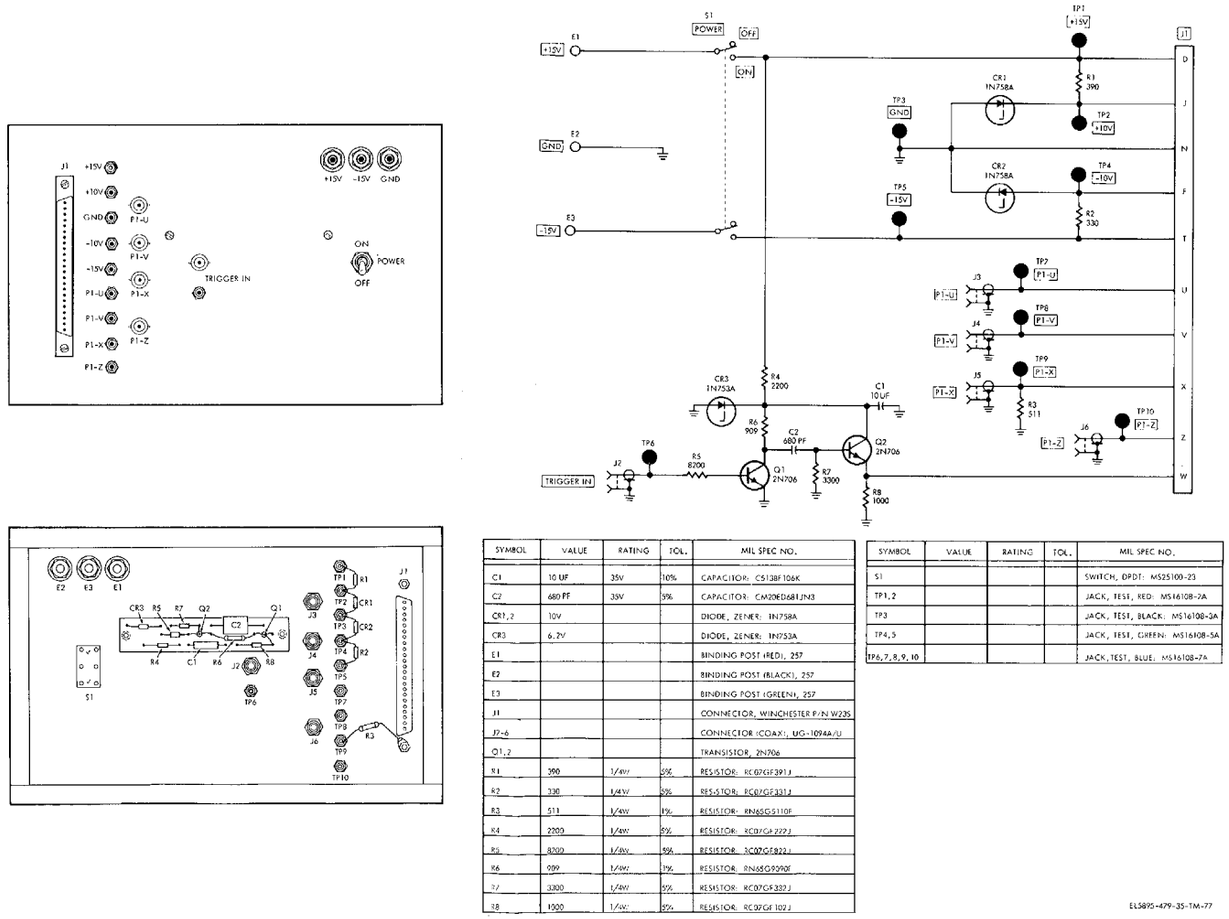
SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO. OR OTHER DESCRIPTION
CR1, 2				DIODE, IN3064
F1	1/2A			FUSE, F028250V 1/2A SLO BLO
J1,2,3				CONNECTOR (COAX) UG1094/U
P1				CONNECTOR: MS3106E16-5-8S
P2				CONNECTOR: 5266
R1,2	51	1/2W	5%	RESISTOR: RC20GF510J
S1,2				SWITCH, DPDT: MS25100-23
XF1				FUSE HOLDER: FHL17G1

Figure FO-16. Blanker, Interference MX-8795/TPX-41, test fixture TF181530.



SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO. OR OTHER DESCRIPTION
J1				CONNECTOR: MS35179-1094A
P1				CONNECTOR: DPZ-23-33-3-F117
R1	47	1/2W	5%	RESISTOR: RC20GF470J
S1,2				SWITCH, DPDT: MS25100-23
TP1-TP6				JACK,TEST, BLUE: MS16108-7A
TP7,8,9				JACK, TEST, RED: MS16108-2A
TP10				JACK, TEST, GREEN: MS16108-5A
TP11,12				JACK, TEST, BLACK: MS16108-3A

Figure FO-17. Blanker, Interference MX-8795/TPX-41, trigger/gate generator test fixture TF125601.



SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO.
C1	10 UF	35V	10%	CAPACITOR: CS13BF106K
C2	680 PF	35V	5%	CAPACITOR: CM20ED681J03
CR1,2	10V			DIODE, ZENER: 1N758A
CR3	6.2V			DIODE, ZENER: 1N753A
E1				BINDING POST (RED), 257
E2				BINDING POST (BLACK), 257
E3				BINDING POST (GREEN), 257
J1				CONNECTOR, WINCHESTER P/N W235
J2-6				CONNECTOR (COAX): UG-1094A/U
Q1,2				TRANSISTOR, 2N706
R1	390	1/4W	5%	RESISTOR: RC07GF391J
R2	330	1/4W	5%	RESISTOR: RC07GF331J
R3	511	1/4W	1%	RESISTOR: RN65G5110F
R4	2200	1/4W	5%	RESISTOR: RC07GF222J
R5	8200	1/4W	5%	RESISTOR: RC07GF822J
R6	909	1/4W	1%	RESISTOR: RN65G9090F
R7	3300	1/4W	5%	RESISTOR: RC07GF332J
R8	1000	1/4W	5%	RESISTOR: RC07GF102J

SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO.
S1				SWITCH, DPDT: MS25100-23
TP1,2				JACK, TEST, RED: MS16108-2A
TP3				JACK, TEST, BLACK: MS16108-3A
TP4,5				JACK, TEST, GREEN: MS16108-5A
TP6,7,8,9,10				JACK, TEST, BLUE: MS16108-7A

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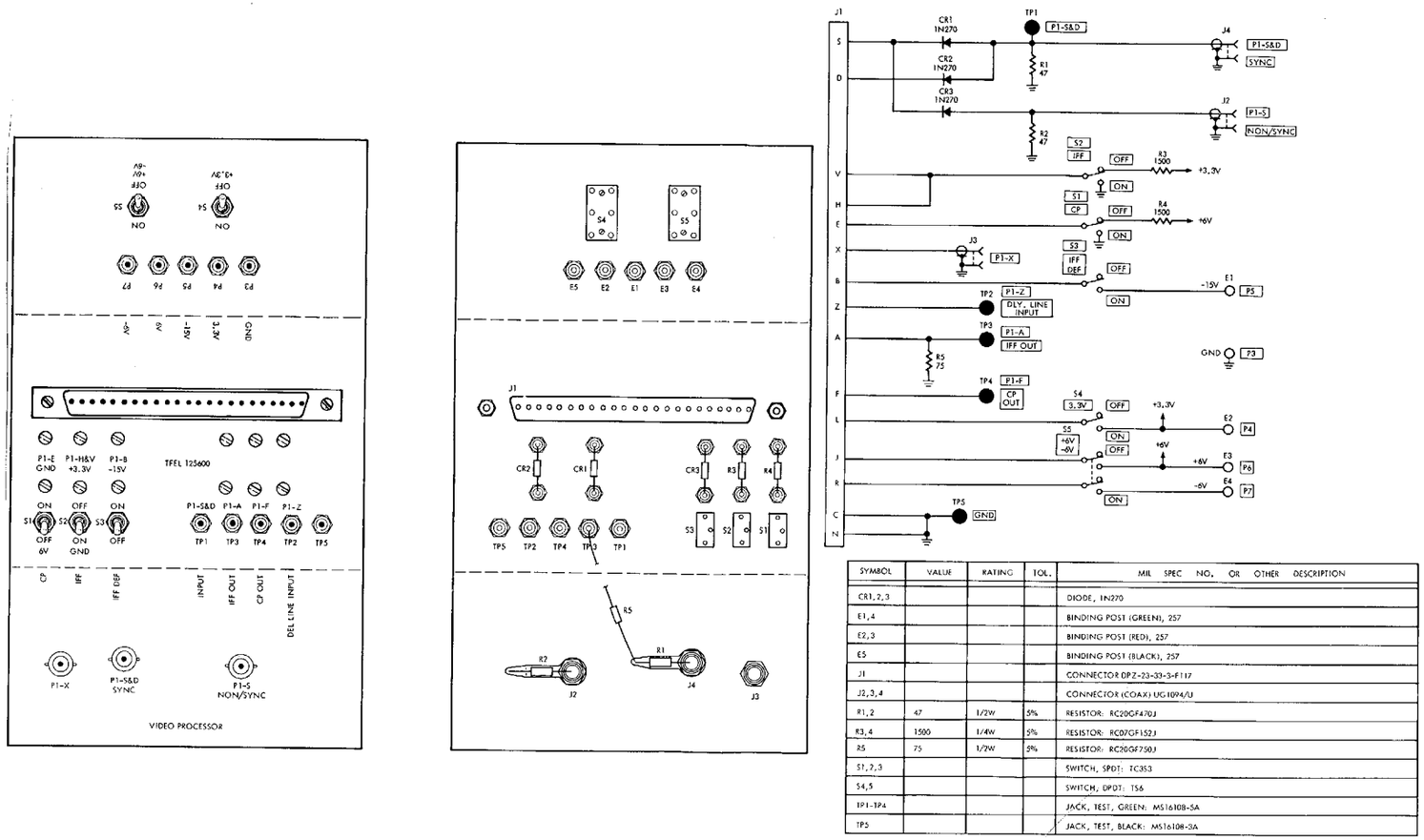
Figure FO-18. Blanker, Interference MX-8795/TPX-41, synchronizer-multiplier test fixture TF170114.



SYMBOL	VALUE	RATING	TOL.	MIL SPEC. NO. OR OTHER DESCRIPTION
CR1,2,3				DIODE, 1N270
E1,4				BINDING POST (GREEN), 257
E2,3				BINDING POST (RED), 257
E5				BINDING POST (BLACK), 257
J1				CONNECTOR DPZ-23-33-3-F117
J2,3,4				CONNECTOR (COAX) UG1094/U
R1,2	47	1/2W	5%	RESISTOR: RC20GF470J
R3,4	1500	1/4W	5%	RESISTOR: RC07GF152J
R5	75	1/2W	5%	RESISTOR: RC20GF750J
S1,2,3				SWITCH, SPDT: TC353
S4,5				SWITCH, DPDT: TS6
TP1-TP4				JACK, TEST, GREEN: MS16108-5A
TP5				JACK, TEST, BLACK: MS16108-3A

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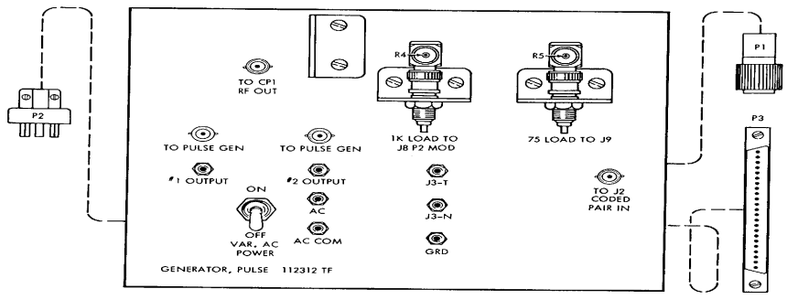
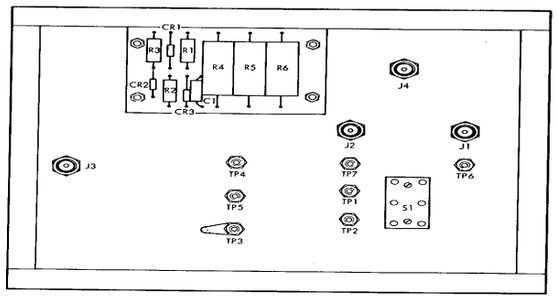
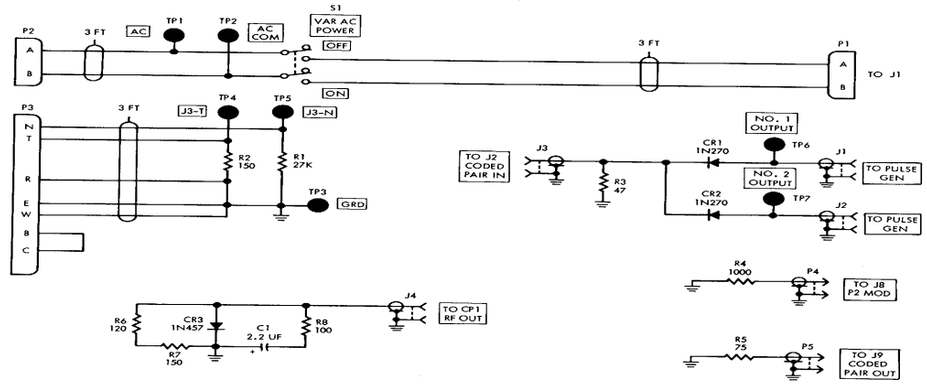
Figure FO-19. Blanker, Interference MX-8795/TPX-41, processor test fixture TF125600.



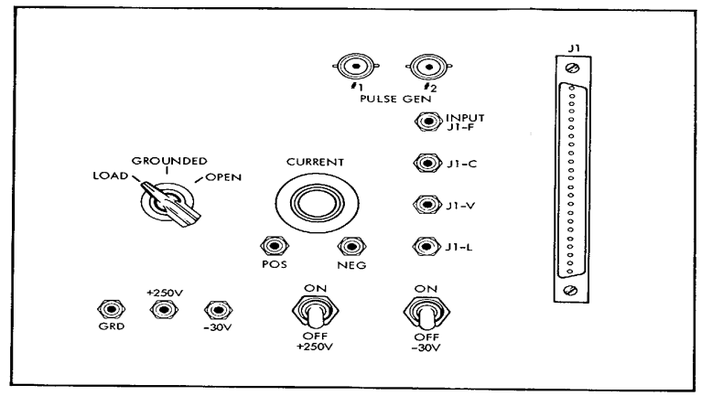


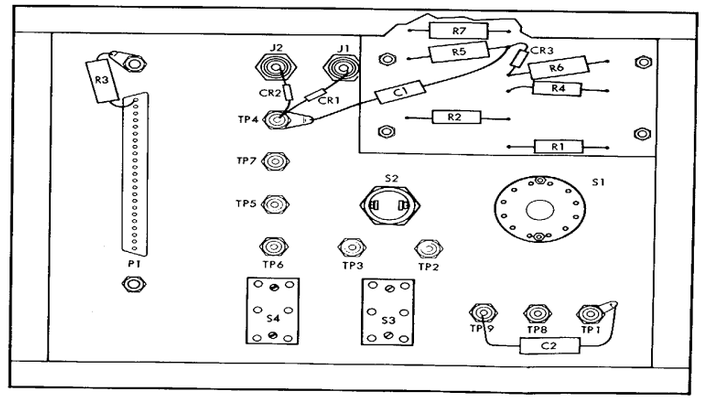


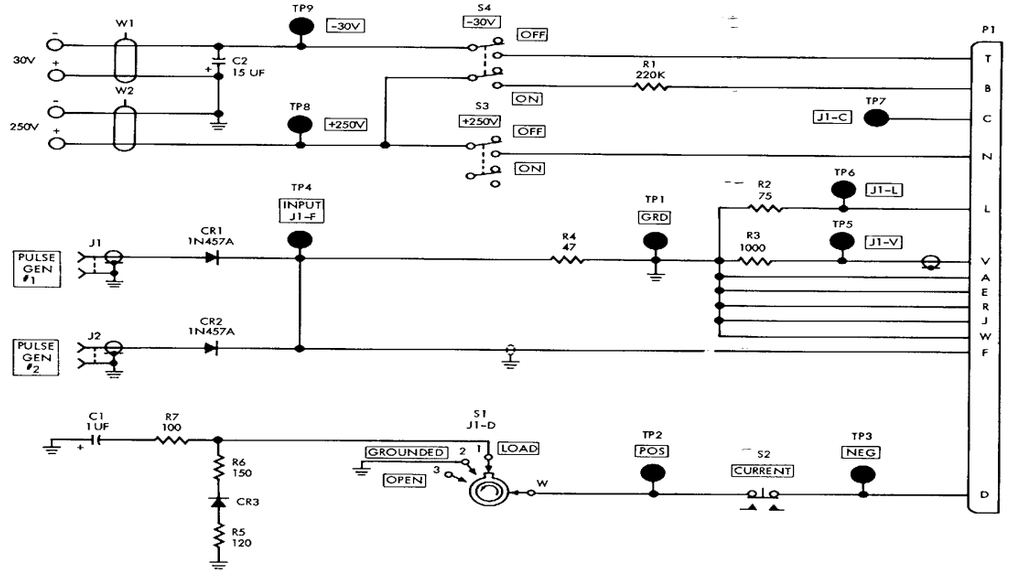
SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO. OR OTHER DESCRIPTION
C1	2.2UF	35V	10%	CAPACITOR: SPRAGUE P/N 150D225X 9035B2
CR1,2				DIODE: 1N270
CR3				DIODE: 1N457
J1-4				CONNECTOR, COAX, UG1094/U
P1				CONNECTOR, MS3106E1654S
P2				CONNECTOR, HUBBELL P/N 5266
P3				CONNECTOR, DPZ19-34B
P4				CONNECTOR, COAX, 8575
P5				CONNECTOR, COAX, 8575
R1	27K	1W		RESISTOR: RC20GF273
R2	150	12W	5%	RESISTOR: OHMITE P/N 1722
R3	47	1/2W	5%	RESISTOR: RC20GF470J
R4	1000	1/2W	5%	RESISTOR: RC20GF102J
R5	75	1/2W	5%	RESISTOR: RC20GF750J
R6	120	3W	5%	RESISTOR: OHMITE P/N 2762
R7	150	5W	5%	RESISTOR: OHMITE P/N 2874
R8	100	2W	5%	RESISTOR: RC42GF101J
S1				SWITCH, TOGGLE, DPDT, MS25100-23
TP1,2				JACK, TEST, ORANGE: MS16108-6A
TP3-7				JACK, TEST, BLUE: MS16108-7A

EL5895-479-35-TM-79

Figure FO-20. Modulator, Pulse MD-638/TPX-41, test fixture TF112312.







SYMBOL	VALUE	RATING	TOL.	MIL SPEC NO. OR OTHER DESCRIPTION
C1	1 UF	450WV		CAPACITOR, ELECTROLYTIC: TVA-1700
C2	15 UF	50 VDC		CAPACITOR, ELECTROLYTIC
CR1,2				DIODE: 1N457A
J1,2				CONNECTOR (COAX), UG1094A/U
P1				CONNECTOR, DPZ19-33-3F117
R1	220K	1/2W	5%	RESISTOR: RC20GF224J
R2	75	1/2W	5%	RESISTOR: RC20GF750J
R3	1000	1/2W	5%	RESISTOR: RC20GF1001J
R4	47	1/2W	5%	RESISTOR: RC20GF470J
R5	120	2W	5%	RESISTOR: RC42GF121J
R6	150	2W	5%	RESISTOR: RC42GF151J
R7	100	2W	5%	RESISTOR: RC42GF101J
S1				SWITCH, ROTARY: PA2003
S2				SWITCH, SPDT (PUSH-BUTTON): MS25089-3CR
S3,4				SWITCH, DPDT: MS251000-23
TP1				JACK, TEST, BLACK: MS16108-3A
TP2-7				JACK, TEST, BLUE: MS16108-7A
TP8				JACK, TEST, RED: MS16108-2A
TP9				JACK, TEST, GREEN: MS16108-5A

EL5895-479-35-TM-80

Figure FO-21. Modulator, PUlse MD-638/TPX-41, pulse generator processor test fixture TF119849.

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